Functional requirements for HVDC grid systems and subsystems

InterOPERA

Enabling multi-vendor HVDC grids

ABOUT INTEROPERA:

The InterOPERA project will define technical frameworks and standards for electricity transmission and accelerate the integration of renewable energy. Ensuring that HVDC systems, HVDC transmission systems or HVDC components from different suppliers can work together – making them "interoperable"- is a top priority to accelerate Europe's energy transition.

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2.3	25/02/2025	T2.1 group	

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1. Abbreviations and definitions

AC/DC	alternating current / direct current
CBC	Current Breaking Capability
CO	Continuous Operation
CS	Converter Station
DCGC	DC grid controller
DCR	DC Reactor
DCSS	DC Switching Station
DCSU	DC Switching Unit
DCVLM	DC Voltage Limiting mode
DCVSM	DC Voltage Sensitive mode
DMR	Dedicated Metallic Return
DUT	Device under test
ERTS	Earth Return Transfer Switch
EMT	Electromagnetic Transients
FCLD	Fault Current Limiting Device
FCST	Fault Current Suppression Time
FSD	Fault Separation Device
FIZ	Fault Isolation Zone
FRR	Frequency Restoration Reserve
FRT	Fault-Ride-Through
FSZ	Fault Separation Zone
GSC	Grid Side Converter
HV	High Voltage
IM	Islanded mode
KPI	Key Performance Indicator
MMC	Modular Multi-level Converter
MV	Medium Voltage

LDCVSM-O/U	Limited DC Voltage Sensitive Mode-Overvoltage/Undervoltage
LVRT	Low Voltage Ride Through
OVRT	Over Voltage Ride Through
MRTS	Metallic Return Transfer Switch
MT	Multi Terminal
PCS	Peak Current Suppression
PLL	Phase-locked loop
PLES	Pole local earthing switch
PLM	Power Limiting Mode
PoC	Point of Connection
PPM	Power Park Modules
PtG/PtP	Pole-to-Ground/ Pole-to-Pole
RCS	Residual current Switch
(DC)SU	(DC) Switching Unit
TB	Temporary blocking
TIV	Transient Interruption Voltage
TS	Temporary Stop
TSO	Transmission System Operator
ZDD	Zone Distinction Device

2. Executive summary

The European target of installing more than 300GW of offshore wind power in the North Sea by 2050 urges for an increasing need of HVDC systems. In Europe, single vendor turnkey solutions predominate. Consideration of an expandable multi-terminal HVDC grid with multi-purpose interconnectors would significantly improve the power exchange flexibility, the wind power transfer and the global system cost efficiency.

This deliverable provides a guideline for the definition of provisional functional requirements in HVDC systems considering a multi-terminal multi-vendor context. The functional framework supports future expandability and interoperability of HVDC systems by specifying connection requirements at the DC Point of Connection. The proposed functional framework is described in an inclusive and technology-agnostic way. It allows different technical solutions to cohabitate in an HVDC grid and avoid excluding any technical solutions without justification. The proposed functional requirements are purpose oriented, generic, solution-open and justified. They are intended to provide a clear functional split between subsystems to maximise interoperability by design.

Section 4 provides an overview on the functional aggregation of the following subsystems: AC/DC converter station, DC switching station, energy absorber, Power Park Module (PPM) and AC switching station. The subsystems are aggregated based on their primary functional purpose. The AC/DC converter station is a power exchange device. Energy storage and energy absorption are functions assigned to functionally independent subsystems such as energy storage devices and energy absorption devices. A DC switching station includes all relevant DC switchgear and automation functions to ensure connection and disconnection operations for planned and unplanned events. All subsystems are monitored and coordinated with vertical communication interfaces with a DC grid controller and AC/DC dispatch centre. A major result of the functional aggregation is the generic and technology-agnostic definition of the switching unit. The switchgear of a switching unit depends on assigned functionalities. In addition, different switching functions (e.g. fault/load current interruption or energization) and fault detection functions (e.g. for different fault types, primary/backup protection) can be assigned to the switching unit. The aggregation of switchgear is a design choice of the vendor if the functional requirements associated to the switching unit are fulfilled.

The functional requirements at the DC side address multi-disciplinary subjects. To ensure the work progress in a structured way, the following functional groups have been formed: Sequential control, Continuous control, DC grid protection, AC/DC security and dispatch. The main outcomes of each functional group will be outlined in the following.

Sequential control

Within a given HVDC system topology, different DC connection modes are possible. The DC connection modes describe the connection between the individual units within the HVDC system at their DC-PoC. The sequential control describes all actions that allow the HVDC system to switch from one connection mode to another. The main operational modes and transitions are captured in flowchart diagrams. Such transitions may be triggered automatically, or manually by an operator, or a combination of both.

The main states of a switching unit are either "open" or "closed". The transition sequence depends on conditions of surrounding units which are verifiable at switching unit level based on voltage and current quantities. A transition from "open to "closed" state may be carried out by an aggregation sequence (connection of two discharged units), an energization sequence (connection of one charged and one discharged unit) or a synchronization sequence (connection of two charged units). From close to open the transition sequence is characterized by the presence or not of current. Depending on whether fault, load or residual current is observed, the performed sequence and applicable requirements for the switching unit are different.

Finally, a list of functional requirements is provided including the following functions: Command routing, interlocking, aggregation, energization, synchronization, disconnection, separation, isolation, discharge, auto-reclosing, earthing, reconfiguration.

Continuous control

HVDC systems must deliver scheduled power while ensuring their own security and reliability to guarantee continuous operation. It is imperative to prevent power flows and DC voltages that exceed the physical capabilities of system components. Disturbances in the system can disrupt the balance of power, resulting in fluctuations in DC voltages. In such instances, the AC/DC converters within the system must promptly and collectively restore system energy equilibrium to prevent violations of system limits.

The functional group continuous control addresses the overarching control architecture of HVDC systems by defining roles and responsibilities allocated to each layer. Boundary conditions from surrounding AC grids and physical constraints are introduced. These conditions serve as a basis for the functional description of static and dynamic requirements for primary DC voltage control.

A deviation of DC system voltage is an indicator of an imbalance in power flow from the initial load flow, which was originally at equilibrium. The primary DC voltage control plays a crucial role in preventing this imbalance and reaching an equilibrium point of the system. In order to achieve improved security while achieving the maximum exploitation, the multi-segment droop characteristic for primary DC voltage control is defined as a distinct set of control capabilities, each with specific operational requirements.

The stability of the system is determined by the dynamic response of each AC/DC converter and their interactions through the network. To fully satisfy all system-level expectations, each AC/DC converter station must comply with clearly defined performance specifications. A comprehensive set of dynamic performance requirements, evaluation criteria, and appropriate preliminary standalone testbenches are proposed transparently. Then, the justification and effectiveness of these frameworks are demonstrated through comparative analysis with detailed simulations. Furthermore, harmonic stability requirements for each AC/DC converter station are introduced, along with a proposed standalone methodology for compliance evaluation.

Finally, a list of functional requirements is provided including the following functions: Element status analysis, System topology analysis, Element limitation analysis, DC power flow optimization, Secondary DC voltage control, Ramp rate coordination, Offshore power curtailment, Control mode management, primary DC voltage control related modes.

DC grid protection

The protection of DC systems should follow the same objectives as in AC systems: Ensuring a reliable and secure HVDC system operation during contingencies including DC faults and component failures. In a large scale HVDC system the shutdown of the entire system is not compliant with power system criteria which imposes a limited impact for a single event. This implies a need for fault separation in the HVDC system. The fault separation zones on the DC side need to be defined such that the maximum loss of power of surrounding AC grids is respected. AC/DC Converter stations outside of the fault separation zone shall ensure post fault active power recovery. The DC-Fault Ride Through (DC-FRT) capability of converters shall be specified such that any unexpected disconnection of the converters from the grid is avoided.

The functional group DC grid protection defines the system states (normal, alert, emergency, blackout) and associates them to ordinary and extraordinary contingencies. Requirements for fault detection and fault current suppression are defined on DC switching station level and a DC-FRT profile for AC/DC converter stations is defined with the objective of a clear functional split between AC/DC converter station and DC switching station.

The DC-FRT profile ensures that the AC/DC converter station has sufficient withstand capability to ride through a DC fault while the primary or backup protection operates avoiding any unplanned disconnection. The functional group DC grid protection has investigated different ways to define DC-FRT requirements, mainly distinguishing between a generic and design-based approach and between DC voltage and DC current profiles. To leave freedom to the vendors for different converter design strategies, only a DC-FRT profile based on DC voltage quantities is defined, and no overcurrent capabilities are prescribed. The actual fault current level in the converter is left unspecified and then depends on the design strategy of the converter's vendor. The definition and evaluation of alternative DC-FRT profiles is provided in the appendix section. In the new version, preliminary standalone compliance tests have been developed for converters with regards to the DC-FRT requirement and for DCSS with regards to the fault separation requirement. A key investigation has been carried out to ensure that the protection related requirements have been defined well enough and that it is verifiable and applicable at the DC-PoC of the subsystems. System studies have been carried out to verify satisfying system level behaviour with regards to pre-defined key performance indicators. A second key investigation allows evaluation of how wind farms behave during temporary blocking of the offshore converters, thus investigating islanding mode operation.

Finally, a list of functional requirements is provided including the following functions: DC-FRT (connection requirement, operational requirement), Fault separation, Fault isolation, Fault current withstand, Fault detection/discrimination (fault separation & fault isolation), Tele-communication, Protective auto-reclosing, Monitoring.

3. Introduction

This deliverable is listing basic functional requirements for the building blocks of multi-vendor HVDC grids ensuring interoperability by design.

The building blocks of HVDC grids include the following subsystems: AC/DC converter stations; DC switching stations; coordinated DC grid control; power park modules connected to the offshore AC system. Functional requirements are defined for a bipolar configuration with Dedicated Metallic Return (DMR) as a full set while considering rigid bipolar and asymmetrical monopolar configurations covered as sub-sets. It should be noted that requirements for symmetrical monopolar configurations may not be fully represented in this deliverable.

The main functions of a multi-vendor HVDC grids (continuous control, sequential control, DC grid protection) have been analysed, divided and assigned to the subsystems. This leads to the definition of basic functional requirements for each subsystem. Those basic functional requirements are defined to be verifiable at subsystem level with standalone compliance tests and dedicated simple models.

Interoperability by design is a success if the standalone compliance of individual subsystems is enough to ensure the desired integrated DC grid system performance and behaviour.

Interoperability will be tested through the Demonstrator of InterOPERA. The integration tests and interaction studies may lead to the discovery of interoperability issues. Solving those issues should ideally be possible through a refinement of the subsystems' basic functional requirements. This learning process will reinforce the basic functional requirements and their capability to ensure interoperability by design.

Some control and protection functions belong to the grid level and others at subsystem or component level. Functions at subsystem-level, implemented by several different vendors, are the most susceptible to cause adverse interactions. Therefore, in this current version of this deliverable, special attention has been paid to the formulation of functional requirements at subsystem level and at the DC points of connection. For grid operation functions, it was first assumed that there is only one instance of grid-level operation in the system, so they are less prone to adverse interactions. This second version of the deliverable further elaborates on distributed architectures for this control layer, in a multi-operator context.

Functional requirements shall be described in a technology agnostic and purpose-oriented way. The basic functional requirements are intended to open the market for different technical solutions and to foster innovation while addressing and fulfilling the relevant requirements for a stable MT MV HVDC network. Any restrictions are to be justified by technical efficiency gains. Functional requirements shall be formulated in a generic manner and as independent from a specific design or topology as possible. The basic functional requirements are still subject to screening for identification of patents that may relate to them. The evaluation of patent relevance or essentiality will then be organized. This may lead to revisit the functional requirements or to include a reference to a patented item, granted that the right licensing conditions are secured.: Section 4 describes the aggregation of the subsystems by defining the terminology, boundaries and interfaces. Sections 5-7 define functional requirements and provide reasoning for different functional groups. The section 5 provides an overview of global and local sequences in an HVDC system. In this context states of subsystems, transitions and relevant communication interfaces are defined. The section 6 provides an overview on functional requirements related to continuous control. In the first part, a clarification on different functional levels and responsibilities is provided by distinguishing between operational level, converter station-level and converter unit level. In the second part, main sections deal with static and dynamic control concepts and define relevant functional requirements. Section 7 provides an overview on functional requirements related to DC grid protection. In the first part, a relation between system states and DC grid contingencies is defined leading to DC grid protection coordination requirements. The second part focusses on DC-Fault Ride Through (FRT) requirements for converter stations on the one hand and fault separation requirements on the other hand. At the end of each section a list of functional requirements and associated parameters are provided.

Deliverable 2.1 consists of two versions. This first version describes the functional framework and basic functional requirements for the HVDC system and subsystems. In the second version a functional framework for insulation coordination in a MTDC context and system grounding has been added.

Additionally, in the second version some central functional requirements have been investigated based on technical studies to ensure that they are well defined, applicable and verifiable based on the methodology shown in **FIGURE 1**. First, the initial list of functional requirements has been assessed and prioritized. Requirements susceptible to lead to interoperability issues such as DC-FRT or dynamic control requirements have been selected for further investigation. In the second step possibilities to verify the prescribed requirements have been assessed. First definitions of standalone tests, DC grid equivalents and compliance evaluation criteria are formulated which need to be respected by the device under test (DUT). The functional requirements together with the standalone tests open up a design space for the subsystems in which different technical solutions are compliant. Finally, compliant subsystems are tested in a MTDC context based on pre-defined key performance indicators (KPIs). The system level verification is used to verify against interoperability (IOP) issues. Learnings from subsystem standalone compliance tests and performance verification at HVDC system level are used to refine the functional requirements if necessary. **TABLE 1** provides a list of added or modified versions in version 2 compared to version 1 of deliverable 2.1.

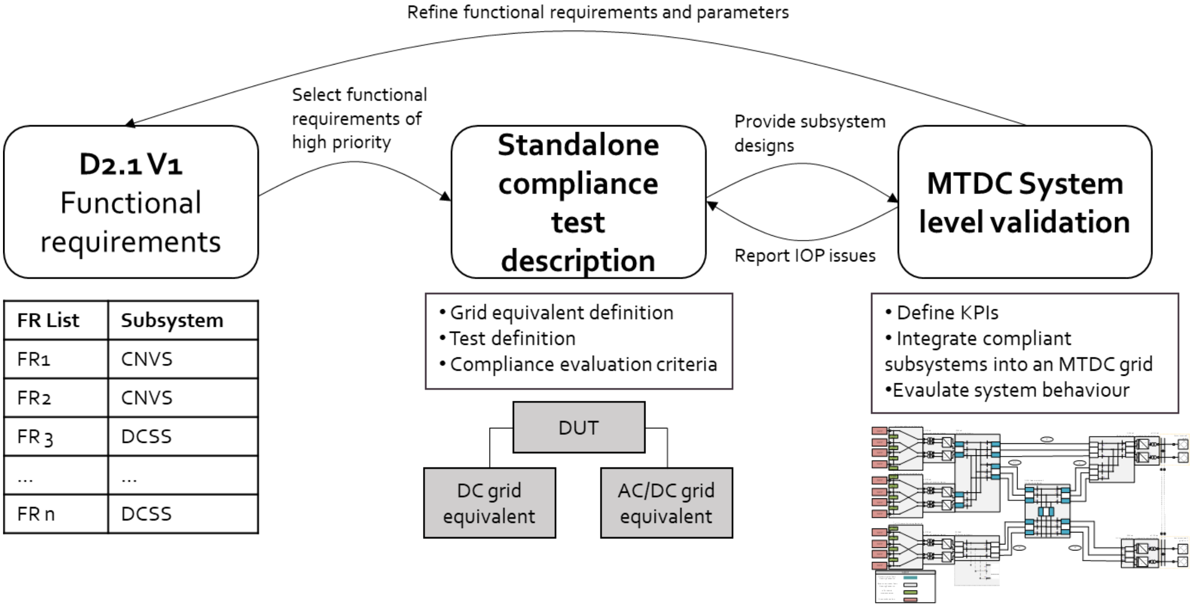

FIGURE 1 Methodology from version 1 to version 2: Investigate definition, applicability and verifiability of functional requirements and dedicated parameters for HVDC subsystems (i.e. DC switching station (DCSS), converter station (CNVS))

TABLE 1 List of modified or added sub-sections in version 2 compared to version 1

Section	Title
4.8	DC grid controller
6.5.4	Necessary considerations for dynamic requirements of primary DC voltage control
6.6	Performance requirements and recommendation of behavioral specification procedure
7.3.6	DC-FRT requirements of converters
7.4.3	Compliance test for DC fault separation
7.5	Coordination between DC-FRT and fault separation requirements
7.6	Insulation coordination
7.7	DC system grounding
9.5	Example for application and verification of dynamic performance requirements
9.6	Example for application and verification of harmonic stability performance requirements
9.8	Example for application and verification of protection requirements
9.9	Temporary blocking offshore
9.10	DC grid control architecture in multi-TSO context (added in version 3)

4. Functional subsystem definition

In this section, the aggregation of subsystems in a multi-terminal HVDC system are defined such that connection requirements can be assigned at the DC-Point of Connection in an independent and verifiable way while ensuring a clear split of interfaces and functional responsibilities[1]. The following functional levels are defined.

HVDC system

Means an electrical power system which transfers energy in the form of high-voltage direct current between two or more alternating current (AC) buses and comprises at least two HVDC converter stations with DC transmission lines or cables between the HVDC converter stations.

DC grid control layer (DCGC)

Represents an interface for getting information on the power flow conditions and accessing all electrical nodes in the HVDC grid. It continuously receives and transmits status and command messages to and from any high voltage equipment necessary for HVDC power transmission. Based on this information, the HVDC grid control provides modifications on the dispatched converter schedules in order to properly respond to changing external conditions according to desired optimization targets.

DC switching station (DCSS)

Part of an HVDC system with the primary purpose to establish electrical connections between functional elements in the HVDC system. It is composed of:

- **Switching unit:** Set of all switchgears that ensures the connection between one external unit (transmission or converter) and a busbar of the switching station [1]. Some switching units may also ensure connection between busbars of the same switching station. The switching unit corresponds to an aggregation of all switchgear for a given pole, and a given feeder. A switching unit comprises both the primary equipment, as well as the secondary equipment needed for automation and monitoring of the switchgear including fault detection and discrimination functions. Switching unit may comprise fault separation device (FSD) or not.
- **Busbar unit:** Including secondary equipment for busbar related fault detection and discrimination functions.
- **Grounding unit:** The grounding unit is located in the DC switching station. It is a passive device ensuring the system grounding which is configured by a switching unit.
- Measurement device required for the automation of the switching unit and switching station control.

AC/DC converter station

[1] Disclaimer: It should be noted that no techno-economical assessment has been made which might, for individual functionalities and subsystem aggregations, come with a certain cost of oversizing or redundancy.

Part of an HVDC system which consists of one or more HVDC converter units installed in a single location together with transformers, reactors, filters, reactive power devices, control, monitoring, protective, measuring and auxiliary equipment. While system relevant switching functions are located in DC switching stations, switchgear required for the self-protection may still be part of the converter station. This in particular includes ACCB and NBS.

- **Converter units**[2]: An AC/DC converter unit is a power exchange device with the ability to transfer power from/to an AC network from/to a DC network. It is defined per pole on the DC side, so that a bipolar converter station comprises two converter units with opposite polarity. It comprises switching, earthing and protective devices relevant for the internal functioning of the converter. Switching capabilities that are relevant for the entire HVDC system are however not part of the converter unit. A Converter unit would typically comprise an AC circuit breaker for self-protection whereas DC fault separation device would be part of DCSS. Additional AC switchgears relevant for system operation would be part of AC switching stations, and not converter stations.

Transmission line

- **Transmission units**: A transmission unit is passive component with the ability to transmit DC current, assuming it is connected on both sides. The capability of a transmission unit to earth itself, *e.g.*, for maintenance purposes is delegated to a neighbouring switching unit. Transmission units are defined per pole (HV poles, medium voltage pole/DMR) and may be grouped to form a transmission line.

Energy absorber

Devices to absorb dynamically excessive energy in case of contingency scenarios to limit overvoltage within the HVDC system. Typically, these devices are triggered by over-voltage conditions arising from such contingencies.

FIGURE 2 provides an overview on the functional aggregation of the subsystems (primary equipment) with a focus on DC grid components and relevant AC components in direct relation with the HVDC system such as Power Park Modules (PPM) at the AC side offshore and AC switchyards.

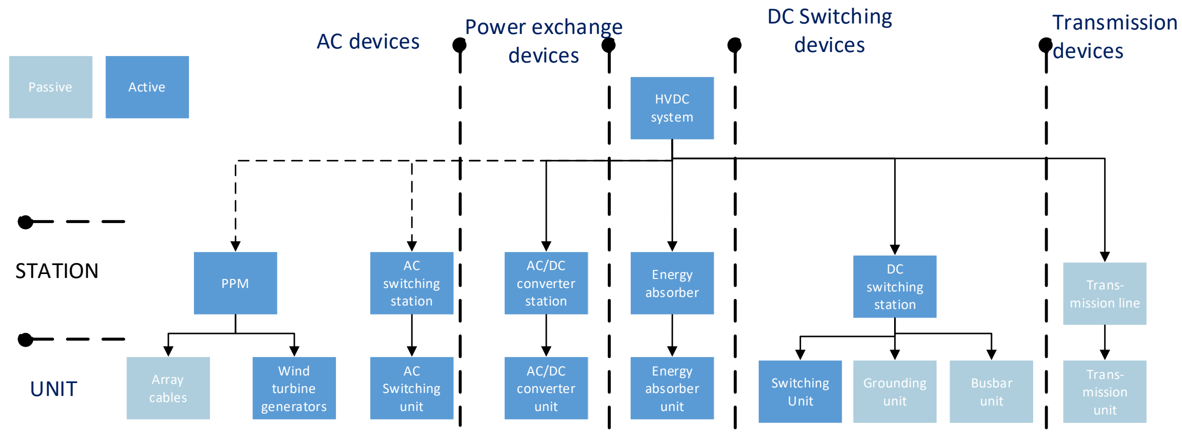

FIGURE 2: Functional aggregation of subsystems and sub-units related to an HVDC system with focus on primary equipment

[2] The proposed definition follows and further specifies the one from COMMISSION REGULATION (EU) 2016/1447: "means a unit comprising one or more converter bridges, together with one or more converter transformers, reactors, converter unit control equipment, essential protective and switching devices and auxiliaries, if any, used for the conversion."

4.1 DC switching station

The primary purpose of a DC Switching Station (DCSS) is to establish electrical connections between functional elements in the HVDC system. Therefore, the functional aggregation is such that all DC switchgear with system functionalities is located in the DCSS including fault separation devices (FSD). Sub-units of a DC switching station are DC busbars (passive), earthing unit and switching unit (see **FIGURE 4**).

A switching unit is the functional block that contains all switching functions associated to one point of connection of the DC switching station. This point of connection can be for example towards a transmission unit or towards a converter unit. In case the DC switching station comprises only two points of connection per pole, a switching unit may directly link these two points of connection. Otherwise, the switching unit typically connect the point of connection to a busbar. A switching unit can for instance connect a busbar (per pole) and a transmission unit, or a converter unit (per pole) and a busbar. It is intended that all switching functions relevant for DC system level operations, and hence all switching units, are hosted in DC switching stations[3]. Note that the number and capabilities of the different switchgears comprises in a switching unit will vary from one switching unit to another, depending on the individual functional requirements that are assigned to the specific switching unit. The individual switchgear shall be designed such that all functional are satisfied.

An illustrative functional single line diagram of a switching unit connecting two units (unit A and unit B) at high voltage level is provided in **FIGURE 3**. The switchgear of a switching unit depends on the desired functionalities. In addition, different switching functions (e.g. fault/load current interruption or energization) and fault detection functions (e.g. for different fault types, primary/backup protection) could be embedded in a single device. The realisation of the function and the aggregation of switchgear is subject to the vendor as long as the functional requirements associated to the switching unit are fulfilled. The possibility of the switching unit to have access to the earth is represented (for instance to discharge unit A or unit B). It should be noted that a switching unit may have more than two connection points (i.e. a third internal connection to a low voltage connection point).

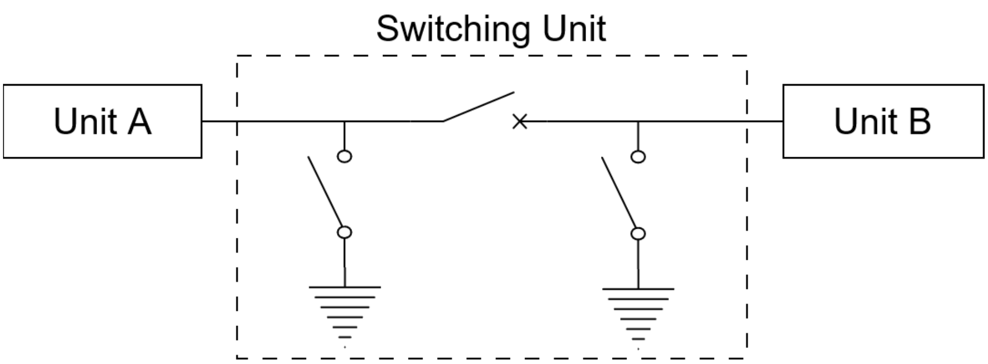

FIGURE 3: Exemplary functional diagram of a switching unit connecting two other units (e.g., converter unit, transmission unit...). The circuit breaker symbol is indicative only as not all switching units may have fault separation capabilities. The switching unit may have access to earth itself for maintenance purposes, or to earth the neighbouring unit (A or B) if they are passive ones, such as cables.

[3] A disconnected converter station may still have a local earthing point to respond to AC side statcom requirements. It should be noted that this is an exception which is not considered as a DC system level function.

A switching unit having two connection points, assuming it is not earthed, can either be in open or closed state. An earthed state can be introduced for maintenance purposes.

The functional behavior of a switching unit for a close and open commands is further specified in section 5 in flowchart diagrams. While the close/open commands are always initiated outside the switching unit (e.g. by operator, DC grid controller, protection relay), the remaining of the sequence is executed based on local information only. In fact, the switching unit consists not only of primary equipment (DC switchgear and hardware components) but also of secondary equipment (automation, measurements, monitoring) in order to execute open and close commands based on local information[4].

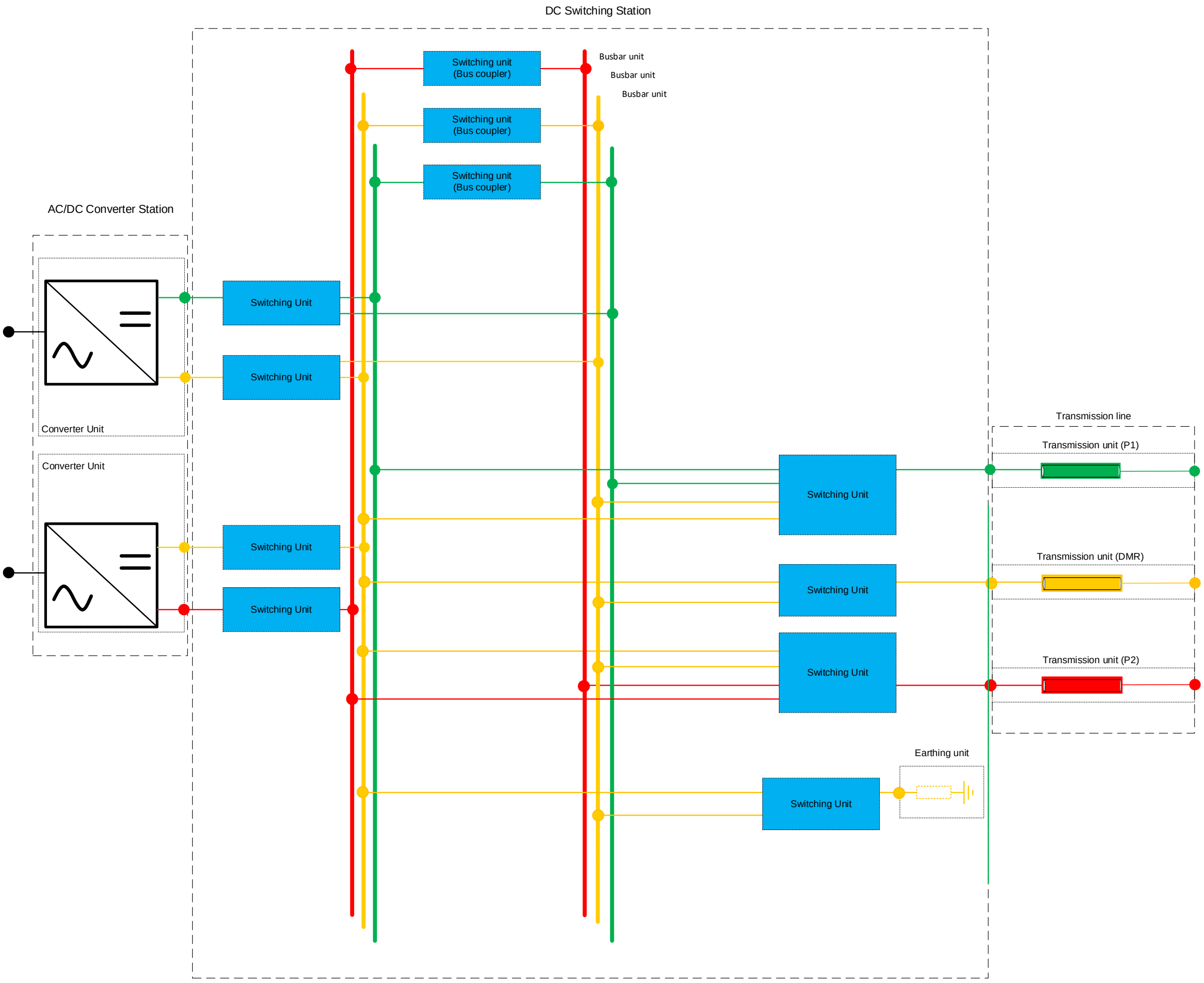

FIGURE 4: Example of a switching station layout connecting one converter station to one transmission line. The station includes two busbars connected by switching units (bus couplers) and an earth reference connected to the neutral busbar through a switching unit. Other layouts are possible such as having a single switching unit connecting the two neutral point of the two converter units.

[4] It should be noted that some secondary equipment and automation functions for coordinated switching unit operations inside a DCSS can be located at central automation level of the DCSS.

4.2 AC/DC converter station

The primary purpose of the AC/DC converter station is to exchange power between the AC grid and the DC grid. Considering this, primarily control functions are assigned to the AC/DC converter stations, whereas AC and DC switching functions are assigned respectively to the AC switchyard and the DCSS with the exception of internal switchgears for self-protection and local earthing of the converter. This in particular includes ACCB and NBS.

4.3 Energy absorber

The primary purpose of the energy absorber is to absorb dynamically excessive energy in case of contingency scenarios to limit overvoltage within the HVDC system. Typically, these devices are triggered by over-voltage conditions arising from such contingencies. The Energy absorber is considered as a separate subsystem because of its functional independence to the AC/DC converter station or the DCSS. Due to the functional independence the physical placement is not limited to close vicinity of the AC/DC converter station.

4.4 AC switching station

All AC switching elements are placed in the AC switching station. Physically, they are part of the AC grid. However, some functionalities are also relevant for the protection or coordination of the DC grid. From a functional perspective they can be activated due to both DC and AC events. It should be noted that in case of activation due DC contingencies, the AC Circuit Breaker can be activated by protection relays located at the DC side or by AC/DC converter stations according to the DC-FRT definition. More information is provided in section 7. Note that a detailed functional description of the AC switching station is not in the scope of this deliverable.

4.5 Power Park Modules

The PPMs are power generating modules consisting of multiple wind turbines, which are power park units connected to the AC offshore grid. Due to the direct connection to offshore converters they are functionally related to the HVDC system and may have direct or indirect control and communication interfaces with the DCGC or other DC grid subsystems. For instance, in case of a DC contingency depleting power export reserves, wind turbine curtailment needs to be coordinated throughout offshore connection points and PPMs.

4.6 DC Point of Connection (DC-PoC)

DC-Point Of Connection (DC-PoC) means a point at which HVDC equipment is connected on the DC side, at which technical specifications affecting the performance of the equipment can be prescribed. The -DC-PoC should be accessible for converter stations and other subsystems to ensure and verify conform operation. Voltage and current measurements shall be accessible without telecommunication. **FIGURE 5** provides an overview on the DC-PoC for the AC/DC converter station and for the DCSS. It should be noted that the AC/DC converter station is connected to an AC-PoC and a DC-PoC, whereas the DCSS is connected to at least two DC-PoCs.[5]

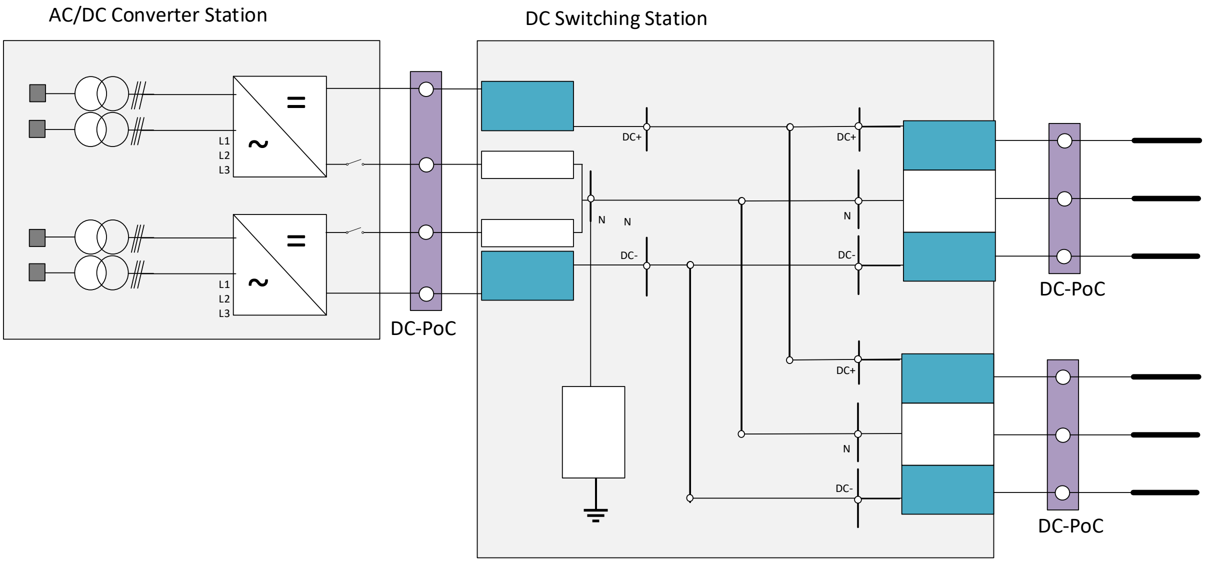

FIGURE 5 Indication of DC- Point of Connection (DC-PoC) for AC/DC converter station and DC switching station

4.7 AC-Point of connection (AC-PoC)

'**Connection point**' means the AC interface at a synchronous area at which the power-generating module, demand facility, distribution system or HVDC system is connected to a transmission system, offshore network, distribution system, including closed distribution systems, or HVDC system, as identified in the connection agreement. The connection point is also typically referred to as the point of connection (PoC) [2].

4.8 DC grid controller

The DC grid controller refers to the layer that handles coordinated functions across the HVDC system. It comprises both continuous control such as computing setpoints, sequential control and monitoring functionalities. It is interfaced with the AC/DC grid control layer, and with the HVDC subsystems, in particular the converter stations, DC switching stations, and possibly PPM.

[5] The definition of DC-PoC is subject to the subsystem's ownership. Therefore, the exact electrical interface is to be defined in detail on project level by the HVDC system owner, in coordination with the relevant system operator, subject to the relevant connection agreement.

5. Sequential Control

Within a given HVDC system topology, different DC connection modes are possible. The DC connection modes describe the connection between the individual units within the HVDC system at their DC-PoC. Those connection modes are determined by the individual states of all the switching devices within the grid. Given the large number of such devices, all connection modes may hardly be described exhaustively in a synthetic way such that "bipole" or "asymmetric monopole". The sequential control describes all planned actions that allow the HVDC system to go from one connection mode to another. Such actions may be triggered automatically, or by an operator, or a combination of both. Change of connection modes after protection action, *e.g.*, line disconnection, are not seen as sequential control actions but rather as protection actions.

On one hand, the handling of large number aggregated connection modes on a multiterminal HVDC system level is not practical, due to the very large number of possible combinations. On the other hand, the control of each individual switch by an operator or DC grid controller is also unsuitable. As such, the main purpose of this workstream is to define the appropriate granularity to describe the switching devices within the grid. It is proposed that the set of switches connecting two DC units (i.e. for one pole) is a relevant aggregated level, called a switching unit. A switching unit may hence connect a converter unit to a busbar (per pole), a busbar to the ground, a HV conductor to a busbar, etc. While some switching units may have many more capabilities than others, they can all be described as a state machine[6] being open or closed. The opening and closing of switching units will induce changes in other units throughout the grid, for instance the energization of converter or transmission units. The concepts defined in this section significantly differ from the ones introduced in [3], where an aggregation per feeder is adopted. As already introduced in Section 4, all switchgears relevant for the HVDC system operation have also been grouped in the switching station, whereas they may be part of converter stations in [3]. Those two modifications are deemed to facilitate interoperability and compatibility between the different functional sub-systems, as well as between HVDC systems with different topologies (bipolar with and without metallic return and asymmetric monopole).

An overview of the control structure for sequential control is first presented in Section 5.1.The main units constituting an HVDC grid and their states are then defined in Section 5.2. A functional definition of a switching unit is provided in Section 5.3, including the transition from closed to open and from open to closed.

5.1 Control structure for sequential control

An overview of the control hierarchy for sequential control of an HVDC system is depicted in **FIGURE 6**. For sequential control purposes, the change of states of the units within the HVDC system or a network of HVDC stations and switching stations connected on DC side may be directly controlled by a DC grid controller, or similarly may be directly controlled by a national dispatch centre where software with similar

[6] A state machine is a model defined by a finite number of states, its initial state, and the inputs that trigger each transition between two states.

functionality exists. If necessary, local control of switchgear at the switching station level shall be possible. States of the HVDC system or a network of AC/DC converter stations and switching stations may also be controlled more locally for other purposes (*e.g.*, protection). In the context of sequential control, the functionality of the DC grid controller or relevant software being part of the TSOs national dispatch centre may be:

- To propose operational simplification of default scenarios for planned reconfiguration. While the exhaustive description of all connection modes of the grid and the transition between them shall be defined by the relevant TSO in coordination with adjacent TSOs (if applicable) the macro-sequence that allows to perform planned reconfiguration actions can still be coordinated by the DC grid controller. Such usual actions for instance include: start-up and shut-down of the DC network, connection or disconnection of a transmission line, or of a converter, and change of the system earthing point location. The proposed macro-sequences can then be activated step-by-step by an operator, or automatically. In all cases, the abortion of the sequence must be possible.
- To be able to respond to unscheduled events[7], when required. Unscheduled events such as faults are primarily handled by protection, ensuring the security of the HVDC system or the network of HVDC converters stations. Sequential control actions can then be performed to improve the reliability of the power system. Such actions may be included in the DC grid controller as "operational simplification" as described above, or may be triggered automatically and locally if a faster action is beneficial. Examples of unscheduled events that may benefit from automatic reconfigurations are:
- Recovery procedure after fault isolation in order to reconnect the part of the fault separation zone that is healthy. Such a reconfiguration may also be performed locally as an auto-reclosing attempt, known as "protective auto-reclosing".
- Busbar reconfiguration after a busbar fault, for instance in case of double busbar single breaker scheme.

For any of such sequences, the commands will consist of open and close commands sent to switching units. For convenience, such commands would be sent to the switching station automation, which will in turn re-dispatch them to the switching units. However, the switching station has not been identified as a relevant functional level for sequential control and may hence only pass the open and close commands to the appropriate switching unit. In return, the switching units report their status to the DC grid controller, through the switching station. In addition, a switching station may implement interlocks between switching units to prevent non-suitable switching operation (*e.g.*, closing onto an earthed unit, or controlling an out of service unit). The DCSS will only issue a command to the switching unit if necessary, interlock checks are satisfied.

As depicted in **FIGURE 6**, all interfaces for sequential control are deemed vertical. No horizontal communication between different switching units, converter units, or switching stations and converter stations are envisaged. Exceptions to this principle may be considered, if functionally required. If needed, the DCGC can act as a communication bus to provide information to the relevant unit. However, this approach would unlikely satisfy ultra-fast communication needs. In sequential control, no such functionalities requiring fast horizontal communication have been identified yet.

Other functional devices may be present in switching stations, in particular protection relays for protection purposes.

[7] In the context of sequential control, unscheduled event refers to any fault that may affect the HVDC system. It also comprises any opening or closing of switchgear that does not follow from the appropriate command, such as a spurious trip.

Beyond sequential control, many reconfigurations of the grid would also involve continuous control actions, for instance for the dispatch of new power flow references. Such actions may be part of the planned connection / disconnection of a converter or transmission unit or can also be used in a post-fault recovery process.

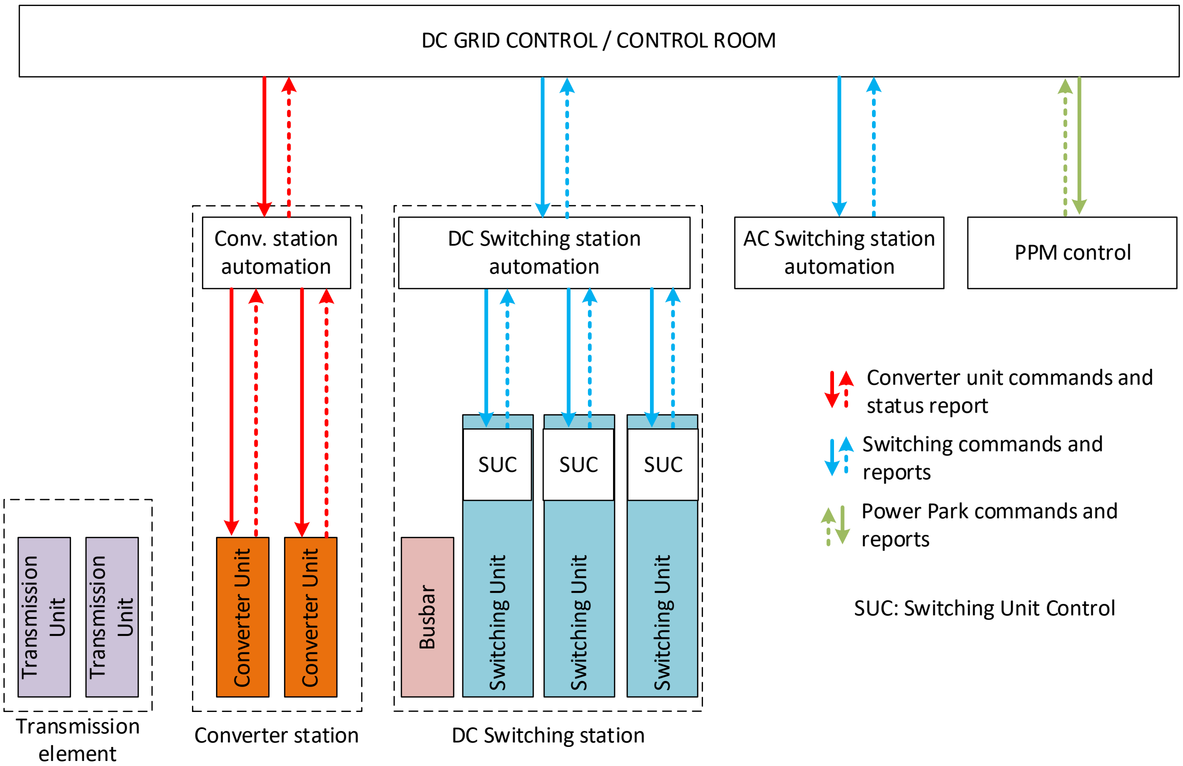

FIGURE 6: Sequential control architecture of an HVDC system: channels between the DC grid controller and the converter or switching stations are an aggregation of the commands sent to the unit layer. Interactions with AC side equipment such as PPM and AC switchyard are also included, though not detailed in this chapter. Note that relays can also be included in switching stations, controlling one or multiple switching units for protection purposes, see Section 7.4 for further details.

5.2 Interface and state of the main units

This section provides the main interfaces for the sequential control of the units within an HVDC system. Based on those interfaces, state diagrams are proposed to illustrate the behaviour of the units. In [3], state representation based on a three-pole aggregation (2 HV poles and neutral) is proposed, linking "connection modes" of the AC/DC converter stations (bipole, monopole…) with the ones of the switching station. By contrast, the functional scope split presented in Section 4 leads to a single pole (HV or neutral) description of the connection states within the system. The proposed approach allows a clear definition of the behaviour of the functional units of the grid, without the complexity of states of combined units that would depend on specific topologies and configurations.

5.2.1 Switching station

As discussed in Section 5.1, the switching station is not deemed a relevant functional layer for sequential control. Its main role is to transmit commands from the upper layer (e.g. DC Grid Control) to switching units, and to report feedback the other way around. In addition, it may implement interlocks between switching units to prevent unsecure switching operations, such as closing onto an earthed subsystem. An overview of the switching station interfaces is provided in **TABLE 2**.

TABLE 2: Interface of the DC Switching Station with DCGC and DC Switching Units

Top layer interface : Between DC grid control and DC switching stations	
From DCGC to DCSS	Commands for switching units: open, close, discharge (if applicable), auto-reclose attempt enabled (if applicable), maintenance & earthing (if applicable).
From DCSS to DCCG	- Feedback on switching unit status (open, closed, maintenance…) - Continuous measurements (V, I) - Failure of switching unit functionality (e.g. FSD function unavailable) - Protection information: fault zone (from protection relay), and trip command issued
Bottom layer interface: Between DC switching stations and switching units	
From DCSS to Switching Unit	Commands for switching units: open, close, discharge (if applicable), auto-reclose attempt enabled (if applicable), maintenance & earthing (if applicable).
From Switching Unit to DCSS	- Feedback on switching unit status (open, closed, maintenance) - Continuous measurements (V, I) - Failure of switching unit functionality (e.g. FSD function unavailable) - Trip report (following trip issued from protection relay)

5.2.2 Switching unit

A switching unit is defined as the switchgear that forms a connection path per pole between two units. A functional view of a switching unit connecting two other units is provided in **FIGURE 7**. It may be composed of one or more switching devices depending on the functionalities available. It is controlled by the switching unit automation which is responsible for the control of each switching device within the unit. Switching units can for instance be used

- between a HV transmission unit (cable) and a HV busbar
- between a converter unit and a HV busbar
- between a neutral transmission unit (cable) and a neutral busbar
- between a converter unit and a neutral busbar
- between a neutral busbar and the ground, to provide the ground reference for the network. Electrical components associated with the ground reference (surge arresters, resistance…) are gathered in the "grounding unit".

The main role of the switching unit is to open or close the connection path. The corresponding close and open commands are received from the DC Grid Controller for planned operation but can also be issued by IEDs for protection purposes (i.e. trip). Optional functionalities of a switching unit include the ability to discharge one of the connected units (e.g. a cable), and to attempt to auto-reclose after a trip. In addition, a switching unit can be earthed for maintenance purposes. In this state, all relevant earthing switches are closed.

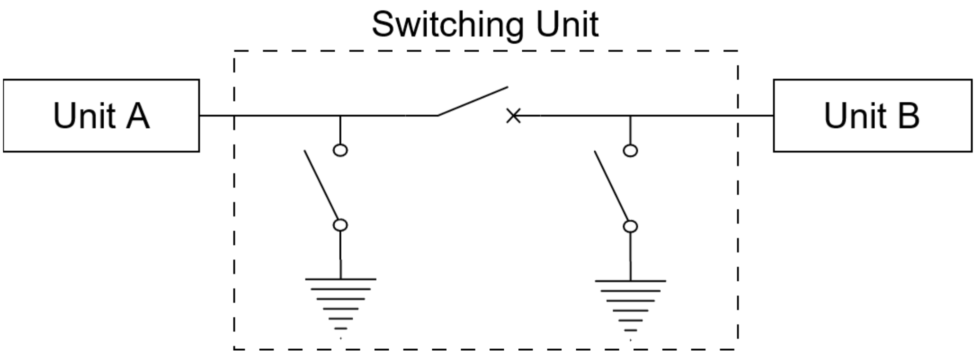

FIGURE 7 Functional view of a switching unit connecting two units. The circuit breaker symbol is indicative only as not all switching units may have fault separation capabilities.

When connecting passive units, such as busbars or cables, a switching unit can have the duty to earth those units for maintenance purposes. Though it is those passive units that are in a maintenance state, the commands are given to the switching unit. Additional commands and states are hence introduced to account for such cases. When connecting an active unit such as a converter, this maintenance functionality would typically not apply.

The interfaces of a switching unit are summarized in **TABLE 3**, and a corresponding state machine is proposed in **FIGURE 8**. In case of a failure of an internal component of the switching unit, the switching unit can be stuck in an intermediate state, which is reported to the DC grid controller (see detailed flowcharts in Sections 5.3.2 and 5.3.3 for further details).

In some cases, a switching unit may have the possibility to connect more than two units (*e.g.* a HV transmission unit may either be connected to a HV busbar, or to a MV busbar). In such cases, the close/open state shall be supplemented with the relevant units, see Section 5.3.5 for more details.

TABLE 3: Interface of the switching unit automation for sequential control. It is assumed the switching unit reports to the switching station the status of each action.

Switching Unit inputs	Short description	Mandatory/Optional
Go to maintenance	The switching unit will go to a maintenance state where all earthing switches are closed.	Mandatory
Prepare to connect	The switching unit will go from the maintenance state to the open state and is ready to close.	Mandatory
Open	The switching unit will open.	Mandatory
Close	The switching unit will close.	Mandatory
Auto-reclose	After a trip, the switching unit will attempt to auto-reclose.	Optional
Discharge transmission unit A (or B)	When open, the switching unit can discharge one of the neighbouring transmission units.	Optional

Switching Unit inputs	Short description	Mandatory/Optional
	After discharging, the switching unit remains open and the neighbouring unit (A or B) are not earthed.	
Earth transmission unit A (or B)	If open, the switching unit can provide maintenance earthing for the neighbouring transmission units.	Optional
Remove earthing of transmission unit A (or B)	Removing the connection to ground from one of the neighbouring transmission unit.	Optional

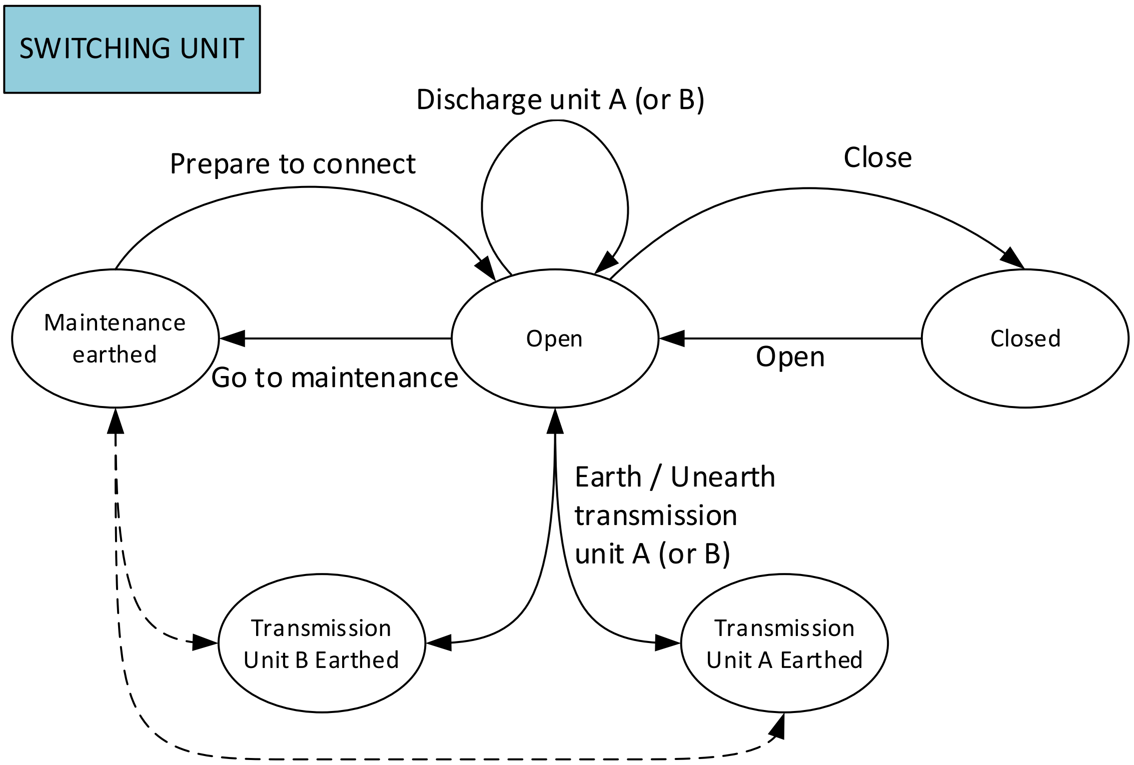

FIGURE 8: State diagram for the switching unit, including the discharge and earthing commands. Switching units have the ability of earthing neighbouring passive units (busbars or cables). It is assumed that earthing of both neighbouring transmission units is equivalent to the switching unit being earthed itself (dashed-lines).

5.2.3 Transmission unit

A transmission unit typically refers to subsea/underground cables and overhead transmission lines. A transmission unit consists of a single pole conductor, which may either be HV or MV (for neutral path). A busbar can also be considered as a special case of transmission unit, being particularly short and having typically more than two connection points. Within the HVDC System, the neutral path shall be connected to the ground to provide reference to the neutral path for the entire grid. Such reference is typically established within a switching station by the closing of a dedicated switching unit between the neutral busbar and the ground.

Transmission units are passive components and do not include any switchgear, assuming they are earthed through the neighbouring switching units when they are out of service. As such, no control interface is associated with such units. A state machine can still be established to model the behaviour of a transmission unit, but all transitions will only depend on other units within the grid. Thus, states of a transmission unit depend on the number of connected units as well as whether DC voltage has been established:

- It is considered the “ready to connect” state assumes residual voltage has been reached. It is thus mandatory when going from “Energized” to “ready to connect” to use the “open & discharge” command of the switching unit. In “ready to connect”, all earthing switches are open.
- After the closing of a single DC switching unit, the transmission unit is connected to another DC unit but cannot transmit power. Depending on whether the connected unit is itself energized, the transmission unit may either be energized, or only connected.
- A transmission unit connected to at least two DC switching units is either “aggregated” or “ready to transmit” depending on whether the connected units are energized and also connected to other DC systems.
- A busbar can be connected to more than two DC switching units and remains in “ready to transmit” state if energized, or in “aggregated” state if not energized.

The state diagram for a DC transmission unit is pictured in **FIGURE 9**.

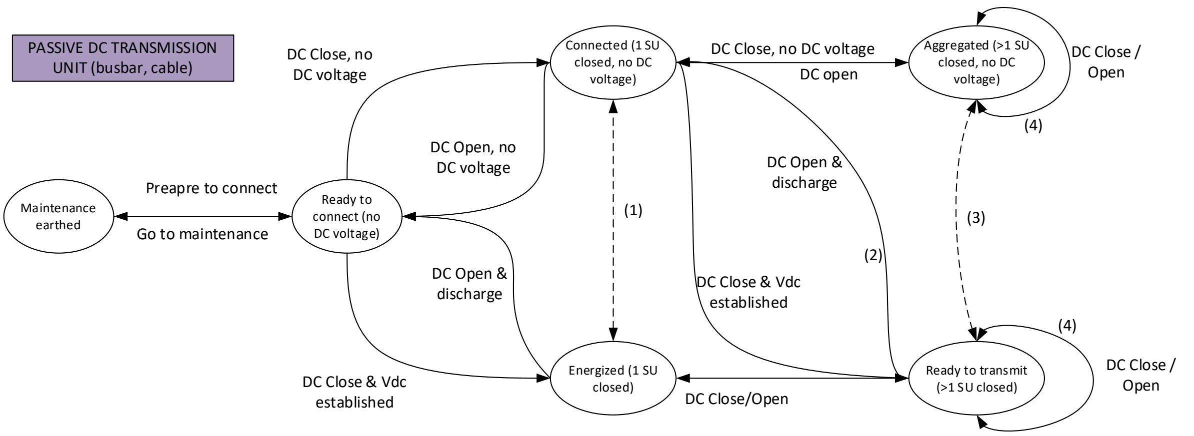

FIGURE 9: State diagram of a transmission unit. All transitions are induced by the actions of the switching units (SU) connecting the unit to the rest of the grid. States are further distinguished depending on whether DC voltage is established or not. Transitions in dashed (1) and (3) are caused by operation of remote units. The energization of multiple DC units already aggregated can for instance be due to a single unit closing. Going from “Ready to transmit” to “connected” (2) using a DC open and discharge command should be carefully considered as the remaining closed unit should not be connected to a live DC grid. For busbars, it is possible to be connected to more than two other units (4).

5.2.4 Converter station and unit

From a sequential control perspective, a converter station only consists in one converter unit (monopole) or the aggregation of two converter units of opposite polarity (bipole). Only the interfaces of the converter unit are thus further detailed. In addition to the inputs listed in **TABLE 4**, the converter unit shall report the corresponding status (*e.g.* "ready to energize") after completion of a command. Those status shall be communicated to the DC grid control or any equivalent upper layer control. It should be emphasized that the connection of the converter to the DC grid is determined by the closing of the relevant switching units, which are not part of the converter stations. Any converter unit may still include relevant switchgear for protection purposes, including an AC breaker.

TABLE 4: Sequential control interfaces of the converter unit. In addition, the converter unit reports whenever the commands have been executed.

Converter Unit inputs	Short description
Go to maintenance	The converter unit will go to a maintenance state where all earthing switches are closed. The submodules are discharging.
Prepare for energization	The converter unit will go from the maintenance state to a "ready to connect" state. The energization may either come from the AC or DC side.
Close AC side	The converter will close the ACCB within the converter area (additional ACCB can be located further on the AC switching unit).
Open AC side	The converter will open the ACCB within the converter area.
Close local earth reference	Closing of the local earthing switch to provide neutral reference. Typically used for STATCOM operation.
Open local earth reference	Opening of the local earthing switch.

The states of a converter unit depend on whether it is connected on the AC and/or DC side, as well as on the presence of voltage or not (energization). A state diagram of a converter unit is provided here in Figure 10.

The proposed states can be modified by the converter itself through the following commands:

- Prepare for energization: this step is a prerequisite to any connection to the HVDC system, and comprises multiple actions such as opening of the maintenance switches, preparation of internal controls, establishing a DC reference to ground
- Prepare for maintenance.
- AC Close and AC open, as this action controls the AC side breaker of the converter. Note that operation of more AC breakers may be required to effectively connect the converter to an AC bus.

By contrast, DC side connections are established through the closing and opening of DC Switching Units, included in DC Switching Stations and not in the converter station. As the converter may be connected to dead subsystems (so called "aggregated" state), the energization may be induced by the closing of remote units in the system.

The converter unit can either be energized from AC or DC side, leading to the "ready to STATCOM" or "ready to be islanded" modes, respectively. When connected on both sides and energized, the converter is "ready to transmit".

Closed loop controls concepts are intentionally not specified as sequential states. As such, blocked or deblocked state as well as control modes (STATCOM, islanded…) do not appear in **FIGURE 10**.

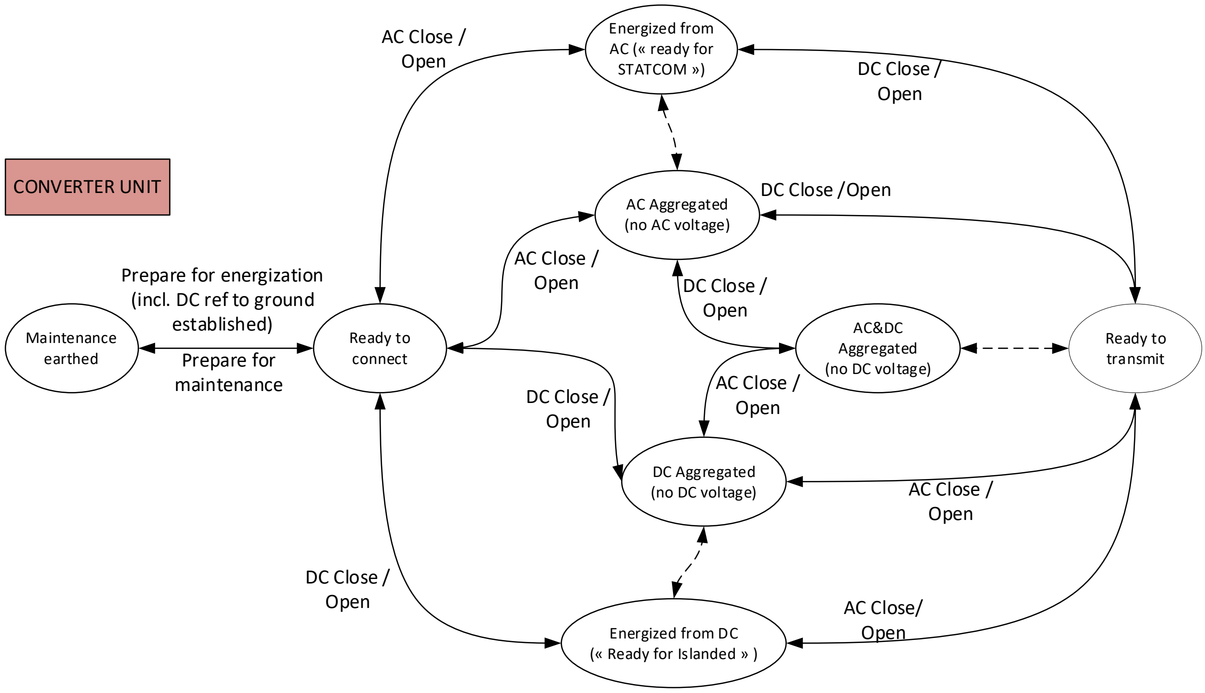

FIGURE 10: State diagram of a converter unit. Plain arrows indicate transitions due to the switching units at the PoC of the converter, while dashed arrow transition may be due to remote switching units within the grid. The only transitions handled locally at the converter unit are between "maintenance earthed" state and "ready to connect" and to open & close the AC side.

5.3 Detailed specification of the switching unit

5.3.1 Switching unit connecting two units

A **switching unit** may comprise one or more switches, depending on the desired functionalities. An exemplary overview of a switchgear arrangement is provided in **FIGURE 11** of a switching unit with full capabilities (fault separation, energization, discharge, earthing…). It is reminded a switching unit may comprise much less switchgear if less functionalities are needed. In addition, the arrangement presented in **FIGURE 11** is indicative only, and the same functionality may be satisfied with different set-ups. For instance, if it is required to bypass the entire switching unit during maintenance, all the SU switchgear shall be within disconnectors.

Those switches are further specified in **TABLE 5**, from a functional point of view. It is assumed that the residual current switch (RCS) also embeds the making current capability.

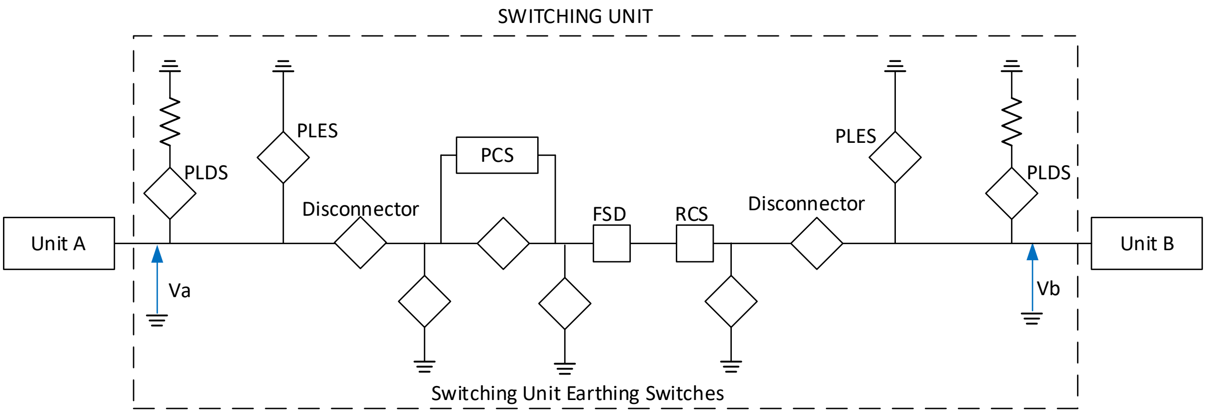

FIGURE 11: Detailed functional description of a switching unit with full capabilities. The number of switches and their arrangement is only indicative for illustration purposes. Additional energy dissipation devices can be embedded whenever relevant, in particular within the FSD or the PCS.

TABLE 5: List of devices that can be included in a switching unit.

Full name	Acronym	Functionality
Disconnectors		Switches with no current making nor interrupting capability. In the absence of an RCS, the disconnectors embed the aggregation and disconnection capabilities of the switching unit.
Residual current switch	RCS	Switch with ability to break small amount of current (typ. residual current) and with making current capability.
Fault Separation Device	FSD	Active device able to suppress fault current by producing a counter voltage. Within switching units, such devices are typically DCCB. FSD can be "activated" (fault current suppressed) or deactivated (normal onload operation). By extension, this device is able to suppress load current are denoted as FSD with smaller capabilities.
Peak Current Suppression	PCS	Component that limits the inrush current at the closing of the RCS, for instance a pre-insertion resistor (PIR). The PCS can be inserted or bypassed by controlling the relevant switches.
Pole Local Discharge Switch	PLDS	Switch connected to the earth with the ability to discharge an element (typically a cable) connected to the switching unit, after the opening of the switching unit.
Pole Local Earthing Switch	PLES	Switch to the earth to permanently earth the transmission line for maintenance.
Switching Unit Earthing Switch	SUES	Internal earthing switches for maintenance of the switching unit itself.

A switching unit having two connection points, assuming it is not earthed, can either be in open or closed state. Those two states are further specified in the table below, depending on the specific switchgear that composes the switching unit.

TABLE 6: Definition of the closed and open states for the switching unit. (*) In the specific case where a switching unit does not include an RCS, the disconnectors should be open in the open state.

State	Short description
Maintenance	All disconnectors are open, as well as residual current switches, if any. If available, fault separation devices are deactivated (e.g. DCCB are not tripped). All earthing switches are closed.
Open state	All disconnectors are closed (*). Residual current switch is open. If available, fault separation devices are deactivated (e.g. DCCB are not tripped). All earthing switches are open.
Closed state	All disconnectors are closed, as well as residual current switches, if any. If available, fault separation device and peak current suppression device are deactivated.

The functional behaviour of a switching unit for a close and open commands are further specified using flowcharts. While the close/open command are always initiated outside the switching unit (e.g. by operator, DC grid controller, protection relay), the remaining of the sequence is executed based on local information only.

5.3.2 The close command

The transition sequence for a switching unit going from open to closed state is detailed in **FIGURE 12**. The closing of a switching unit connecting two DC units may involve three different functionalities:

"Aggregation" of two units. This situation is characterized by the absence of voltage on both sides of the switching unit (first check). The use of disconnectors is sufficient to handle this function.
"Energization" of one unit through the other one. This situation is characterized by the presence of voltage on only one side of the switching unit. The inrush current resulting from the energization typically requires the activation of a PCS.
"Synchronization" of two live HVDC subsystems. This situation is characterized by the presence of voltage on both sides of the switching unit. A convergence of the voltages at the two sides of the switching unit is typically expected before the switching unit is closed (check $\Delta V < V\mathrm{sync}$). If a load current is scheduled between the two subsystems, a voltage drop between the two sides of the switching unit will be observed.

Some of the failure modes are considered, whenever a component may fail or if one of the conditions required for the proceeding of the sequence is not met (e.g., $\Delta V > V\mathrm{sync}$). Such conditions are associated to a timeout to avoid the switching unit being stuck in an intermediate step. Failure modes are handled such that, as much as possible, the switching unit gets back to a stable closed or open state. This may not be always possible however. It may for instance happen that a switching unit is closing onto a fault, or more generally onto an earthed unit. This will result in a persistent current after the closing of the RCS. Depending on the availability of an FSD at this switching unit, the switching unit may be able to get back to a stable open state or may end up in a faulty state "closed onto fault". In the latter case, it is recommended to deactivate the PCS to 1) avoid damage to the equipment, and 2) increase the current so that the abnormal behaviour can be detected and handled by other protection equipment.

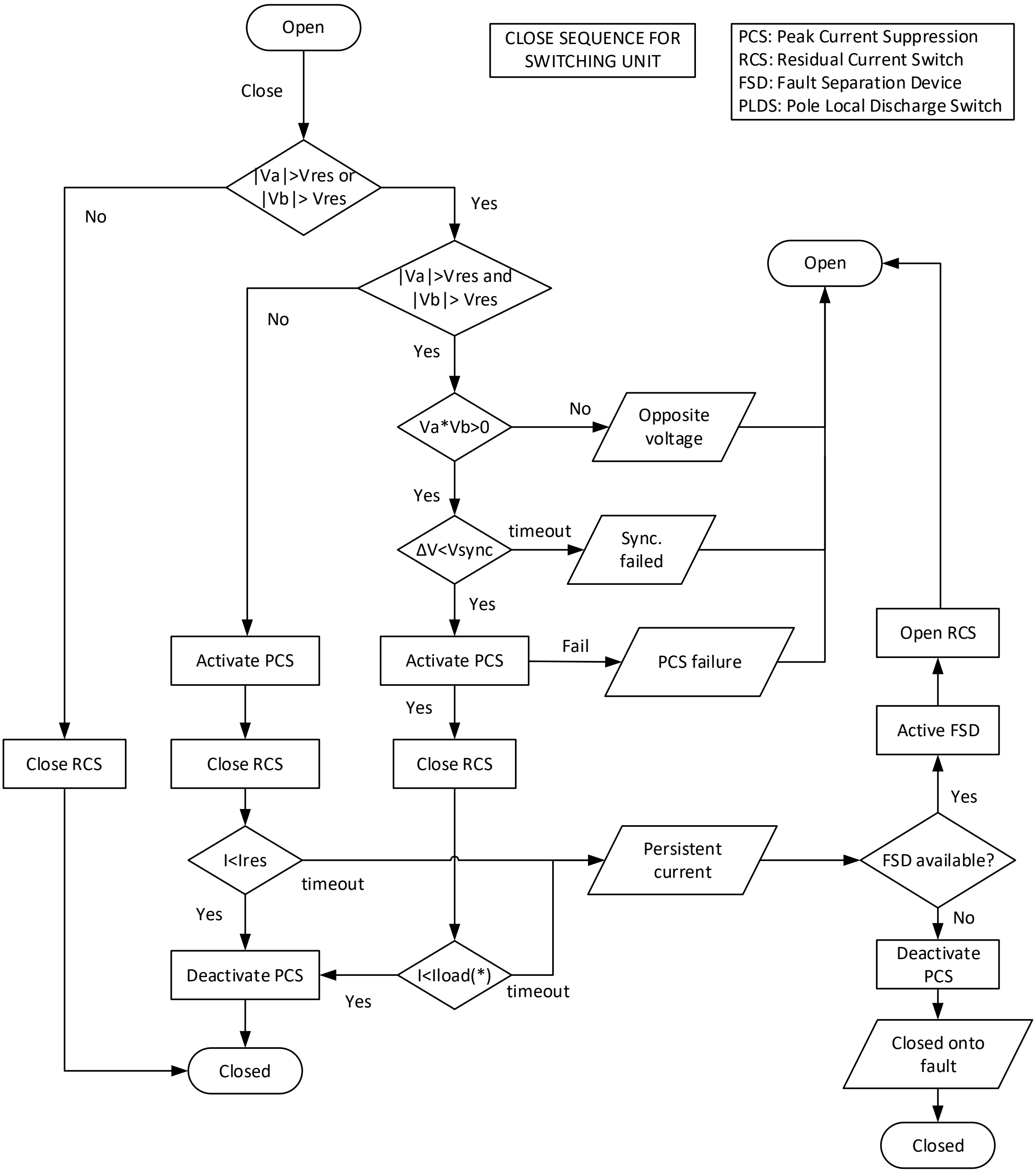

FIGURE 12: Transition sequence of a switching unit for the close command. (*)The threshold used to detect persistent current after the connection of two live sub-grids may be lower than the load current Iload.

5.3.3 The open command

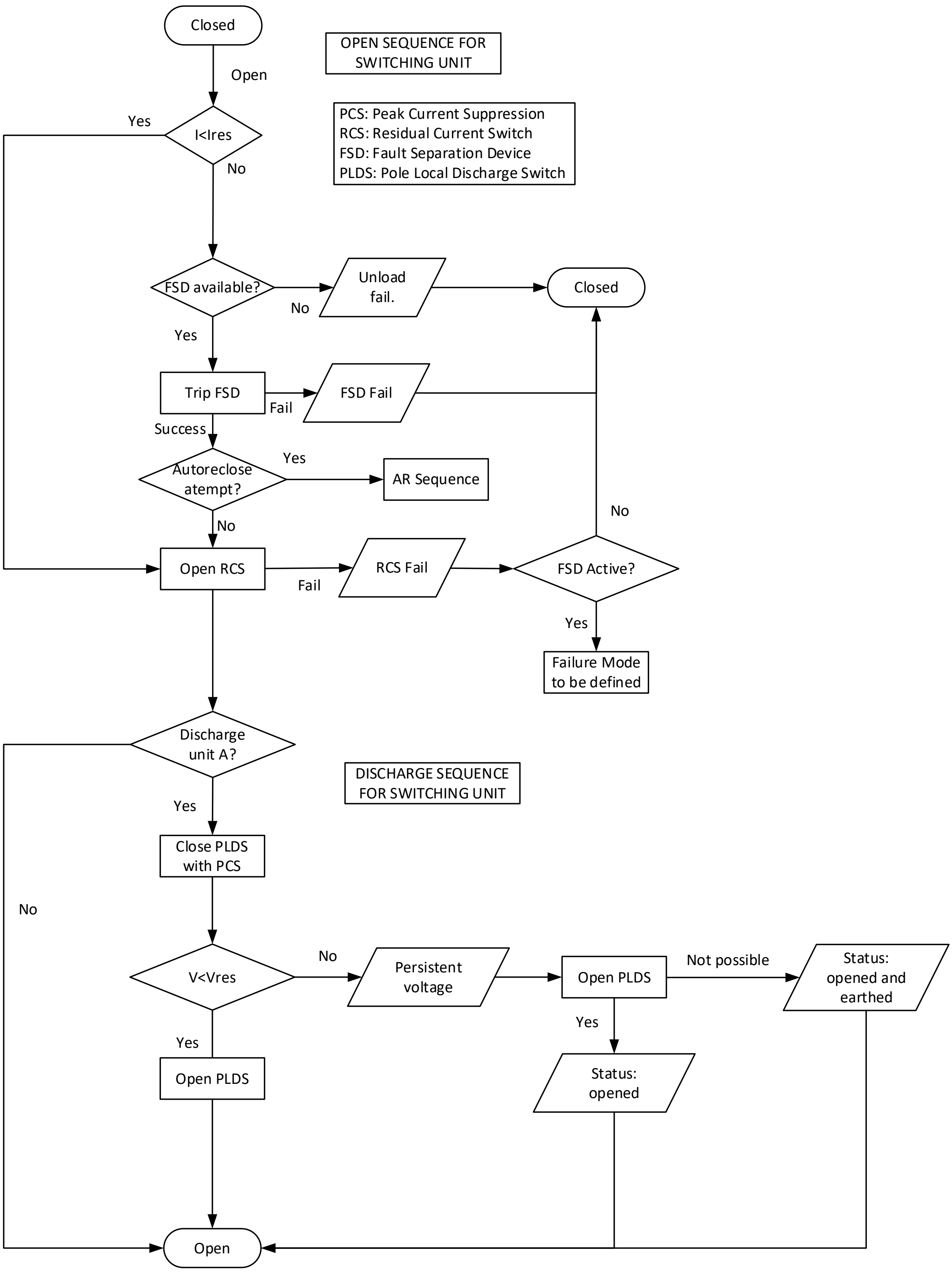

FIGURE 13: Transition sequence of a switching unit for the open command and discharge commands.

The transition sequence for a switching unit going from closed to open state is detailed in **FIGURE 13**. This transition is typically performed after the switching unit has received an open request from the switching station control. Though protection trips are typically issued by protection relays, they can functionally be described within the "open" command framework. As for the close command, the open command may involve two different functions:

- "Fault/Load separation" if the current is above residual current, in which case the activation of a FSD is required. This function may also be used to disconnect a unit with load current.
- "Fault isolation" if the current is below residual current. This function is also used to disconnect a unit with residual current only.

In a protection context, a trip command may comprise an auto-reclose request. Auto-reclosing can be performed in either an automatic way, or in a coordinated way:

- Protective auto-reclosing is considered as a protection action. It assumes that the fault has been cleared in some predefined time.
- Recovery procedure relies on the DC grid control to send the reclosing command, after the fault isolation has been confirmed.

In addition to the open command, the ability of the switching unit to discharge the unit it is disconnected from is also considered. If such an action is desired, the open command should be supplemented with the discharge command, specifying which unit should be discharged (e.g., open and discharge unit A). The discharge command does not include the permanent earthing of the unit A (or B), which is controlled by the corresponding earthing commands, as specified in **TABLE 3**.

5.3.4 Main functions of a switching unit

The specification of the behaviour of the switching unit for the close and open commands allows to identify the main functions that can be embedded in a switching unit. Those functions are defined in **TABLE 7**. Which specific functions (as well as the corresponding ratings) must be chosen for a specific switching unit is a design choice, *e.g.*, some switching units will provide only aggregation and separation functions, while others may provide synchronization and isolation functions. More complex functions may imply more basic functions, for instance a switching unit with the synchronization ability will have the energization ability, and similarly the energization function includes the aggregation function.

TABLE 7: Main functions that may be embedded in a switching unit, associated with the open and close commands.

Command	Function	Short description
Close	Aggregation	Connection of two units without significant voltage.
	Energization	Connection of one unit without voltage to a unit with established DC voltage. The inrush current during the charging shall be limited to acceptable level.
	Synchronization	Connection of two units with significant DC voltage. The inrush current during the discharge shall be limited to acceptable level. The current oscillation during synchronisation shall be sufficiently damped.
Open	Disconnection	Opening of the switching unit without significant current nor voltage.
	Separation	Opening of the switching unit under fault or load current, including suppression of the fault/load current.
	Isolation	Opening of the switching unit under residual current and isolation of the two units.
Discharge unit A (or B)	Discharge	Discharge of one of the units connected to the switching unit, after the opening. The discharge current during the discharge shall be limited to acceptable level.
Earth Unit A (or B)	Earthing	Earthing for maintenance purposes one of the units connected to the switching unit, assuming the unit has already been discharged.

The proposed function names are intended to help visualize the main use cases of the functions. It does not correspond to an exhaustive description of what the functions can be used for. For instance, "isolation" may be used in both the context of fault isolation, or in the context of a planned line disconnection.

5.3.5 Switching unit connecting more than two units

It may happen that a switching unit has the ability to connect to more than two units. In general, it is considered that a switching unit, within a switching station, can only connect to one unit external to the switching station (eg converter unit or transmission unit), but can connect to several connection points within the switching station (eg busbar).

Two examples of such cases are:

- Switching unit connecting on one side a HV transmission unit with the ability to connect on the other side either to a HV bus or to a MV bus, as depicted in **FIGURE 14**. Such a scheme allows the use of the HV transmission unit as a backup or parallel MV path.
- Switching unit connecting on one side a transmission unit with the ability to connect on the other side to two different busbars. Such a scheme allows the use of double busbar configuration.

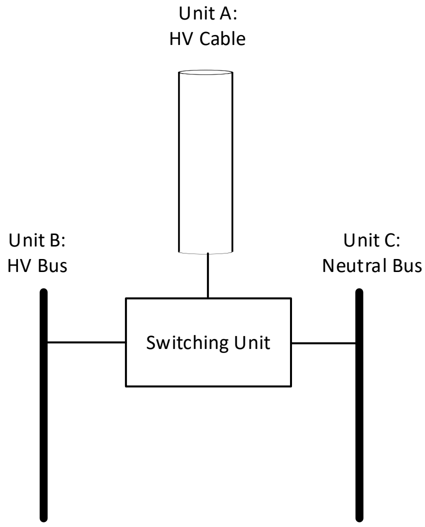

FIGURE 14: Exemplary scheme where a switching unit connect a HV cable to either a HV or a MV busbar.

For such units, the close command remains valid but shall be specified with respect to which units are to be considered. A close command shall for instance specify "close between unit A and unit B". On the opposite, the open command implies an opening with respect to all DC-PoC or only one of them.

The functional specification of such switching units should allow for different functionalities being associated to the different current paths. A connection matrix can be used to specify such functions. An exemplary connection matrix is provided in **TABLE 8**. It can be interpreted as the possible specification of a switching unit connecting a HV transmission cable (unit A), a HV busbar (unit B), and a neutral busbar (unit C). When connecting the HV path, the unit has the separation functionality, as well as the synchronization ability. By contrast, the MV current path is limited to isolation and aggregation functions. The discharge and earthing function, as it relates to a unit rather than to a connection path, is expressed on the diagonal, when included. By construction, the matrix is symmetric.

TABLE 8: Exemplary connection matrix of a switching unit connecting three units

	Unit A (e.g. HV cable)	Unit B (e.g. HV busbar)	Unit C (e.g. MV busbar)
Unit A (e.g. HV cable)	Discharge & earthing	Separation, isolation, synchronization	Isolation, Aggregation
Unit B (e.g. HV busbar)		Discharge & earthing	Not allowed
Unit C (e.g. MV busbar)			Discharge & earthing

The choice of specifying an architecture using such multi-terminal SU must be compared to a specification using multiple two-terminal SU. The latter should be preferred whenever the use of multi-terminal SU makes the design too complex.

5.4 Functional requirements & parameter list

This section provides a summary of the functional requirements related to sequential control as well as associated parameters.

TABLE 9: List of functional requirements and associated parameters for sequential control.

FR	Short description	Associated parameters	Subsystem
Command routing	A switching station shall be able to receive and redispatch commands to the appropriate switching unit.	N/A	Switching Station
Interlocking	A switching station shall be able to block commands that lead to a non-safe operation of the grid.	N/A	Switching Station
Aggregation	A switching unit shall be able to connect two units without significant current nor voltage.	No-load current and no-load voltage.	Switching unit
Energization	A switching unit may be able to connect one unit without voltage to a unit with established DC voltage while limiting the inrush current.	Maximum inrush current. Energy to be dissipated.	Switching unit
Synchronization	A switching unit may be able to connect two units with significant DC voltage while limiting the inrush current.	Maximum current Maximum voltage difference. Synchronization time.	Switching unit
Disconnection	A switching unit shall be able to disconnect two units without significant voltage nor current.	Disconnector characteristics	Switching unit
Separation	A switching unit may be able to suppress a fault or load current.	FSD characteristics, cf Protection WS	Switching unit
Isolation	A switching unit may be able to suppress of residual current and isolation of the two units.	Residual DC current to be interrupted (Ires). Isolation Time.	Switching unit
Discharge	Ability to discharge one of the units connected to the switching unit, after the opening. The inrush current during the discharge shall be limited to acceptable level.	Discharge time. Maximum peak current.	Switching unit

Auto-reclose	After activation of an FSD, the switching unit may attempt to auto-reclose based on local information only, assuming the fault has been cleared.	O-C-O cycle time	Switching unit
Earthing	Ability to earth for maintenance purposes one of the units connected to the switching unit, assuming the unit has already been discharged.	N/A	Switching unit
Reconfiguration sequence	The DC Grid controller may provide operational simplifications to perform a reconfiguration sequence of the HVDC system.	Reconfiguration time.	DCGC

6. Continuous control

The HVDC systems should deliver scheduled power while ensuring the security and reliability of the HVDC systems themselves to guarantee their continuous operation. It is imperative to prevent power flows and DC voltages that exceed the physical capabilities of system components. Disturbances in the system can disrupt the balance of power, resulting in fluctuations in DC voltages. In such instances, the AC/DC converters within the system must promptly and collectively restore system energy equilibrium to prevent violations of system limits.

In order to ensure both the scheduled power transmission and reliable, continuous system operation, the overarching control architecture of HVDC systems is hierarchically structured, with defined roles and responsibilities allocated to each layer and secure exchange and propagation of essential information between each layer.

This chapter first delineates the physical and operational constraints that HVDC systems must consistently satisfy, along with providing definitions of system-level operational DC voltage ranges and system states in terms of DC voltage. It then elucidates the expected roles and responsibilities of each control layer within the control hierarchy, considering the delineated constraints and limitations. Based on those, the fundamental principles of DC grid voltage control, classified into primary and secondary DC voltage controls analogous to the AC system frequency framework, are described. Finally, comprehensive continuous control functional requirements for each subsystem are summarized.

6.1 HVDC System Physical and Operational Constraints

This section presents the pertinent physical constraints of the HVDC system that shall be ensured by continuous control. Subsequently, it provides the definitions of system-level operational DC voltage ranges and the system states in terms of DC voltage level.

6.1.1 Physical Constraints on the DC side of System Components

All components in the HVDC systems shall be designed to operate within the defined ratings and withstand capabilities. The continuous control of the HVDC systems shall be designed to ensure continuous operation without violating any physical limits. The following outlines pertinent physical constraints to be considered in the design of continuous control.

- **AC/DC Converters:** AC/DC converters have inherent physical limitations regarding over and under voltages, both in terms of terminal-to-ground and terminal-neutral voltages. While the network code for HVDC systems [4] clearly stipulates the AC voltage and frequency ranges as well as associated time within which the HVDC converter station must remain connected, it is important to note that it only defines requirements for the AC side at AC-PoC, with no regulation currently in place for the DC-PoC. Building on these statements, it is considered appropriate to adapt them for DC voltage in HVDC systems. Thus, AC/DC converters shall be capable of staying connected to the DC network and capable of operating within the DC voltage ranges for the time periods specified by the relevant system operator, in coordination with the relevant TSOs[8]. The required operational performance and allowed protective measures must be consistent with the specified DC-FRT profile (see Section 7 for more details). The HVDC system owner and the relevant system operator, in coordination with the relevant TSO may agree on wider or narrower voltage ranges and associated period of time for operational capability of individual AC/DC converter stations in order to ensure the best use of the technical capabilities if needed, especially in case of radial and sparse DC network. Additionally, AC/DC converters are subject to rated current equivalent to maximum current capabilities within which their secure operation shall be ensured. The maximum current may change over time depending on the constraints of the converter unit (e.g. problems with the cooling system).

- **High Voltage transmission lines/units:** They shall be designed to withstand the temporary and continuous DC voltage profile within the specified DC insulation capabilities. Additionally, they shall be designed to have sufficient thermal capability to continuously carry the rated current. Temporary overcurrent is possible due to the thermal capacity of the conductor, it depends on the environment and external conditions (e.g. temperature), according to IEC 62067 [5].

- **Neutral transmission lines/units:** Neutral transmission lines and units, here referring to return conductors such as DMRs, typically operate at much lower voltages relative to the ground and shall be designed with adequate DC insulation capabilities. Furthermore, like high voltage conductors, they shall be designed to possess sufficient thermal capability to continuously accommodate the rated current.

6.1.2 Operational Constraints at AC Connection Points

In addition to the physical constraints, HVDC systems are required to comply with the functional requirements at each point of connection with the AC systems in accordance with [4]. In other words, the AC/DC converters that interface with AC systems must meet the specified operational requirements. They are broadly classified into those pertaining to transmission capability and those related to functional requirements. The following introduces the essential transmission capabilities.

- **AC active power exchange capacity:** the maximum AC active power transmission capacity, denoted by P_{max}, shall be defined at the AC side connection point (AC-PoC) for steady-state condition. P_{max} means the maximum continuous active power which an HVDC system can exchange with the AC network at each AC-PoC as specified in the connection agreement or as agreed between the relevant system operator and the HVDC system owner. In the case of a bipolar AC/DC converter station, this must be defined separately for bipolar operation and monopolar operation, where one of converter units is out of service. Unless otherwise specified, the AC active power transmission capacity shall be defined for each direction of power.

- **Reactive power exchange capacity**: the AC/DC converter station or unit shall possess the constructive ability of injecting or absorbing reactive power at the AC-PoC within the U-Q/Pmax profile specified by the relevant system operator, in coordination with the relevant TSO. Additionally, when operating at an active power output below its maximum AC transmission capacity, the AC/DC converter station

[8] For instance, NC-HVDC Article 18 stipulates the minimum time periods an HVDC system shall be capable of operating for AC voltages deviating from the reference 1 p.u. value at the connection points without disconnecting from the network.

shall be capable of operating in every possible operating point, as specified by the relevant system operator, in coordination with the relevant TSO and in accordance with the reactive power capability set out by the U-Q/Pmax profile specified.

6.1.3 Functional requirements at AC connection points:

The functional requirements that the HVDC system and each of AC/DC converter station or unit within the system must satisfy are comprehensively stipulated in [4]. For the sake of self-containment, please see Appendix 9.1 for a concise summary of these requirements.

6.2 Definition of System-Level DC Voltage Ranges

The system-level DC voltage ranges are one of the most important parameters for achieving secure and reliable operation of the HVDC system[9]. **The system operator shall aim to maintain voltages at all nodes in the system within these voltage ranges.** They must be carefully established so as not to violate the rated design constraints of the components in the system in the event of credible and dimensioning disturbances[10]. This ensures the proper operation of the DC grid and desired power flow while also respecting the compliance with the operational requirements at each of the AC-PoCs.

The system operator shall aim to maintain voltages at all nodes in the system within these ranges.

They shall serve as the basis for monitoring the system's condition and for coordination of specific requirements for individual equipment.

It should be noted that terminal-to-neutral and terminal-to-ground voltages may vary depending on the topology of the HVDC system and operating conditions. Therefore, the definition of DC voltage ranges must be specified, indicating which voltage they refer to. In the context of continuous control, the DC voltage specifically refers to the pole-to-neutral voltage, unless stated otherwise. This is because pole-to-neutral voltage is relevant for most control considerations. On the other hand, the pole-to-ground voltage is considered pertinent for aspects related to design and protection, as well as insulation coordination.

The behaviour of DC voltage in HVDC systems can broadly be categorized into three ranges with respect to time: transient, dynamic, and steady state.

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[9] For AC systems, SOGL Article 27 defines system voltage ranges as the voltage limits that each TSO shall endeavour to maintain at each AC-PoC within the system during operation.

[10] In a sparse DC grid with long-distance transmission lines, applying uniform voltage ranges to all converter stations may not always result in the most economical design. While the general principle of maintaining consistent voltage ranges across all nodes should remain valid, specific voltage ranges can be agreed upon between HVDC system owner and the system operator, in coordination with the relevant TSOs, when deemed necessary. Please refer to Article 18(2) of for the corresponding formulation in AC systems.

The **transient time range** is primarily characterized by fast electromagnetic stress induced typically by a fault or switching event in the system. The relevant voltage levels and envelopes should be determined within the protection design, accounting for transient stress and insulation coordination, and it is thus not part of the continuous control. The behaviour and withstand capability of the system during transient phenomena is discussed in Section 7.3.

The time range following this is defined as the **dynamic time range**, where the speed at which the system reaches a steady state is predominantly determined by the controller performances. To the extent possible, overshoot and undershoot of the dynamic response related to an event shall not exceed the dynamic voltage range in order to guarantee continued operation of the system and avoid triggering unintended protective actions. Additionally, the system should exhibit sufficient damping to achieve a new steady-state within the desired settling time.

In the **steady-state time range**, voltage profiles are predominantly determined by the load flow and DC system resistance. In this state, the DC voltage of each node shall fall within a specified range, ensuring the entire system is capable of operating permanently without violating physical capabilities. It's important to note that security margins may be different depending on pre-contingency operating conditions. Thus, the system operator shall strive to maximize the safety margins in steady-state operation to be prepared for realistic incidents that might happen.

FIGURE 15 presents the conceptual illustration of the system-level DC voltage profile, indicating also the parameters essential for this definition.

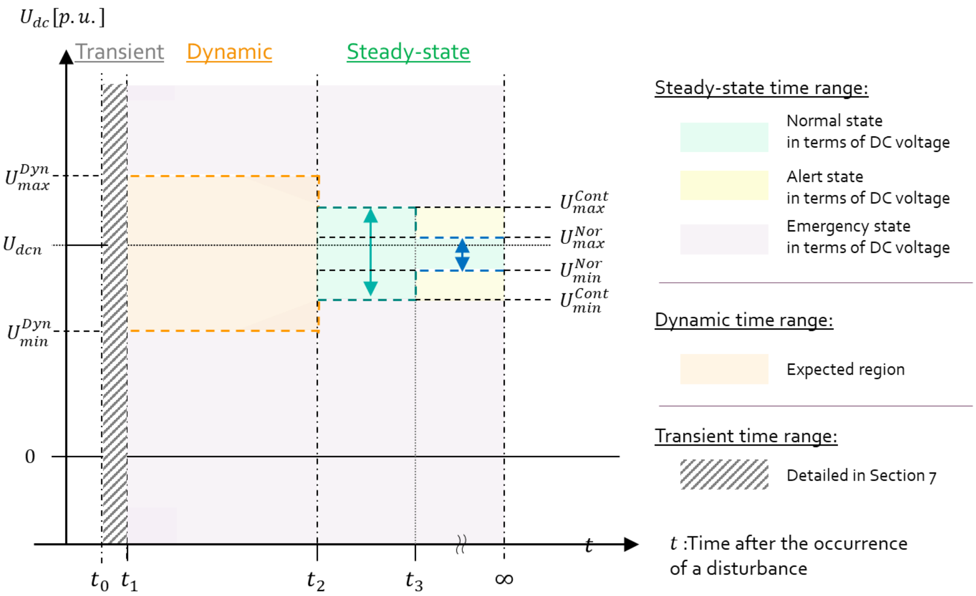


FIGURE 15: General illustration of system-level DC voltage profile.

The parameters are defined as follows:

Voltages	$U_{max}^{Dyn}, U_{max}^{Dyn}$ $U_{max}^{Cont}, U_{min}^{Cont}$ $U_{max}^{Nor}, U_{min}^{Nor}$	Maximum/Minimum dynamic DC voltage limits Maximum/Minimum continuous DC voltage limits Maximum/Minimum normal operating DC voltage limits
Time	$t_1 \leq T_{max}^{Rec} - t_0$	T_{max}^{Rec} here denotes the maximum time for full voltage recovery time to dynamic voltage range (see Section 7.3.2)

$T_{max}^{Dyn} = t_2 - t_1$ Maximum settling time

$T_{Alert} = t_3 - t_2$ Alert-state triggering time in terms of steady-state DC voltage

Furthermore, the system's security is characterized by various other voltage levels, including, but not limited to, the energy absorber unit activation voltage and converter blocking undervoltage. Therefore, the parameters delineating this profile should be specified by the system operator by comprehensively considering all relevant factors, with particular emphasis on the worst-case scenario, i.e. potentially identified dimensioning incidents.

In the following, the detailed definitions of the DC voltage ranges characterized by the introduced parameters within the respective time ranges are presented, focusing on steady-state and dynamic time ranges, along with their implications in terms of HVDC system operation and the expected functionality of the equipment within the system.

6.2.1 Static DC voltage range in Steady-State time range

- **Normal Operating DC Voltage Range** $[U_{min}^{Nor}, U_{max}^{Nor}]$: This range is defined as an interval around the nominal DC voltage between specific upper and lower voltage levels, i.e. $U_{min}^{Nor}, U_{max}^{Nor}$. This range does not have to be symmetrical. It is expected that the voltage at any point within the system falls within this range under normal operating conditions. Therefore, this range shall be established to encompass all foreseeable power flow condition and network configuration. This means that the voltage setpoints of any converter station or unit must fall within this range.

- **Continuous Operating DC Voltage Range** $[U_{min}^{Cont}, U_{max}^{Cont}]$: This range refers to a designated voltage range within which voltages shall be contained in case of ordinary contingencies, provided that such contingencies do not exceed the overall capability of the system. All equipment shall be capable of continuously operating within this range without compromising its security. In the event of contingency, the DC voltages of the node within the HVDC system may deviate beyond the normal operating DC voltage range, but in steady state, they are expected to remain within this continuous operating DC voltage range. The relevant system operator is thus responsible for determining the appropriate primary DC voltage control parameters of each converter station/unit, ensuring that the voltages of all nodes within the system remain within this range in steady state in the event of all credible contingency scenarios.

- The continuous operating voltage range inherently encompasses the normal operating voltage range, however, in cases where voltages fall within this range but outside of the normal operating DC voltage range, it is deemed undesirable due to the reduced security margin. Therefore, remedial control action, such as secondary DC voltage control, shall be taken within the specified time frame to bring the voltage back into the normal operating DC voltage range.

- **Abnormal over/undervoltage ranges** $[-\infty, U_{min}^{Cont}]$ and $[U_{max}^{Cont}, \infty]$: These ranges are defined as the range outside the continuous operating DC voltage range. In the event of a disturbance in the HVDC system leading to an overvoltage or an undervoltage and exceeding the continuous operating DC voltage range, it is imperative to promptly take appropriate discrete countermeasures.

6.2.2 Dynamic DC voltage range in Dynamic time range

- **Dynamic DC voltage range** $[U_{min}^{Dyn}, U_{max}^{Dyn}]$: This range is defined by the maximum and minimum dynamic DC voltage levels, $[U_{min}^{Dyn}, U_{max}^{Dyn}]$. In the event of a disturbance, it is expected that the primary DC voltage control (See Section 6.5) contains peak DC voltage overshoots and undershoots within this range, to the extent possible given the physical and operational capabilities. The primary DC voltage control shall be designed to contain the voltages within these ranges considering the credible and dimensioning disturbances.

- Additionally, after any disturbance, it is expected that voltage oscillations are damped and falls within the continuous operating DC voltage range within the specified maximum settling time T_{max}^{Dyn}.The system operator is responsible for ensuring those limits. To achieve these objectives, the system operator, in coordination with the relevant TSOs, must specify the dynamic behaviour required for each converter.

6.2.3 Transient DC voltage range in Transient time range

Transient voltages are highly location-dependent phenomena and are not considered as the representation of the system state. They are associated with local protective measures and the DC-FRT requirements of AC/DC converter units. For further details on the functional requirements pertinent to transient time range, please refer to DC-FRT requirements of converters defined in section 7.3.

6.3 Definition of System States in terms of Steady-State DC Voltage

Continuous monitoring of the system condition through gathered measurements and relevant information is essential for ensuring the reliable operation. Following the AC system convention clearly delineated in Article 18 of SOGL [6], the system state shall be categorized into "*normal*," "*alert*," and "*emergency*" states according to the defined criteria. Then, for each state detected, predefined actions shall be taken.

The states of the systems are typically defined by multifaceted factors. In AC systems, these factors include AC voltage levels, power flows, frequency deviations, and the availability of both active and reactive power reserves to withstand contingencies in the established contingency list.

Concerning HVDC systems, it is crucial to establish the relationship between the voltage ranges defined in the previous section and the DC voltages observed in a steady state. The following outlines the criteria for distinguishing between the system states from the observed DC voltages. It is important to note that these criteria shall be complemented by other conditions in a disjunctive relationship. The applicability of the following definitions is, hence, limited to the observable DC voltages. For additional definitions related to contingencies, please refer to Section 7.2.1.

6.3.1 Normal state in terms of DC voltage:

In terms of DC voltage, the HVDC system shall be in normal state when the following conditions are fulfilled:

- the voltages of all the nodes in the system are within the normal operating DC voltage range.
- the conditions established for the alert and emergency state are not fulfilled.

The normal state in terms of DC voltage is associated to the normal operating DC voltage range. The overall HVDC system is expected to ensure sufficient margins to keep the system within the continuous operating DC voltage range in case of ordinary contingency, provided that such contingency does not exceed the overall capability of the system. The system shall strive to maintain or always restore the system voltages back to the normal operating range through the secondary DC voltage control by the DC grid controller during operation.

6.3.2 Alert state in terms of DC voltage:

In terms of DC voltage, the HVDC system shall be in alert state when:

- All nodes are within the continuous operating DC voltage range, but one or more nodes are outside the normal operating DC voltage range for a period longer than the alert-state trigger time.

- The alert state means that even though the voltages at all nodes in the system stay within the continuous operating range and meet the security requirements in terms of DC voltage, the operation in a state of reduced security margin persists. This condition indicates a state of alert due to potential issues with the remedial action scheme and the need for promptly re-establishing the necessary security margins.

6.3.3 Emergency state in terms of DC voltage:

In terms of DC voltage, the HVDC system shall be in emergency state when:

- The voltages do not meet the criteria for either the normal or alert state defined above.

6.4 Continuous Control Architecture

IEC TS 63291 [3] presents the general continuous control architecture, which consists of four distinct control layers. Each layer is associated with an indicative typical cycle time for actions. The purpose of this hierarchy is to provide clarity regarding the scope of responsibility, the priority of actions (which must be higher as the layer goes down), the availability of data, and the actuators involved. For more details regarding the IEC definitions of the continuous control hierarchy and the defined information propagation through the control layers, please refer [3].

6.4.1 General Continuous Control Hierarchy

While ensuring the consistency with the definitions in [3], **FIGURE 16** depicts the assignment of the functional hierarchy to the subsystems defined in Section 4.

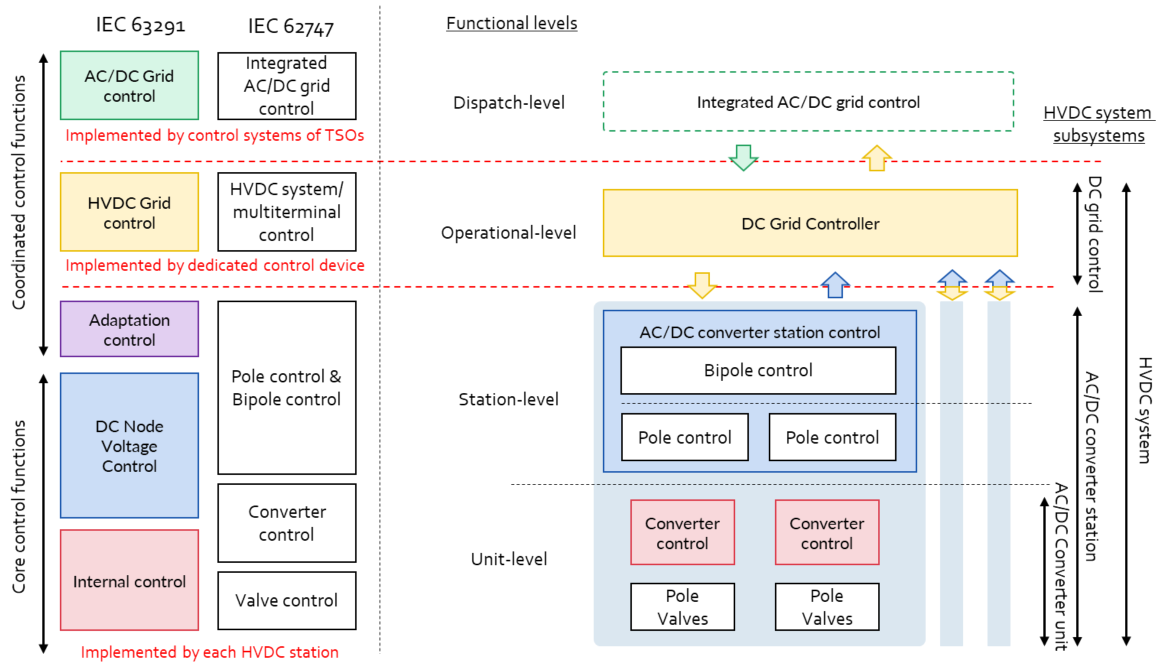


FIGURE 16: General continuous control hierarchy. Additional communication interfaces may be required, though not explicitly depicted in the figure, particularly for the coordination with PPMs.

The following sections outline the expected roles of the subsystem(s) corresponding to each level in the continuous control architecture as well as the generic description of each function.

6.4.2 Dispatch-Level

The dispatch-level, introduced as the highest layer in the continuous control architecture in [3] and is designated as "Integrated AC/DC system control" in IEC 62747 [7], conceptually represents a control system that governs the integrated operation of AC and HVDC systems in a power system.

From the perspective of an HVDC system, this is an **external** control system that serves as the only interface through which the DC grid controller receives all necessary set-points and instructions essential for ensuring the stable operation. It is envisaged that no other interface bypassing this is in place unless there are no communication issues, although in future different design concepts may evolve depending on special design need of the TSOs or HVDC project owners.

This level shall provide the DC grid controller with the active power transmission order for the upcoming dispatch cycle as well as all the other setpoints at the AC and DC connection point (such as but not limited to reactive power set-points, constraints, and any other operational instructions as specified by the relevant TSOs). These inputs, although not strictly limited, may regularly be updated in conjunction with the dispatch program schedule, as specified by the relevant TSO in coordination with adjacent TSOs and hence, may be updated alongside any other generation units in the grid. Therefore, in accordance with the IEC standard, these set of input values for a given time period are hereinafter referred to as **converter schedule**.

6.4.3 Operational-Level

The operational level in the hierarchical continuous control architecture corresponds to the DC grid controller, which is an interface for obtaining information on the power flow conditions and accessing all electrical nodes in the HVDC system. The primary objective of the DC grid controller is to achieve the converter schedules set by the dispatch-level while ensuring compliance with all the security constraints within the HVDC system, as specified by the relevant TSO. During operation, internal and external system conditions may change. Thus, the DC grid controller shall be capable of taking appropriate measures to prevent overloading and overvoltage of any equipment and to achieve the Normal Operating DC voltage ranges as specified in Section 6.2.1, even though it may result in deviation from the initial converter schedules received. The DC grid controller shall ensure that this deviation is both reasonable and justifiable to all stakeholders involved, and then report to the higher control hierarchy, i.e., the dispatch-level.

6.4.3.1 HVDC System state analysis

Like the state estimation commonly conducted in existing AC systems, the DC grid controller shall be aware of the actual conditions of the HVDC system. The system's state is determined based on available real-time measurement. The minimum set of information required for the system state analysis is specified in [3] and categorized as status signal and physical quantities. The system state analysis can be categorized into three main components for convenience:

- **Element status analysis:** The DC grid controller shall comprehend the real-time status of every element within the HVDC system. This involves gathering continuously communicated essential system state variables and equipment state, defined as "station Information", from the AC/DC converter, AC and DC switching stations, energy absorption devices, as well as PPMs.

- **System topology analysis:** Based on the element status analysis, the DC grid controller shall identify the actual grid topology. In general, contingencies can result in the outage of different grid components such as cables or converters that may lead to new grid topologies, such as a system split.

- **Element limitation analysis:** A particular emphasis is given to the importance of comprehending the actual capabilities of converter stations. While the tolerable maximum and minimum values for the DC voltage are typically determined by the design of the component, the limitation regarding active power, as well as reactive power capabilities of an AC/DC converter station may deviate from the rated values during operation due to the state of the cooling system and power electronic devices.

6.4.3.2 DC power flow optimization

One of the essential functionalities expected from the DC grid controller is to establish an adequate DC power flow by sending out appropriate set-points to the AC/DC converter stations. This includes a verification of the received converter schedules and an assessment of its feasibility in accordance with the actual state of the system.

Under changing grid conditions, including deviations in offshore wind generation from forecasted levels or limitation on the transmission capacity due to disturbances, the DC grid controller must accordingly determine the optimal DC power flow while ensuring all the security constraints of the system described in Section 6.1. These constraints encompass the voltages of all nodes, including the neutral voltages, the physical and operational constraints of the AC/DC converter units, and the current capacity of conductors including DMRs.

The objective function for the optimal power flow calculation shall be the operational discretion of the relevant TSOs. Potential factors to be considered, though not exhaustive, include:

- Loss minimization
- Security margin
- Minimization of deviation between pre- and post-contingency situation at each PoC-AC
- Adherence to repartition factor (pre-defined power sharing ratio between control areas)

The parameters required for DC power flow optimization depend on the selected optimization criteria, which shall be left to the discretion of the system operator. It is imperative that the operator identifies these essential parameters beforehand and adequately provides them as input to the DC grid controller.

6.4.3.3 Secondary DC voltage control

Analogue to the hierarchical structure of frequency control in AC systems, which is divided into primary, secondary, and tertiary frequency control, the DC voltage control in DC grids shall also be composed of a hierarchical manner. While the primary DC voltage control is a local control mechanism and thus implemented at each AC/DC converter station, the secondary DC voltage control is an overall HVDC grid control scheme.

Details of the required functions are provided in detail in the dedicated section: Section 6.7.

6.4.3.4 Ramp rate coordination

In general, an abrupt change in power can stress and threaten the AC system stability and, thus, should be avoided. The power set points are usually associated with ramp rate limits. In practice, there are various instances where the power set-point change shall be limited by the specified ramp rate, and typical ramp rate depends on the situation.

The power transmission order for an HVDC system can potentially change significantly from one to the next market time unit[11]. In order to ensure the interconnected AC systems' stability, restrictions are imposed on the ramp rate for power flow change. Such ramp rate limitations shall be predetermined by the relevant TSOs through the assessment of the frequency stability and voltage sensitivity and are normally in the order of minutes. Therefore, for each change of market time unit, an adequate ramp rate must be applied to the set-points to be sent out to the AC/DC converter stations.

DC voltage and power restoration through the secondary DC voltage control following an unscheduled event requires a substantially faster timeframe than the typical dispatch operation.

In addition, for AC ancillary services, such as Emergency Power Control (EPC) and automatic Frequency Restoration Reserve (aFRR), ramp speed specifications are determined by the relevant TSOs of both the receiving and supplying sides for each service, respectively. For instance, in the case of EPC, an automatic reduction or increase of power pursuant to an instruction from the applicable TSO, which may also involve

[11] "Market time unit" means the period for which the market price is established .

power reversal, the ramp rate limitations or requirements are typically in the order of seconds, e.g. up to 999 MW/s.

It is also imperative to acknowledge the distinction between onshore and offshore stations connected to PPMs. The technical specifications on the feasible ramp speed of the connected PPMs must be considered.

Moreover, applying the same ramp rate limitation across all stations, while power step orders differ among them, can lead to potential power imbalances during the ramping process, seen as a disturbance to the HVDC system. Thus, it is desired that the ramp rate limitations are coordinated within the technical specifications and assigned to each AC/DC converter station differently in line with the power step orders such that secure transition of operating points can be ensured.

Consequently, given the significant differences in expected ramp rates for dispatch, re-dispatch following unscheduled events in the HVDC system, and potentially AC ancillary services, the DC grid controller shall be capable of adequately coordinating the ramp rate of individual converter stations to ensure the power balance during the ramping process.

6.4.3.5 Offshore power curtailment

Offshore power curtailment refers here to the intentional reduction of power generation of offshore PPMs below their maximum potential production. This measure may be required to prevent congestion within the DC grid and must be done in accordance with the regulatory agreements. While such considerations shall be taken into account in the DC power flow optimization process, as detailed in Section 6.4.3.2, this section places particular emphasis on the interface requirement of the DC grid controller and the offshore power curtailment in emergency scenarios.

In the event of a disturbance in a DC grid, the primary DC voltage control of AC/DC converter stations handle the power imbalance and contains the DC voltage excursion. However, it is crucial to acknowledge that the power limitations of converter stations inherently impose constraints on their ability to contain such disturbances.

Consider a scenario where the incoming power from PPMs exceeds the total export capability of the HVDC system, due to power limits of the onshore AC/DC converter stations, or a fault on AC side of an onshore station or in an interconnector cable. When the total power injection exceeds the maximum export capacity of the HVDC system, it will result in a persistent increase in DC voltages. It is imperative that this surplus energy must be dissipated by immediate activation of the energy absorber units upon detection of overvoltage exceeding a predefined voltage threshold. However, since the energy absorber unit can dissipate energy only for a limited duration, the wind power curtailment process must be initiated before exceeding the time constraint of the energy absorber units.

To achieve this, various technical options are possible. One such option involves a direct communication channel between the DC grid controller and the PPM controllers. Upon detection of the fault or activation of energy absorber unit, the DC grid controller dispatches a new power limit with a specified ramp-down rate to each of the relevant PPM controllers in order to initiate their offshore power curtailment, which then can limit the PPM output power accordingly. Alternatively, communication from the DC grid controller to offshore AC/DC converter station is also a viable option. In this scenario, the offshore converter station would take the necessary measures to curtail the wind power. This could be achieved either by communicating with the PPM controllers of the connected wind turbines or by modulating the electrical signals that are detected by the wind turbines, prompting them to adjust their output [2].

Moreover, in case of an AC grid experiencing congestion, upon receipt of a request from the responsible AC system TSO, sending a curtailment order to the PPM is also envisioned as a role of the DC grid controller.

6.4.3.6 Converter control mode coordination

Prior to operation, the HVDC system operator, in coordination with the relevant TSO, is responsible for predefining the control mode and the associated parameters of each converter unit, within the parameter range specified. Frequent modifications and update of control parameters are not anticipated, expect perhaps on a seasonal basis, or in certain situations like modification to another grid configuration or change in network constraints. The appropriate parameters associated with any control modes values should be selected in accordance with the parameters and parameter ranges specified during planning and testing phases as outlined in [8]. Prior to actual operation, those values shall be thoroughly assessed for various load flow conditions and a set of contingencies. Through this process, all pertinent stakeholders shall agree on the criteria for selecting control modes and associated parameters for each converter unit across various operational situations.

The DC grid controller should be responsible for setting the control modes and their associated parameter. During the operation, the DC grid controller shall oversee the coordination of the control modes and their associated parameter, making necessary adjustment to meet requirements, all while adhering with predefined criteria.

6.4.4 Station-Level

The station-level encompass high-level control systems responsible for the control, monitoring, and protection functions within an AC/DC converter station. It shall receive the comprehensive converter schedule from the DC grid controller, which shall include at least the valid set-points for active power and DC voltage for each converter unit in the station.

Furthermore, given that this level has access to all the information within the AC/DC converter station, it shall possess the capability of continuously sending the specified set of signals to the DC grid controller. This shall include essential state variables and equipment status signals and those defined as *station information* in [3], as well as any additional signals specified by the relevant TSOs.

Additionally, in case of a bipolar configuration, control systems are divided into bipolar and pole controls, in alignment with IEC 62747 [7]. Note that bipolar control is defined as a control that necessitates the state variables from both the positive and negative converter units, whereas pole control shall rely exclusively on the pole quantities, independent of the counterpart.

6.4.4.1 Bipole Control

In bipolar configuration, an AC/DC converter station comprises positive and negative AC/DC converter units. It is essential that the functional requirements at the AC PoC are fulfilled, either by the station as a whole or individually by each converter unit, in alignment with the specifications set by the relevant TSO[12].

In the case of bipolar configuration with DMR, from the perspective of the DC connection point and DC functional requirements, a bipolar AC/DC converter station possesses two distinct fundamental degrees of freedom: positive and negative AC/DC converter units, yet the physical configuration to which the station is interconnected consists of three conductors: positive, negative, and DMR, as shown in **FIGURE 17**. Therefore, this configuration inherently entails a degree of flexibility in associating the control capabilities of the two converter units within the station with the system variables that are subject to the regulation. Depending on how the control capabilities are associated with the variables, a control function can be classified either as bipolar control or pole control.

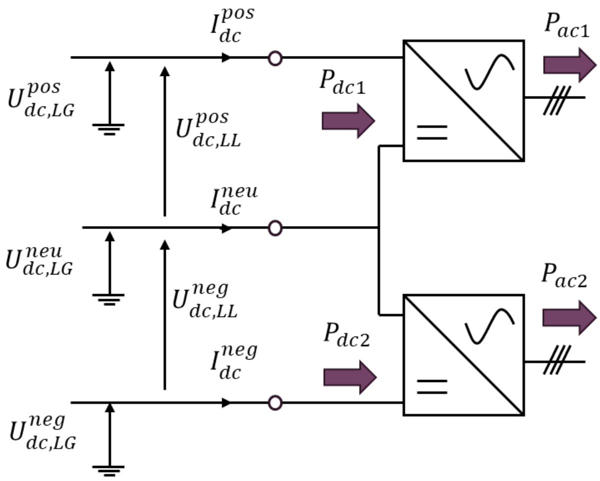


FIGURE 17: Conceptual illustration of DC variables in a bipolar configuration.

One option is to directly correlate the operational capabilities of each converter unit with the physical quantities of its respective pole. This ensures a clear distinction of the responsibilities and independent control over the positive and negative poles. The DC voltage droop control (detailed in Section 6.5) can be understood as controlling the interrelation between voltage and power (or current) in each pole in accordance with the specified characteristic with no consideration for other pole. It is important to note that in scenarios involving changes in the system's configuration, especially the loss of the DMR connection, the independence among the positive and negative pole variables changes. Such changes in the system must be detected and appropriate measures should be taken by the DC grid controller. It can also be considered that, as shown in **FIGURE 18**, a backup function implemented locally at the station-level, be in place to take the necessary action to regulate/limit neutral quantities when communication with the DC grid controller is lost.

[12] Unless otherwise specified, specific features of the AC system may be implemented at the station level or at the unit level, at the vendor's discretion.

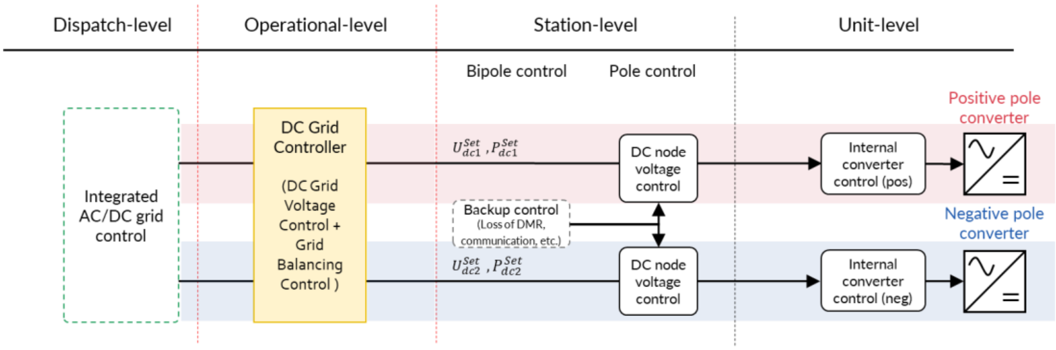


FIGURE 18: Conceptual illustration of the option ensuring independent control over the positive and negative poles, alongside bipolar level control reconfiguration is mentioned. Only the signals relevant are displayed.

Nonetheless, under normal operational conditions, these controls are pole independent controls that do not depend on the quantities of the other pole option; and hence, categorized as pole control. However, it can be noted that this option does not inherently provide any mechanism for controlling the quantities associated with the neutral (or metallic return) conductor.

To address this concern, two innovative solutions have been proposed, summarized as follows.

Option 1, as introduced in [1], originates from the traditional symmetrical components transformation (Fortescue transformation) used for 3 phase AC systems and extends this methodology to DC systems. This approach involves relating the quantities of each pole, specifically, pole voltages and currents, through predefined coupling matrices, deriving balanced and residual mode voltages and currents. By considering the derived quantities as control variables and adopting a similar approach to the set-points for the AC/DC converter station, the positive and negative AC/DC converter units are linearly transformed into two decoupled subsystems in the balanced and residual components. **FIGURE 19** shows the conceptual illustration of this option.

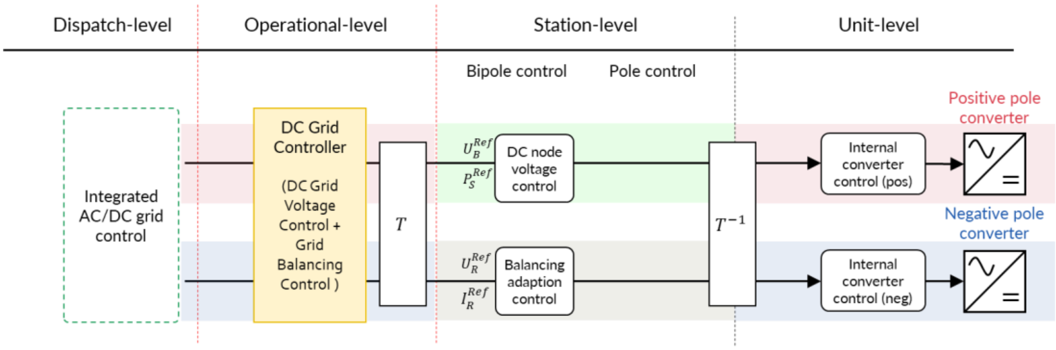


FIGURE 19: Conceptual illustration of Option 1, within which only the signals relevant are shown.

Option 2, on the other hand, maintains the fundamental independencies between the positive and negative poles while introducing supplemental control measure over the neutral quantity. This approach leverages the inherent and intuitive separation of the poles, while employing the supplemental measure aimed at neutral quantity to manage the issue arising from the asymmetrical power flow conditions. **FIGURE 20** provides a conceptual depiction of this option.

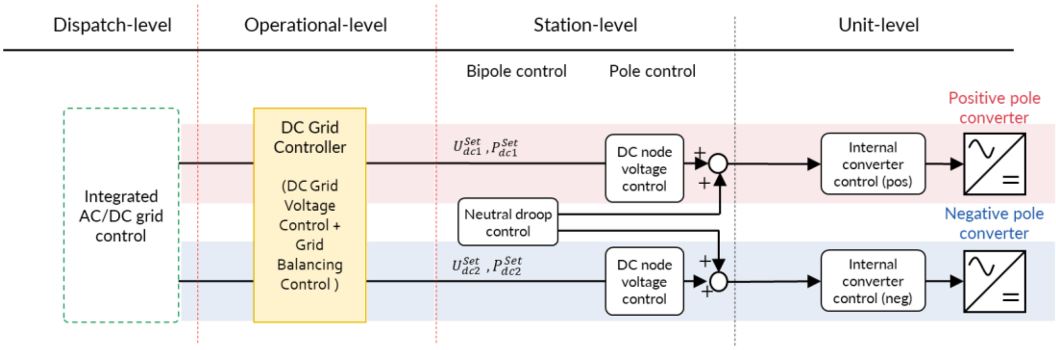


FIGURE 20: Conceptual illustration of Option 2, within which only the signals relevant are shown.

The comparative performances of these solutions have been demonstrated by their respective entities proposing the solutions. In addition, both have been thoroughly investigated analytically. While they are significantly different in terms of the operating principles and associated design space, they share a certain commonality in terms of the regulation over the neutral quantities, which necessitates, in both, coordination in measurement and actions from both the positive and negative converter units.

As delineated in Section 6.1, while it is imperative to ensure all the physical and operational constraints during operation, the bipolar control shall be capable of managing the following operational conditions of the station:

1. Normal operation of the station: This assumes an ideal bipolar operation with the presence of a DMR connection, where the identical functioning of the positive and negative pole units would be expected.
2. Operation in the event of disconnection with the neutral (DMR connection loss)
3. Asymmetric monopolar operation due to the loss of one of the pole converter units or a pole conductor
4. Asymmetric operating set-points of power between positive and negative units: This situation arises when there's a difference in power injection between the positive and negative poles, which might occur due to decoupled AC busbars in offshore stations connected to PPMs, maintenance activities on one of the pole converter units, or the loss of a pole conductor connecting a station. Different operating set-points between the positive and negative units also implies a difference in the available headroom capacity between the units.
5. Asymmetric power capability: This involves scenarios where there is a problem, such as in an AC transformer in one of the units, affecting the converter unit's power capability and necessitating asymmetric operation.

Ultimately, it falls upon the system operator's responsibility to clearly define the functional specifications and interface signals between operational level and station level, considering all relevant factors and potential operational conditions. Nonetheless, the actual implementation of the solution is at the discretion of the vendor, provided it complies with all the defined functional specifications.

6.4.4.2 Pole Control

Pole control, as defined in accordance with [7], refers to the control system dedicated to the management of each converter pole within an AC/DC converter station. The pole control shall be implemented and managed individually for the positive and negative poles. The functional requirements for the pole control shall be defined for the behaviour of that pole, independent of the counterpart pole.

6.4.5 Unit-level

The unit level includes the internal converter control and the valve control of each converter unit. This level represents the lower most part in the continuous control hierarchy and is highly specific to the technology and the proprietary designs of each vendor.

Regarding converter control, there are two distinct control schemes: Grid Following (GFL) and Grid Forming (GFM). These schemes differ in the fundamental design principles, leading to differences in the withstand capability and dynamic performance requirements that can be fulfilled. For a detailed definition and the required performances of GFM, please refer [2].

The converter control must be designed and tuned such that all the functional requirements and performance requirements specified by the system operator and the relevant TSO are met.

6.5 Primary DC Voltage Control

This section first recalls the conventional control modes, namely fixed DC voltage control mode and fixed active power control mode. It then focuses on primary DC voltage control based on the principle of droop. Formal definitions of the droop and relevant terminology are provided.

6.5.1 Definitions of conventional control modes

The fixed DC voltage control is an extension of the conventional master/slave control method in traditional point-to-point systems. In this setup, only one station in the grid is responsible for maintaining the DC voltages of the system constant, while the other track the respective active power set-points. The following provides a brief description of the two conventional control modes.

6.5.1.1 Fixed DC voltage control mode

When operating in fixed DC voltage control mode, the AC/DC converter station or unit shall be capable of maintaining the DC voltage of its DC-PoC at the reference specified by the system operator or the DC grid controller by adjusting active power injection/absorption according to the specification set by the system operator. The adjustment of the active power response shall be limited by the maximum HVDC active power transmission capacity of the converter or otherwise specified (in each direction).

6.5.1.2 Fixed active power control mode

When operating in fixed active power control mode, the AC/DC converter station or unit shall be capable of regulating its active power according to the specifications set by the system operator, in coordination with the relevant TSOs, according to NC-HVDC Article 13 [4].

6.5.2 Definitions of DC voltage droop

The concept of the primary DC voltage control, based on DC voltage droop control, is well recognized today; however, existing literature presents notable discrepancies in the definitions of DC voltage droop. IEC describes in [3] the DC voltage/DC power droop as the change of active power in response to a deviation of the DC voltage from its reference value, while CIGRE TB699 [9] mentions that the droop value "*is the inverse of the proportional controller gain used in the actual implementation*." In previous research initiatives such as PROMOTioN and BestPaths projects, droop is introduced as the parameter defining the characteristic of the droop control mode, determining the reference values for active power [10] or the DC voltage [11], from implementation focused perspectives, rather than providing a functional, quantifiable definition.

In light of varying interpretations existing in the literature, and referring to the definition of droop in AC system formulated in RfG Article 2 (23) [12], we suggest the definition of the DC voltage droop as follows:

The "DC voltage droop" refers to the ratio of a steady-state deviation of DC voltage to the steady-state change in active power output.

It is noteworthy to state that this definition is universal and solution agnostic, neither excluding nor prescribing any specific implementation methods.

In accordance with the above definition, the ratio, k, can be mathematically expressed as follows:

$$k = \frac{\frac{\Delta U_{dc}}{U_{dcn}}}{\frac{\Delta P}{P_n}} \text{ [p.u.]}$$

where

Steady-state deviation of DC voltage:	$\Delta U_{dc} = U_{dc} - U_{dc}^{Set}$
Steady-state deviation of active power:	$\Delta P = P - P^{set}$

and

U_{dcn}	Nominal DC voltage
P_n	Nominal power
U_{dc}^{Set}	DC voltage setpoint at DC-PoC
P^{set}	Power setpoint
U_{dc}	Measured DC voltage at DC-PoC
P	Measured power

While the droop is formally defined as the ratio between two variables: the numerator being DC voltage deviation and the denominator as active power output, a more precise clarity in the interpretation of these variables is required to ensure the consistency among the AC/DC converter stations or units within the system.

Convention of power flow direction

In accordance with IEC 62747 [7], the power flow through the AC/DC converter flowing from the DC-PoC into the converter and further on from the converter into the AC-PoC is designated with a positive sign. This definition is illustratively represented in **FIGURE 21**.

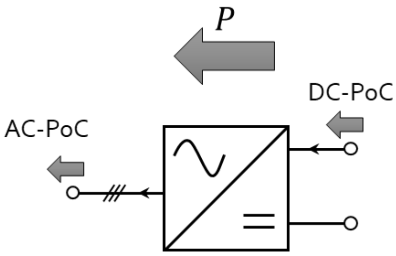


FIGURE 21: Representation of the convention of power flow direction as defined in IEC 62747 [7].

Definition of numerator and denominator variables

Concerning the numerator variable of the droop, the definition of DC voltage presents some ambiguity. DC voltage could be interpreted as the pole-to-ground voltage, pole-to-neutral voltage, or other forms such as balance or residual mode DC voltages, as proposed in [1]. An imprecise definition of the DC voltage could lead to different interpretations of the numerator variable in the droop, resulting in inconsistent behaviour among the AC/DC converter stations within the system. It is essential that a consistent definition is uniformly applied across the system. The system operator should make this selection with careful consideration, as altering them at a later stage could introduce significant challenges. For compatibility with symmetrical monopolar configurations, it is recommended that this DC voltage to be defined as the pole-to-neural voltage at DC-PoC.

Similarly, the denominator variable in the droop, referred to as active power output, is acknowledged that it encompasses the possibility of being defined as either the AC active power at AC-PoC or DC power at DC-PoC, as well as either the converter unit's power or the bipolar station power. The current preference is to use AC active power, as it aligns with the existing network code and is more directly relevant to the TSOs[13]. However, considering the future evolution of the network code, the adoption of DC power shall not be excluded. In principle, whether defined as AC active power or DC power, achieving full compliance with the droop by controlling the other requires consideration of loss characteristics, which typically remain less than 1%.

General implication of DC voltage droop

FIGURE 22 illustrates the implication of varying droop. Drawing an analogy to frequency droop in AC systems, the value of the DC voltage droop can be understood as the change in DC voltage at the DC-PoC causing the converter to change its power by 1 p.u. in steady state. For instance, a 0.05 p.u. DC voltage droop implies that a 0.05 p.u. deviation in voltage leads to a 1 p.u. change in power output of the AC/DC converter in steady state.

[13] The decision to adopt AC active power or DC power ultimately depends on where the power for dispatch is defined within the system.

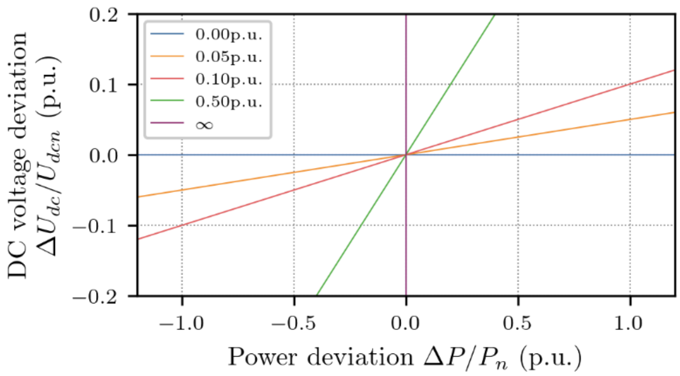


FIGURE 22: Example of characteristics in different droop.

To summarize, with a larger droop, the power output is less sensitive to changes in DC voltages, leading to a smaller contribution to DC voltage regulation. Conversely, with a smaller droop value, the power becomes more sensitive to fluctuations in DC voltage, resulting in a greater contribution to DC voltage regulation.

6.5.2.1 DC Voltage Droop Characteristics

For an intuitive representation of the steady-state behaviour of an AC/DC converter, including factors such as set-points and maximum power constraints, it is common practice to plot it as a continuous linear or piecewise linear function on a two-dimensional plane. In this representation, the vertical and horizontal axes correspond to the numerator and denominator variables of the DC voltage droop, respectively. This representation is hereinafter referred to as “DC voltage droop characteristic”, and is formally defined as follows:

The ”DC voltage droop characteristic” is defined for each converter station or unit as a representation of a desired static performance.

Neglecting the maximum power constraints, a typical DC voltage droop characteristic with an indicative droop of 0.05 p.u. is depicted in **FIGURE 23**. The dot in the figure represents the set-point assigned to the converter, i.e. $[P^{Set}, U_{dc}^{Set}] = [0.0\text{ p.u.}, 1.0\text{ p.u.}]$.

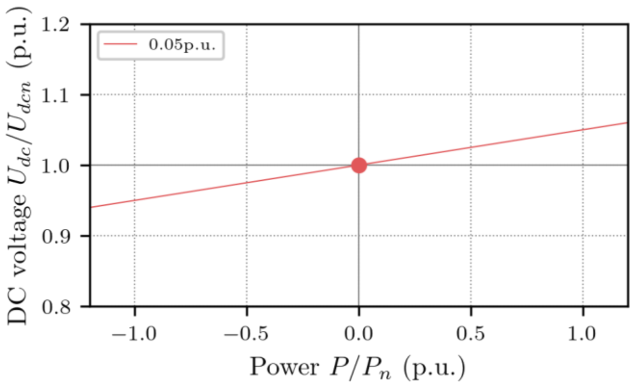


FIGURE 23: Example of DC voltage droop characteristic with a DC voltage droop of 0.05 p.u.

The DC voltage droop characteristic is derived directly from the droop. Following the definition of DC voltage droop, a mathematical manipulation results in two identical equations:

Voltage form:

$$U_{dc} = k\frac{P - P^{set}}{P_n}U_{dcn} + U_{dc}^{Set}$$

Power form:

$$P = \frac{U_{dc} - U_{dc}^{Set}}{k}\frac{P_n}{U_{dcn}} + P^{set}$$

As mentioned in CIGRE TB699 [9], if the DC voltage droop characteristics are plotted on a plane that is different from the chosen definitions of the numerator and denominator of the droop, the resulting characteristic will appear as a nonlinear function. This underscores the importance of adhering to the defined numerator and denominator in subsequent discussions or analyses.

The position of the DC voltage droop characteristics on the plane is determined by the assigned set-points, as can be inferred from the equations above. **FIGURE 24** and **FIGURE 25** show the droop characteristics employing the same droop, with **FIGURE 24** demonstrating the effect of changing the DC voltage setpoint and **FIGURE 25** depicting the impact of modifying the power setpoint, respectively. As observed, adjusting the DC voltage set-point results in a vertical shift of the characteristic, whereas modifying the power set-point results in a horizontal shift in the characteristic.

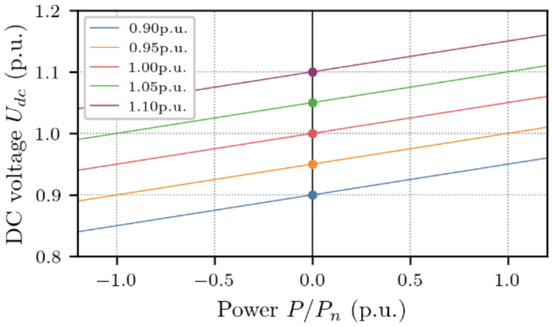


FIGURE 24: DC voltage droop characteristics with different DC voltage set-point U_{dc}^{Set}, (with $\frac{P^{set}}{P_n} = 0 \text{ p.u.}, k = 0.05 \text{ p.u.}$)

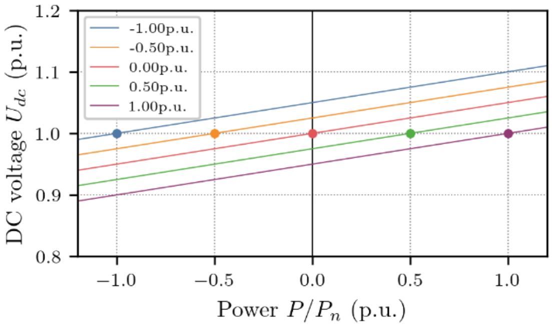


FIGURE 25: DC voltage droop characteristics with different power set-point P^{set}, (with $\frac{U_{dc}^{Set}}{U_{dcn}} = 1 \text{ p.u.}, k = 0.05 \text{ p.u.}$)

6.5.3 Static requirements of primary DC voltage control

In order to achieve improved security while achieving the maximum exploitation of the DC grid operation by overcoming the limitations of the single section droop characteristic, the implementation of multi-segment droop characteristic is essential [13]. In the context of multi-vendor, multi-terminal DC grid, ensuring interoperability between AC/DC converter stations supplied by different vendors requires the establishment of precise definitions and functional requirement for each segment, as well as comprehensive clarification of all essential parameters necessary to be specified.

The primary DC voltage control is defined as the control capability of an AC/DC converter station or unit in which the active power output changes proportionally to a change in DC voltage, in such a way that it prevents power imbalance in the DC grid and supports reaching an equilibrium point for the system.

To achieve efficient DC voltage regulation and ensure steady-state voltages remain within the continuous operating DC voltage range established in Section 6.2.1, the primary DC voltage control is divided into at least three distinct operating modes, each defined with specific operational requirements:

DC Voltage Sensitive Mode: or DCVSM means an operating mode that primarily focuses on the behaviour within the normal operating DC voltage range.

Limited DC Voltage Sensitive Mode-Overvoltage: or "LDCVSM-O" means an operating mode that is activated when the voltage exceeds the upper limit of the normal operating DC voltage range up to the maximum continuous operating DC voltage value.

Limited DC Voltage Sensitive Mode-Undervoltage: or "LDCVSM-U" means an operating mode that is activated when the voltage exceeds the lower limit of the normal operating DC voltage down to the minimum continuous operating DC voltage value.

In addition to the above modes, the following two supplemental operating modes are relevant to the primary DC voltage control in order to enhance the security of the system.

DC Voltage Limiting Mode: or "DCVLM" means a supplemental operating mode that is activated when the voltage is outside the continuous operating range, provided that the full active power headroom was not yet reached[14].

Power Limiting Mode: or "PLM" means a supplemental operating mode that aims to limit the active power output to the maximum and minimum power capability.

FIGURE 26 provides an illustrative overview of the operational implication of each mode, depicted collectively within a single plane.

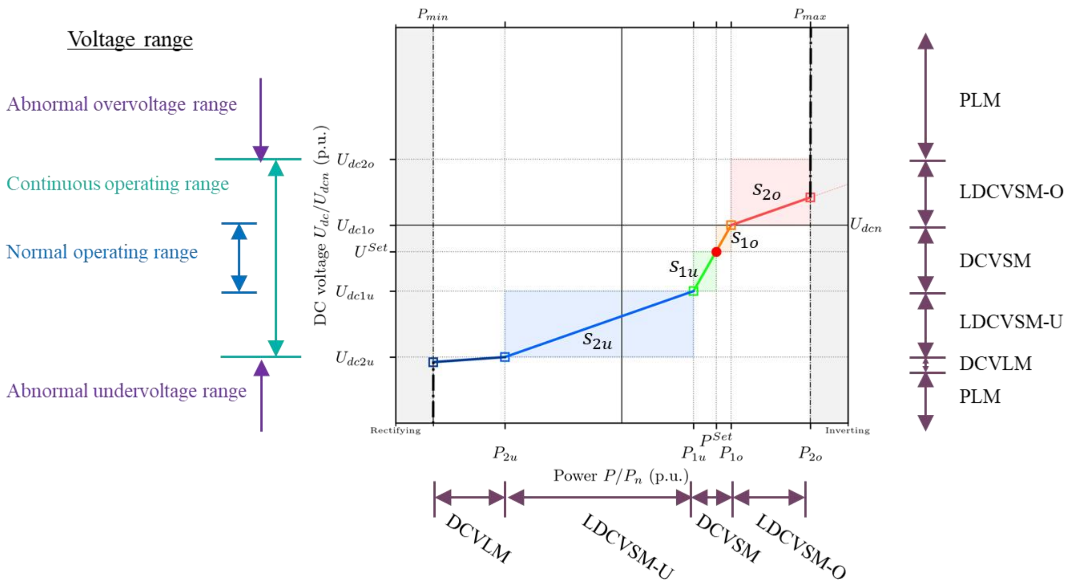


FIGURE 26: Example depiction of typical droop characteristic of an AC/DC converter station or unit in each primary DC voltage control related mode.

Each of these modes shall be defined with specific capability requirements, which are illustratively described in the form of droop characteristics, and associated parameters detailed in the subsequent sections, along with the dynamic requirements outlined in Section 6.6.

The priority of these modes and other AC side functionalities, such as FSM and LFSM-O/U, as well as the conditions under which blocking of these functionalities is permitted, shall be determined by the system operator in coordination with the relevant TSOs, if applicable.

[14] The DCVLM serves as a security backup, depending on other mode parameter selections (e.g., the LDCVSM setting reaching the power limit before reaching the voltage limit). If the converter depletes all available headroom capacity, the DCVLM cannot be activated and, consequently, does not appear in the multi-segment droop characteristic. For an alternative definition of DCVLM, please refer to Section 9.3.

6.5.3.1 DC Voltage Sensitive Mode (DCVSM)

When operating in DCVSM, the AC/DC converter station or unit shall be capable of responding to DC voltage deviation in the connected HVDC system as indicated in **FIGURE 27** and in accordance with the parameters detailed in **TABLE 10** and

TABLE 11. These parameters shall be specified by the system operator within the ranges predefined for each parameter.

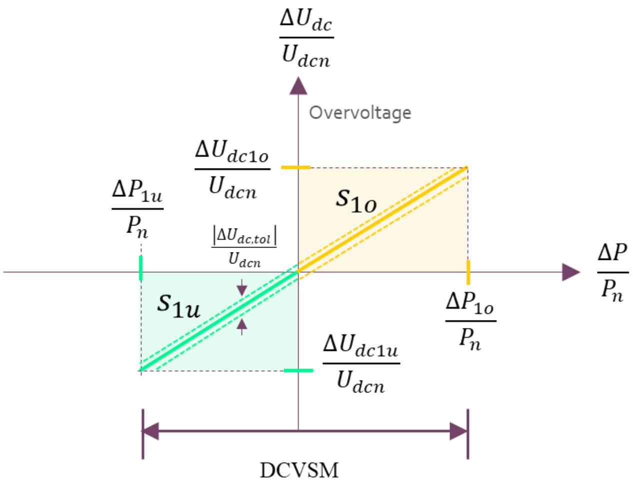


FIGURE 27: Droop capability of an AC/DC converter station or unit in DCVSM.

TABLE 10: Definitions of basic parameters and variables used for defining active power voltage response in DCVSM.

Variables	Definitions	Unit
U_{dcn}	nominal voltage of the DC network for which the DCVSM service is provided	kV
P_n	nominal active power	MW
P_{max}	agreed maximum power defined for the connection point of the converter station or unit	MW
P_{min}	agreed minimum power defined for the connection point the converter station or unit	MW
U_{dc}^{Set}	DC voltage set-point at DC-PoC	kV
P^{Set}	active power set-point	MW
U_{dc1u}	undervoltage threshold value	kV
U_{dc1o}	overvoltage threshold value	kV
ΔP	change in active power by the AC/DC converter station or unit with respect to the present operating point	$\Delta P = P - P^{Set}$

ΔU_{dc}	voltage deviation of the DC network for which the DCVSM service is provided[15]	$\Delta U_{dc} = U_{dc} - U_{dc}^{Set}$

TABLE 11: Parameters for active power voltage response in DCVSM

Variables	Definitions	Unit
ΔP_{1u}	agreed power change at reaching the voltage threshold value ΔU_{dc1u}	MW
ΔP_{1o}	agreed power change at reaching the voltage threshold value ΔU_{dc1o}	MW
s_{1u}	droop at undervoltage	$\mathrm{p.u.}$
s_{1o}	droop at overvoltage	$\mathrm{p.u.}$
ΔU_{dc1u}	undervoltage deviation threshold value	$\Delta U_{dc1u} = U_{dc1u} - U_{dc}^{Set}$
ΔU_{dc1o}	overvoltage deviation threshold value	$\Delta U_{dc1o} = U_{dc1o} - U_{dc}^{Set}$
$\Delta U_{dc,\,db}$	deadband of the power voltage response	kV
$\Delta U_{dc,\,tol}$	voltage response insensitivity (permissible tolerance)	$\%$

The following provides a detailed description of the definition of each parameter.

Maximum and Minimum power limits P_{max} & P_{min}

The maximum and minimum power limits, denoted by P_{max} & P_{min}, are defined for the connection point of each converter station or unit by the relevant system operator.

Those values shall be the maximum and minimum continuous active power which the AC/DC converter station or unit can exchange with the AC network at each AC-PoC as defined in the connection agreement or as agreed with the relevant TSO[16]. It shall not be obligatory for the AC/DC converter station or unit to provide active power beyond these specified limits. Therefore, if the active power voltage response in DCVSM results in the maximum and minimum power limits being reached, active power shall be maintained at these limits.

[15] In AC systems, the frequency is a global variable. This means that any frequency deviation Δf is formally defined as the deviation from the nominal frequency f_n, i.e. $\Delta f = f - f_n$. In a steady state, the frequency deviation is the same at all local measurements throughout the system. Conversely, the voltage in DC system is not a universal variable. Instead, in steady-state, the voltage at each node varies due to line resistance and other factors causing voltage drops. As a result, the DC voltage deviation measured at any given converter unit must be relative to the converter's own DC voltage set-point, i.e. $\Delta U_{dc} = U_{dc} - U_{dc}^{Set}$. When a converter under droop control is operating without any deviation of power, i.e. $\Delta P = 0$, it implies a condition where the voltage deviation equals zero ($\Delta U_{dc} = U_{dc} - U_{dc}^{Set} = 0$).

[16] Here, the adoption of AC power at the AC-PoC is assumed due to its direct relevance for the TSOs. However, the adoption of DC power shall not be excluded. For further details, refer to Section 6.5.2.

Undervoltage/Overvoltage threshold values U_{dc1u} & U_{dc1o}

The undervoltage and overvoltage threshold values, denoted by U_{dc1u} & U_{dc1o}, are defined as the system level values consistent for all AC/DC converter stations or units within the DC grid. Within the voltage range defined by those two values, the AC/DC converter station or unit in DCVSM must fulfil the functional requirement in accordance with the parameters specified by the system operator.

It is recommended to establish the system level common under and over DC voltage threshold values U_{dc1u} & U_{dc1o}, which are consistent across all AC/DC converter units and do not change depending on the power flow conditions [17]. This approach allows to standardize the response to voltage deviations, ensuring a consistent and predictable operational framework for the entire grid. Then, the DC voltage deviation threshold values are defined with respect to the system level DC voltage threshold values as follows:

- $\Delta U_{dc1o} = U_{dc1o} - U_{dc}^{Set}$ is the upper DC voltage deviation threshold below which the AC/DC converter station or converter unit must provide the DCVSM response according to the parameters specified for overvoltage, and
- $\Delta U_{dc1u} = U_{dc1u} - U_{dc}^{Set}$ is the lower DC voltage deviation threshold above which the AC/DC converter station or converter unit must provide the DCVSM response according to the parameters specified for under voltage.

The implications of the above definitions in the DC voltage droop characteristic plane are illustrated in the **FIGURE 28**.

From a technical standpoint, those voltage threshold values can be established independently of the static DC voltage ranges defined in Section 6.2.1. However, it is a common practice in AC systems to align the FSM and LFSM threshold frequencies with the maximum steady-state frequency deviation of the system[18]. Therefore, in accordance with the customary practice of AC systems, it is advisable to align those voltage thresholds values with the voltage levels that define the static DC voltage range. This suggests that $[U_{dc1u}, U_{dc1o}] = [U_{min}^{Nor}, U_{max}^{Nor}]$. Consequently, the range of DC voltage within which the DCVSM is required to provide specified responses corresponds directly to the normal operating DC voltage range.

It shall be noted, however, that in a sparse and/or radial DC grid, particularly with long-distance transmission lines, there may be instances where the same voltage thresholds cannot be applied to all converter stations, necessitating the definition of specific voltage threshold levels for particular stations.

[17] The droop characteristic of a given converter varies vertically in accordance with the designated U_{dc}^{Set}, which can vary during the operation depending on the power flow condition. Therefore, from the TSO's point of view, if DCVSM thresholds are specified with respect to "deviation", it means that each converter will transition the control modes at different grid voltage levels, depending on its pre-contingency power flow condition. To circumvent this and ensure uniformity across the grid, establishing the system level common under and over DC voltage threshold values U_{dc1u} & U_{dc1o} is recommended such that it is consistent across all AC/DC converter stations or units and do not change depending on the power flow conditions.

[18] Article 15 of SOGL specifies the maximum steady-state frequency deviation of the synchronous areas. According to ENTSO-E guideline document, droop for FSM should be calculated to make sure the reserve power capacity could be fully deployed for the synchronous area reference frequency deviation (i.e 200 mHz for CE, 500 mHz for GB).

As the DC grid evolves and becomes more developed and meshed in the future, the need for such specific voltage thresholds may decrease.

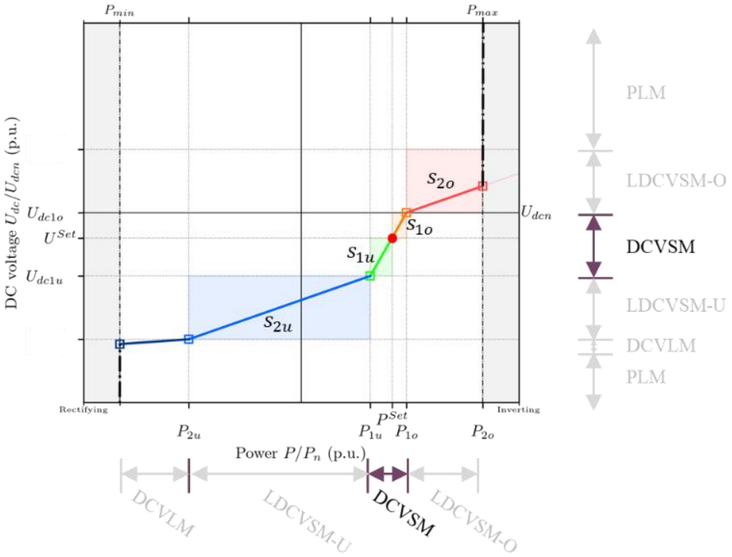


FIGURE 28: Illustration of the implications of the definitions of undervoltage and overvoltage DC voltage threshold values in the DC voltage droop characteristic.

Droop s_{1u} & s_{1o}

AC/DC converter stations or units should have the capability of implementing the droop settings for DCVSM.

The droop s_{1u} & s_{1o} are parameters specifying the expected characteristic in the DCVSM. Selecting the appropriate droop parameter is at the discretion of the system operator. It is indispensable that AC/DC converter stations or units possess the capability of implementing the droop setting for DCVSM. Nevertheless, the application of this capability can vary significantly depending on the operational context of the system, as evidenced in the practice of AC systems[19]. The following further elucidates the implications of these different contexts and provide corresponding recommendations.

Neglecting the deadband, the droop for overvoltage can be expressed by:

[19] For Frequency Sensitive Mode (FSM), the AC system counterpart of the DCVSM, NC-HVDC Annex II.1.1.(c) stipulates that HVDC systems must possess the capability of adjusting the droop for upward and downward upon an instruction from the relevant TSO. In practice, whether the droop for FSM is fixed over its entire exploitation period or changed regularly depends on the operational context, and both are prevailing practice. For the former, the droop is determined in the initial contractual agreement and remains fixed until this contractual agreement is renewed. In the latter case, the droop is considered as a variable that ensures the provision of FCR (Frequency Containment Reserve) services. For a practical example, please refer to . Thus, the droop setting is regularly adjusted based on the portfolio of the balance responsible party and the outcomes of FCR market auctions. Theoretically, this means that the actual droop could potentially be modified every dispatch cycle.

$$s_{1o} = \frac{\frac{\Delta U_{dc1o}}{U_{dcn}}}{\frac{\Delta P_{1o}}{P_n}} \text{ [p.u.]}$$

Here, ΔU_{dc1o} is the overvoltage threshold value, s_{1o}, is the droop for overvoltage, and ΔP_{1o} is the agreed power deviation at reaching the voltage threshold value. The equation indicates that only two of the parameters ΔU_{dc1o} , s_{1o} , and ΔP_{1o} can be independently chosen, as the remaining parameter is determined as a consequence of the other two. **FIGURE 29** illustrates the relation between the three parameters.

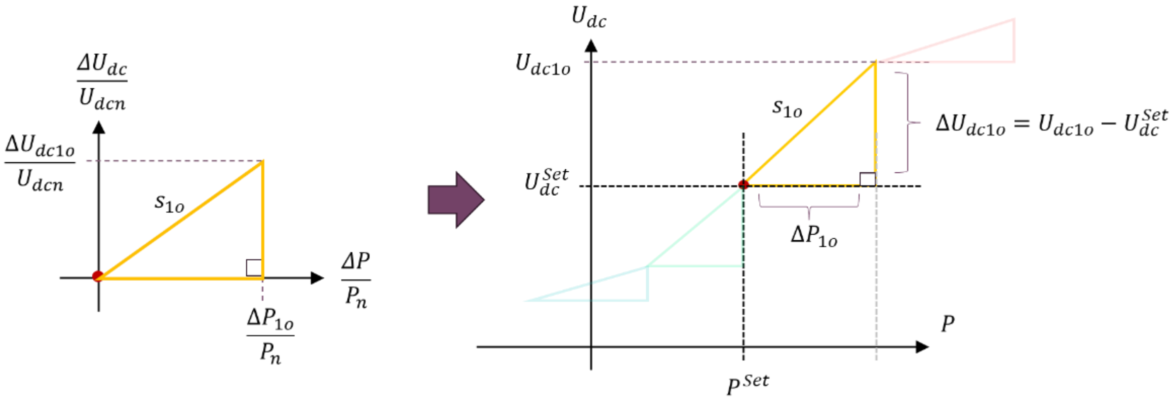


FIGURE 29: Inherent relationship between the parameters.

Given that ΔU_{dc1o} is determined by the system level DC voltage deviation threshold value, the different operational contexts can be effectively reduced to prioritizing either droop s_{1o} or power deviation ΔP_{1o}.

From the above reflection, two distinct operational contexts for the DCVSM are possible within the functional framework, namely, basic and advanced options. The choice between the basic and advanced options should be made by the system operator, considering factors such as the size of the grid and the number of converter units within the system, as well as the impact on the interconnected AC systems.

Basic option: In this option, priority is given to the droop. The droop for each AC/DC converter station or unit is fixed and is not frequently adjusted, even when operating set-points change. The droop values determine the distribution of disturbance power between converters in steady state, which shall be agreed upon and may be updated (e.g., seasonally) to reflect the changing conditions of the connected AC grids. The trade-off for this option is that the power deviation at reaching the DC voltage threshold values is no longer specifiable.

Advanced Option: In this option, the power deviation at reaching the voltage threshold is prioritized over droop. Here, the assigned quantity of power is considered a specifiable attribute for the overall system management, analogues to FCR service provision in AC systems. The droop settings of each unit are adjusted to ensure the provision of the agreed power. The droop can be theoretically updated at every dispatch cycle.

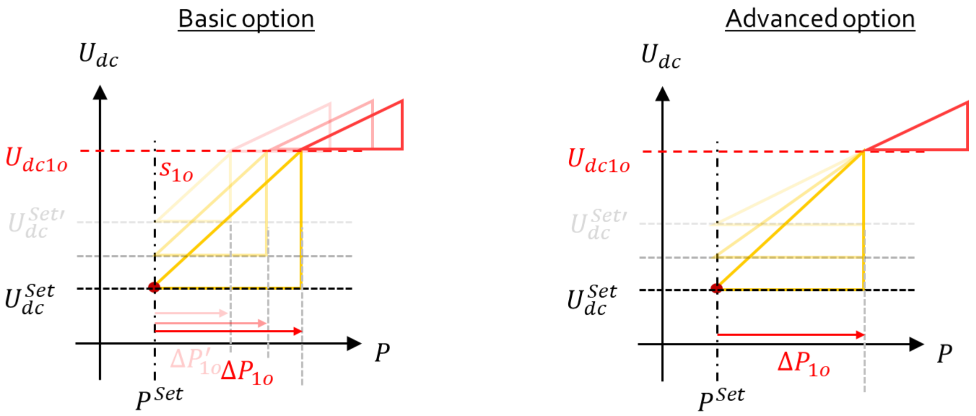


FIGURE 30: Illustrative representation contrasting the basic and advanced options, highlighting their respective impacts of the change in DC voltage setpoint and active power setpoint.

FIGURE 30 illustratively depicts the relationship between droop and the power deviation at reaching the voltage threshold in each option, highlighting their distinct impacts those options have on the change in DC voltage setpoint. In the basic option, the amount of power contribution at reaching the voltage threshold U_{dc1o} is determined by the voltage setpoint and the specified droop gain, indicating that the extent of the contribution of the AC/DC converter station or unit to maintaining the voltage within the normal operating range varies depending on the DC voltage setpoint. Conversely, in the advanced solution, the droop settings are adjusted to ensure the provision of the agreed-upon active power contribution when reaching U_{dc1o}. Ultimately, the selection between the basic and advanced options depends on the operator's assessment of the grid's needs. The primary advantage of the basic option lies in its simplicity, coupled with reduced communication and reliability issues. This benefit holds true irrespective of the grid's size. While the advanced option may allow for a more flexible system operation, it requires more sophisticated management and control systems capable of handling frequent droop adjustments.

Deadband & Insensitivity

The HVDC system owner and the relevant system operator, in coordination with the relevant TSO may agree on the implementation of deadband for DCVSM in the AC/DC converter stations or units and the capability of adjusting the deadband settings for DCVSM. The insensitivity of active power voltage response for DCVSM should be less than the value specified by the system operator.

Definitions:

Deadband: refers to an interval centred around the set-point. This is used intentionally to make the DC voltage control unresponsive.

Insensitivity: refers to an inherent feature of control system specified as the minimum change in the DC voltage or input signal that results in a change of output power or output signal.

If implemented, the deadband should be adjustable according to the operator's needs. While no stringent technical considerations mandating the implementation of the deadband have been identified, the deadband may be viewed as a means to provide additional flexibility for the system operator, potentially used to prevent undesirable interactions. It is important for the system operator to ensure that not every converter station in the system is set to operate with a deadband, since it is essential that at least one converter in the system must regulate the DC voltage.

Concerning insensitivity, this unintentional characteristic typically arises from the measurement accuracy. The system operator shall specify the reasonable upper limit for sensor accuracy requirements, while ensuring consistency with other functional specifications.

6.5.3.2 Limited DC Voltage Sensitive Mode-Overvoltage (LDCVSM-O)

In addition to the requirements of DCVSM, the following shall apply with regard to LDCVSM-O. The AC/DC converter station or unit shall be capable of responding to DC voltage deviation in the connected DC grid according to **FIGURE 31** and the parameters detailed in **TABLE 10** and **TABLE 12**. These parameters shall be specified by the system operator within the ranges defined for each parameter.

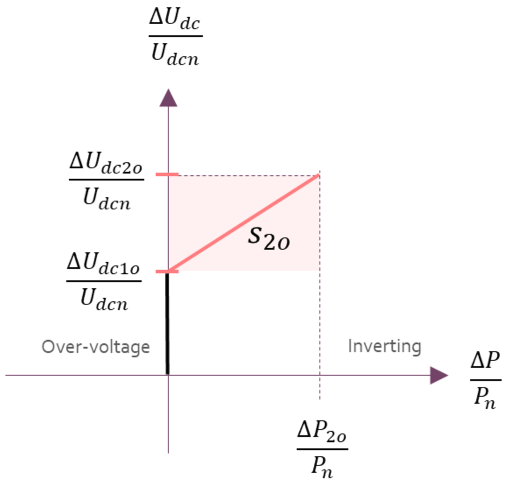


FIGURE 31: Droop capability of an AC/DC converter station or unit in LDCVSM-O.

TABLE 12: Parameters for active power voltage response in LDCVSM-O.

Variables	Definitions	Unit
ΔP_{2o}	agreed power change at reaching the voltage threshold value ΔU_{dc2}	MW
s_{2o}	droop at overvoltage	p.u.
U_{dc1o}	overvoltage threshold value that triggers LDCVSM-O	kV
U_{dc2o}	overvoltage level below which the AC/DC converter or unit shall adjust the active power according to the parameters specified for LDCVSM-O	kV

Overvoltage level U_{dc2o}

The overvoltage level, denoted by U_{dc2o}, is defined as the DC voltage value consistent for all AC/DC converter stations or units within the DC grid. Below this level, the AC/DC converter station or unit in LDCVSM-O must fulfil the functional requirement in accordance with the parameters specified by the system operator.

The parameters specified for LDCVSM-O applies the voltage range defined by this U_{dc2o} and the previously established overvoltage threshold value U_{dc1o}. The LDCVSM-O is triggered upon detecting an overvoltage that surpasses the threshold U_{dc1o} and is required to provide active power adjustment up to ΔP_{2o} or the specified maximum power limit. This shall be executed up to the voltage level U_{dc2o}.

Similarly to the DCVSM, this voltage level can be established independently from those defining the static DC voltage ranges defined in Section 6.2.1. However, following the convention in AC systems, it is recommended that this voltage level to be aligned with the maximum continuous DC voltage limit, i.e. $[U_{dc2O}] = [U_{max}^{Cont}]$. This implies that the AC/DC converter station or unit in LDCVSM-O shall provide the specified response up to the maximum limit of the continuous operating DC voltage range.

Droop s_{2o}

AC/DC converter stations or units should have the capability of implementing the droop settings for LDCVSM-O.

The droop for LVSM-O can be mathematically expressed in a slightly different form compared to the case with DCVSM:

$$s_{2o} = \frac{\frac{\Delta U_{dc2o} - \Delta U_{dc1o}}{U_{dcn}}}{\frac{\Delta P_{2o}}{P_n}} = \frac{U_{dc2o} - U_{dc1o}}{\Delta P_{2o}} \frac{P_n}{U_{dcn}} \; [\mathrm{p.u.}]$$

Here, $U_{dc2o} - U_{dc1o}$ is the difference between the system level overvoltage threshold value for LDCVSM-O and that of DCVSM, s_{2o}, is the droop in LDCVSM-O, and ΔP_{2o} is the power deviation at reaching the voltage threshold value for the LDCVSM-O. The equation above indicates that, owing to the previously established system level voltage threshold values, the degree of freedom in selecting parameters in the LDCVSM-O is governed by a more stringent triangulation relationship. This relationship differs from the case in the DCVSM, where the influence of the voltage setpoint remains unavoidable. By the principle of droop, only two of the parameters $U_{dc2o} - U_{dc1o}$, s_{2o}, and ΔP_{2o} can be independently chosen, as the remaining parameter is determined as a consequence of the other two.

Given that U_{dc2o} is to be determined as the system level DC voltage, and thus $U_{dc2o} - U_{dc1o}$ is a fixed value, two different operational contexts namely, basic, and advanced option can be considered, as previously introduced.

Basic option: In this option, priority is given to the droop over the power level. The droop for each AC/DC converter station or unit is fixed and is not frequently adjusted. The trade-off for this option is that the power deviation at reaching the overvoltage level ΔP_{2o}, which is indeed subject to the limitation of the available converter headroom, cannot be considered as a specifiable parameter.

Advanced Option: In this option, the power deviation at reaching the voltage threshold is prioritized over droop. Here, the assigned quantity of power designated for the LDCVSM-O is considered as a specifiable parameter. Subject to the constraint by the available headroom capacity of the converter, the system operator can adjust the desired power deviation at reaching the overvoltage level, ΔP_{2o}, to ensure the DC voltage security of the HVDC system, as well as the AC system security, especially when there is a congestion. The droop can, in theory, be updated at every dispatch cycle.

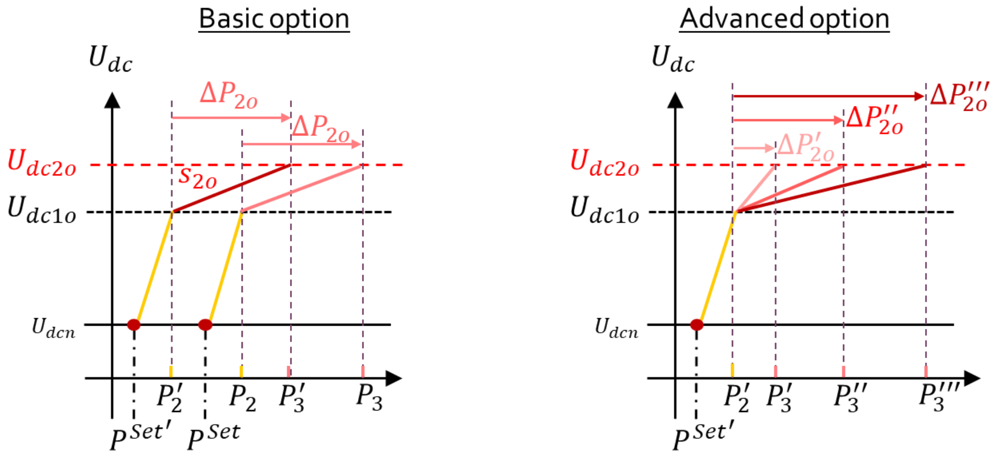


FIGURE 32: Illustrative representation contrasting the basic and advanced options in LDCVSM-O.

FIGURE 32 illustratively shows the implication associated with the two options. In the basic option, where the droop is fixed, there is no degree of freedom, and as long as it remains within the available headroom capacity, its droop contribution before reaching the voltage level U_{dc2o} is always fixed at the value determined by the assigned droop for LDCVSM. Therefore, the droop must be meticulously chosen to ensure the capability of coping with any ordinary contingencies when operating at any possible operating power set-point. In contrast, in the advanced option, the droop is determined in order to adjust the amount of contribution of the power at reaching the voltage level U_{dc2o} within the availability of the headroom capacity. Again, ultimately, the selection between the basic and advanced options depends on the operator's assessment of the grid's needs.

6.5.3.3 Limited DC Voltage Sensitive Mode Undervoltage (LDCVSM-U)

In addition to the requirements of DCVSM and LDCVSM-O, the following shall apply regarding LDCVSM-U. The AC/DC converter station or unit shall be capable of responding to DC voltage deviation in the connected DC grid according to **FIGURE 33** and the parameters detailed in **TABLE 10** and **TABLE 13**. These parameters shall be specified by the system operator within the ranges defined for each parameter.

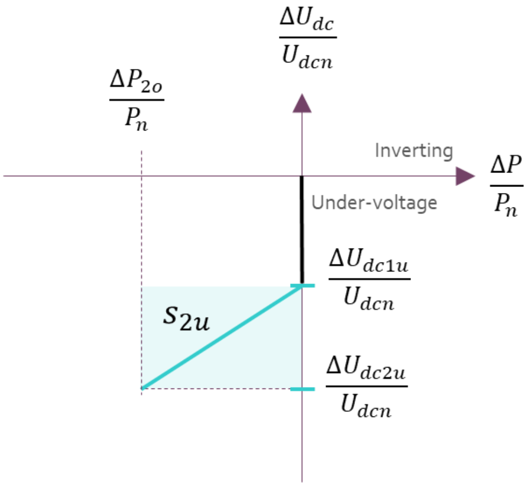


FIGURE 33: Droop capability of an AC/DC converter station or unit in LDCVSM-U.

TABLE 13: Parameters for active power voltage response in LDCVSM-U

Variables	Definitions	Unit
ΔP_{2u}	agreed power change at reaching the voltage level ΔU_{dc2u}	MW
s_{2u}	droop at undervoltage	$\mathrm{p.u.}$
U_{dc1u}	undervoltage threshold value that triggers LDCVSM-U	kV
U_{dc2u}	undervoltage level above which the AC/DC converter or unit shall adjust the active power according to the parameters specified for LDCVSM-U	kV

Undervoltage level U_{dc2u}

The undervoltage level, denoted by U_{dc2u}, is defined as the system level value consistent for all AC/DC converter stations or units within the DC grid. Above this level and below U_{dc1u}, the AC/DC converter station or unit in LDCVSM-U must fulfil the functional requirement in accordance with the parameters specified by the system operator.

The parameters specified for LDCVSM-U applies the voltage range defined by this U_{dc2u} and the previously established under threshold value U_{dc1u}.

The LDCVSM-U is triggered upon detecting an undervoltage that surpasses the threshold U_{dc1u} and is required to provide active power adjustment down to the specified maximum power limit.

Similarly to the LDCVSM-O, it is recommended that this voltage level to be aligned with the minimum continuous DC voltage limit, i.e. $[U_{dc2u}] = [U_{min}^{Cont}]$. This implies that the AC/DC converter station or unit in LDCVSM-U shall provide the specified response down to the minimum limit of the continuous operating DC voltage range.

Droop s_{2u}

AC/DC converter station or units should have the capability of implementing the droop settings for LDCVSM-U.

Similarly, to LDCVSM-O, the droop for LDCVSM-U can be mathematically expressed as:

$$s_{2u} = \frac{\frac{\Delta U_{dc1u} - \Delta U_{dc2u}}{U_{dcn}}}{\frac{\Delta P_{2u}}{P_n}} = \frac{U_{dc1u} - U_{dc2u}}{\Delta P_{2u}} \frac{P_n}{U_{dcn}} \; [\mathrm{p.u.}]$$

Here, $U_{dc1u} - U_{dc2u}$ is the difference between the system level under threshold value and the LDCVSM-U undervoltage level, s_{2u} is the droop for LDCVSM-U, and ΔP_{2u} is the power deviation at reaching the voltage threshold value for the LDCVSM-U. Since U_{dc2u} is to be determined as the system level DC voltage, and thus $U_{dc1u} - U_{dc2u}$, the same, basic, and advanced options can also be considered, as previously introduced.

6.5.3.4 DC Voltage Limiting Mode (DCVLM)

In addition to the requirements of DCVSM, LDCVSM-O, and LDCVSM-U, the following shall apply with regard to DCVLM. The AC/DC converter station or unit shall be capable of responding to DC voltage deviation in the connected DC grid according to **FIGURE 34** and the parameters detailed in **TABLE 10** and **TABLE 14**. These parameters shall be specified by the system operator within the ranges defined for each parameter.

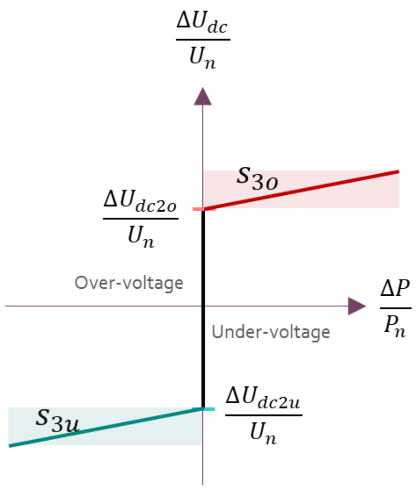


FIGURE 34: Droop capability of an AC/DC converter station or unit in DCVLM.

TABLE 14: Parameters for active power voltage response in DCVLM.

Variables	Definitions	Unit
s_{3o}	droop at overvoltage	$\mathrm{p.u.}$
s_{3u}	droop at undervoltage	$\mathrm{p.u.}$
U_{dc2o}	overvoltage threshold value that triggers DCVLM	kV

U_{dc2u}	undervoltage threshold value that triggers DCVLM	kV

Activation of DC Voltage Limiting Mode

DC Voltage Limiting Droop Mode shall be activated when detecting the voltage exceeding the overvoltage level U_{dc2o} and similarly below the undervoltage level U_{dc2u}.

The parameters specified for DCVLM applies the abnormal voltage range above the previously defined overvoltage level U_{dc2o} and below undervoltage level U_{dc2u}.

The DCVLM is triggered upon detecting an overvoltage that surpasses the threshold U_{dc2o} or an undervoltage below U_{dc2u}.

Expected roles of DC Voltage Limiting Mode

This mode is activated following the full engagement of the LDCVSM-O or -U. Whether the entire reserve capacity is depleted before exceeding U_{dc2o} or U_{dc2u} depends on the selected parameters and the pre-contingency operating conditions. The DCVLM becomes relevant only in the scenarios where the LDCVSM-O or -U of an AC/DC converter station or unit does not deplete all available headroom capacity before reaching the voltage threshold values, implying the potential to evacuate or inject more power.

When the excursions of the DC voltages surpass the thresholds, U_{dc2o} or U_{dc2u}, the AC/DC converter stations or units with available capacity are expected to contribute up to their maximum or minimum power limits. In instances where more than one converter is capable of additional power injection/evacuation, a power sharing mechanism is needed to prevent conflicts arising from simultaneous voltage control by multiple converters (Such as multiple converters in fixed DC voltage control mode inadvertently work against each other.)

DCVLM is designated to address such situations. Upon activation, an AC/DC converter station or unit is expected to contribute to the voltage containment until it exhausts its maximum or minimum capability in accordance with the specified parameters.

Droop of DC Voltage Limiting Mode s_{3o} & s_{3u}

Given that the primary objective of this mode is to contain abnormal voltage excursion that falls outside of the continuous operating range, the droop of this mode is naturally set to be low.

As this mode serves as an emergency measure for the system operation, it should be designed to provide a robust and reliable response. Therefore, altering the control configuration related to this mode after commissioning should not be considered.

Alternative DCVLM definition

An alternative definition of the DCVLM offers a different perspective for specifying the capability requirements of this control mode and addresses the different needs of AC/DC converter operation. For a detailed explanation on this alternative DCVLM definition, readers are encouraged to refer to Section 9.3.

6.5.3.5 Power Limiting Mode (PLM)

In addition to the requirements of DCVSM, LDCVSM-O, LDCVSM-U, and DCVLM, the following shall apply regarding PLM. The AC/DC converter station or unit shall be capable of protecting itself from reaching its capability limits during transient and limiting the power to the maximum and minimum power limits P_{max} & P_{min} in steady state.

Expected roles of Power Limiting Mode

P_{max} and P_{min} are the maximum and minimum active power which the AC/DC converter station or unit can continuously exchange with the network at each connection point as specified in the connection agreement or as agreed with the relevant system operator. On the other hand, power capability limits are design parameters dependent on the manufacturer.

In steady state, power should be confined within P_{max} and P_{min}. During dynamic time range, power should not reach the capability limits of the converter.

The implementation of the scheme and the dynamic characteristics of this mode are subject to the discretion of the converter manufacturer.

6.5.4 Necessary considerations for dynamic requirements of primary DC voltage control

In the previous section, static requirements for the primary DC voltage control related control modes, which define their static bahavior, were presented. In the event of a disturbance, the parameters specifying those static behavioral characteristics uniquely determine the post-contingency equilibrium state of the system. However, they do not determine the dynamic behavior of the system, nor do they guarantee the system stability.

In the context of multi-vendor multi-terminal HVDC systems, the applicable methods, required inputs, and constraints for conducting preliminary design studies would be significantly different from those of turnkey Point-to-Point (PtoP) HVDC projects delivered by a single vendor. In such a system, although it is ultimately imperative to assess overall system security and ensure the absence of interoperability issues through comprehensive system-level tests in an integrated testing environment –incorporating all C&P systems together with detailed representation of the entire HVDC system equipment and adjacent AC systems in a real-time simulation framework– it is equally important to facilitate the integration process and minimize the interoperability risks by establishing standardized DC side dynamic performance requirements upfront. This also implies setting clear expectations for the performance of each AC/DC converter station. Achieving this, however, requires addressing several key considerations.

6.5.4.1 General System Expectations for Primary DC voltage Control

The consensus on the general expectations among TSOs for the primary DC voltage control and the corresponding definition of the system-level DC voltage ranges are outlined below:

In the event of the identified worst-case scenario (for instance, the maximum sudden loss of infeed or load), the DC voltage at any node within the system shall be maintained within the predefined system-level DC voltage parameters outlined in Section 6.2, which entails:

- Ensuring that the post-contingency steady-state voltages at any system node remain within the continuous operating DC voltage range,
- Limiting the dynamic voltage overshoot exceeding the continuous operating DC voltage range to no more than the value specified as a percentage of the nominal voltage,
- Ensuring that any oscillations to be settled within T_{max}^{Dyn}, and
- Preventing the primary DC voltage control from triggering any unintentional protective actions of any equipment during such events.

In addition,

- Converters with the same droop parameter equally contribute dynamically to the extent feasible, provided they are equidistant electrically from the source of the event and connected to AC networks with respective similar grid strength.
- The primary DC voltage control shall not render the system unstable in any circumstance.
- Accessibility to all relevant parameters, deemed necessary and mutually agreed upon for ensuring system stability and future expandability.

The relevant TSO is responsible for selecting all static parameters as detailed in Section 6.5.3, which theoretically define the "***Static***" characteristics of the system under a given disturbance. However, as illustrated in Section 9.4, even when two stations have identical droop settings, variations in droop control implementations can lead to significant differences in their dynamic behavior. These differences affect key parameters such as response time, damping, and stability margins. This demonstrates that droop settings alone do no not dictate the dynamic response of the converter, and consequently, the overall system dynamics.

This implies that the dynamic characteristics of the overall system cannot be ascertained until the integrated testing environment is established, incorporating the actual control solution of each vendor altogether. As a first mitigation step, it is imperative for the system operator to establish standardized "dynamic performance requirements for individual AC/DC converter stations" upfront. These requirements must be adhered to by each converter manufacturer in their controller design.

A viable approach is to adhere to established formal definitions, such as those provided by IEC for step response and ramp response. For instance, IEC IEV 351-46-12 “reference-variable response of the control system” [14] defines the set of parameters that describes the dynamic response of a system. The definition involves the step response of a control system, triggered by the application of a step function to one of the input variables, as well as dynamic response to exogenous events, such as disturbances.

Alignment to such formal definitions could offer a fundamental basis for evaluating dynamic performance and ensuring consistency across AC/DC converter stations in multi-vendor systems.

6.5.4.2 General description of dynamic requirements for primary DC voltage related control modes

The system operator shall establish a comprehensive specification with which the dynamic response of the AC/DC converter station or unit must comply. In the absence of a standardized specification methodology for DC-side control dynamics, several different approaches for dynamic performance specification can be considered, including, but not limited to:

- Step Voltage Reference Response
- Step Power Disturbance Response
- Step Voltage Disturbance Response
- Step Power Reference Response[20]

According to IEV 351-46-12 (reference-variable response of the control system) [14] and IEV 351-46-13 (disturbance response of the control system) [15], a set of parameters is defined to describe the dynamic characteristics of a closed-loop feedback control system. Building upon these definitions, the dynamic performance requirements specification should include, but are not limited to, the following parameters, with their graphical representation provided in **FIGURE 39** and **FIGURE 41**:

- Steady-state deviation Δx_{∞}
- Overshoot x_m
- Control rise time T_{cr}
- Control settling time T_{cs}
- Specified tolerances $\Delta \mathrm{x}_s$

The implications of these parameters may vary depending on the respective specification approach outlined above.

In addition, to ensure the overall system stability, AC/DC converters must provide sufficient damping when interfaced with various grid configurations under different operating points, while meeting the specified dynamic performance requirements.

The following section provides an in-depth discussion of the rationale behind these specification approaches.

6.6 Performance requirements and recommendation of behavioral specification procedure

The dynamic behavior of an HVDC system is inherently complex, as it is influenced by the dynamic characteristics and interactions of all its subsystems. To meet the overall system stability and reliability expectations of the overall HVDC system, each AC/DC converter station or unit within the system must possess specific performance capabilities. These capabilities are influenced by both their physical design parameters (e.g., inductor and capacitor sizes) and control design parameters (e.g., proportional and integral gains).

However, the actual dynamic behavior also depends on the control architecture of the control scheme, which may vary between manufacturers, as well as on the connected AC system dynamics. Consequently,

[20] Article 12 of NC HVDC specifies the active power controllability, including the control range and ramping rate requirements at AC-PoC. In the context of a DC grid, assessment of the behavior of power at DC-PoC is equally important and is therefore considered here.

the dynamic characteristics of an AC/DC converter station or unit cannot be fully defined by design specifications alone. Instead, they must be defined as behavioral specifications, which are subject to assessment under specific environment and evaluated against specified criteria.

This approach aligns with established practice in AC systems[21]. Behavioral specifications are essential because they capture real-world interactions and dynamic responses that design specifications alone may not predict, especially when integrating converters from multiple vendors.

This section aims to provide a clear and transparent description of the general framework for the DC side behavioral specification and their evaluation procedure. Along with the various possible options and their respective advantages and disadvantages, it provides preliminary recommendations.

6.6.1 HVDC system stability classification

In alignment with the conventions in AC systems, the dynamic expectations of an HVDC system can be broadly classified into **large-disturbance stability** and **small-disturbance stability** [16]. These classifications are made to streamline the following discussions and are not intended to serve as rigid standards. It is anticipated that they will be refined and adapted as experience and developments in HVDC systems evolve.

Large-disturbance stability:

In general terms, large-disturbance stability refers to the ability of a system to maintain stable operation following significant disturbances. When applied to DC systems, it can be understood as the system's ability to maintain the voltages after relatively large disturbances, such as DC faults, the loss of AC/DC converter station or unit, circuit contingencies, or intentional change in power for ancillary services. To ensure large disturbance stability of the system, each AC/DC converter station or unit must possess adequate dynamic performance capabilities, aligned with the functional requirements, to cope with worst-case disturbance scenario in the system for the given converter.

Small-disturbance stability:

Small-disturbance stability, also known as small-signal stability, is a common concern across all types of systems. It refers to the system's ability to remain stable when subjected to small disturbances. It is typically related to inadequate damping of oscillations or undesired control interactions. For analytical purposes, linearization of the system under consideration is generally acceptable. To ensure small-disturbance stability, each AC/DC converter station or unit must provide sufficient damping when interfaced with various grid configurations under different operating points. This must be accomplished without compromising the fulfilment of the dynamic performance requirements.

Dynamic performance requirements for large-disturbance stability:

[21] For example, VDE-AR-N 4131 specifies the functional requirement for dynamic AC voltage control by stating "*The control behaviour shall be evaluated based on a step change of the voltage at the connection point*." It also provides the associated dynamic performance evaluation metrics. Additionally, it assigns the responsibility to the system operator to predefine the network short-circuit impedance for the evaluation.

For large-disturbance stability, the **dynamic performance requirements** for the AC/DC converters must be specified. These requirements are typically aligned with corresponding functional requirements. In the context of DC systems, ensuring large-disturbance stability requires a focus on performance requirements associated with the converter control modes, such as DC voltage droop control. Compliance to the specified dynamic performance requirements shall be evaluated in an adequate environment, which should include clearly defined criteria and evaluation methods.

Stability performance requirements for small-disturbance stability:

For small-disturbance stability, the **stability performance requirements** for AC/DC converters must also be thoroughly evaluated to ensure the absence of any undesired contribution to the small-signal instability. In AC systems, harmonic stability requirements are traditionally assessed through harmonic stability studies. For DC systems, similar practical stability performance requirements can be established, tailored to account for the absence of fundamental frequency. These aim to minimize the risk of undesired control interactions and oscillatory behaviors, ensuring that the system remains stable under various operating conditions.

6.6.2 Scope definition for MV-MTDC system design & testing framework

This section provides an overview of the design and testing framework for MV-MTDC systems. The key stages are referred to as the specification stage, the design stage, and the integration stage**.**

Throughout the project lifecycle, the MTDC system is developed, tested, and validated to meet the functional and performance requirements established during the **Specification stage**. In traditional point-to-point HVDC projects, compliance processes are divided into distinct phases: **Energization Operational Notification (EON)**, **Interim Operational Notification (ION)**, and **Final Operational Notification (FON)**. These phases outline compliance checkpoints critical for system approval and integration also relevant for Multi-terminal HVDC systems.

In the **Design stage**, each vendor conceptualizes and designs the C&P system for each converter to meet the dynamic and stability performance requirements specified by the relevant system operator or TSOs . To receive an **EON** from the relevant system operator or TSO, the HVDC system must demonstrate design-phase compliance with specified fundamental requirements. This stage includes initial design validations to confirm that core functional and safety criteria are met, aligning the system's capabilities with the grid's operational standards.

Following the design stage, the project advances to the **Integration Stage**. In this phase, all C&P systems from each vendor are integrated and subjected to coordinated testing. This stage encompasses a comprehensive assessment of all HVDC system equipment and components, validating their collective functionality and interoperability. All potential interactions between subsystems will be thoroughly assessed with high degree of certainty of each subsystem's behavior to ensure that the entire system performs as expected. Successful compliance in this phase allows the HVDC system owner to obtain an **ION**, authorizing subsequent system testing on site.

To achieve the final **FON**, the system must demonstrate compliance in actual operational conditions through on-site measurements and performance evaluations. This phase serves as the final compliance checkpoint, verifying that the HVDC system meets performance requirements compared to site measurements and certifying the system for operational integration into the system.

FIGURE 35 provides a conceptual overview of the general converter control system design and testing framework for MV-MTDC systems. While the flowchart remains general, it is specifically tailored to highlight aspects related to DC-side dynamic performance studies and harmonic stability studies in the design stage. As such, it may not fully capture other aspects not directly associated with them. The dashed line represents the additional interface required for constructing the DC grid from scratch, different from expanding the system, in alignment with the InterOPERA context.

For detailed complementary information on the specification stage, readers are encouraged to refer to InterOPERA deliverables D3.1 [17] and any forthcoming related deliverables. For the integration stage, please refer Deliverable D1.3 [18]. and future deliverables as they become available.

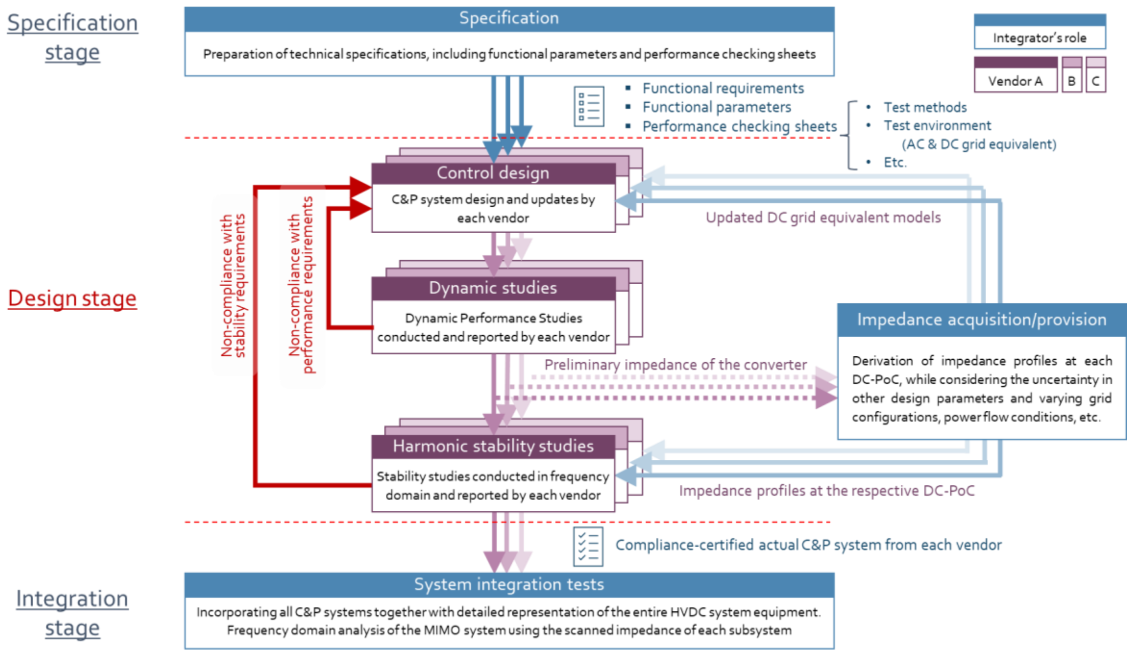


FIGURE 35 Overview of the general converter control system design and testing framework for MV-MTDC systems. For comprehensive details on the project phases and studies to be conducted in each stage, please refer to InterOPERA D1.3 [18].

The necessary specifications, comprehensively addressing the dynamic and stability requirements, must be provided to the vendors upfront to enable them to proceed independently with the C&P system design process in the design stage. The essential inputs for the design stage are, thus, the specified *functional requirements*, *functional parameters*, and *performance checking sheets*, which will be detailed in the subsequent section.

It is important to note that during this design stage, development is carried out independently. In multi-vendor MTDC projects, different vendors may simultaneously develop other sub-systems in parallel. This parallel development introduces an inherent uncertainty, as some critical design and control parameters of other subsystems that could have significant influence on the dynamic characteristic of the system remain unknown. This uncertainty must be mitigated through the careful formulation of dynamic performance specification and execution of harmonic stability studies. This is a particular challenge when constructing an MTDC grid from scratch, whereas it is less critical when expanding an existing DC grid.

The key steps within the design stage are as follows:

Control Design Step: During this stage, each vendor designs and updates their respective C&P systems.

Dynamic Performance Studies: This step involves conducting dynamic performance studies to evaluate compliance with the prescribed dynamic performance requirements, subject to the connection with the respective AC and DC grid equivalents introduced in Section 6.6.3.

Harmonic Stability Studies: Harmonic stability studies are carried out to assess the harmonic stability performance of individual AC/DC converter. The system operator or system integrator, in coordination with the relevant TSOs, shall provide frequency-dependent impedance profiles representing the DC grid as seen from the DC-PoC under a range of possible operational conditions. If necessary, these profiles are derived using the preliminary impedance profiles of converter stations, see **FIGURE 35**.

The respective specifications and their assessment through the studies depend on the scope of interest and the associated conditions on which these specifications and assessment are based, such as the range of frequency of interest. The detailed formulation of the dynamic performance requirements and harmonic stability requirements, along with the recommendations for the associated studies for their evaluations, are provided in the subsequent sections.

6.6.3 General workflow for compliance testing

This section outlines the general workflow for compliance testing in the design stage. In alignment with the practices in AC systems, the dynamic performance and stability requirements, along with their compliance testing procedures are structured through the so-called "**Performance Checking Sheet**"[22]. This practice is used by TSOs to validate the grid code compliance of an HVDC system connected to the transmission grid [19] [20]. This typically comprises the following elements: test objective, test environment, test methods, signals to be reported, and evaluation criteria.

Test objective

The test objective is a fundamental element of the performance checking sheet. For each test, the objective may differ depending on the specific performance aspects to be evaluated.

Test environment

For each test, it shall clearly specify what the DUT must be interfaced with at its AC-PoC and DC-PoC, respectively. The details of its AC and DC grid equivalents for each test shall be determined through the coordination between the system operator, in coordination with the relevant TSOs and the HVDC system owner. **FIGURE 36** illustrates an example of a general test environment, where the Device Under Test (DUT) considered is the positive pole converter unit of an AC/DC converter station. It should be noted that, in some tests, the DUT may also encompass both the positive and negative pole converter units.

[22] The term may vary and be referred to by another name depending on the TSO.

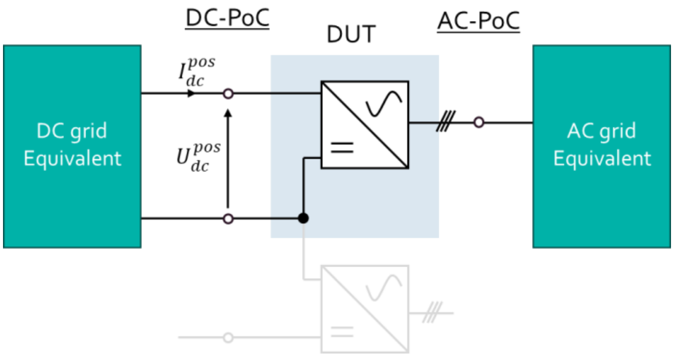


FIGURE 36 Illustrative depiction of test environment where the DUT considered is the positive pole converter unit of an AC/DC converter station

Test methods

The specific test methods should depend on the objectives of each test.

For dynamic performance studies, time-domain simulations shall be conducted. For harmonic stability studies, frequency domain analysis shall be conducted, and verified through time domain simulations.

Signals to be reported

The signals, as agreed upon between the vendor and TSO, must be monitored during the tests and reported.

Evaluation criteria

The evaluation criteria for each test shall be clearly defined and based on the technical requirements specified by the system operator and the relevant TSOs.

6.6.4 Dynamic performance requirements

This section outlines the detailed dynamic performance requirements specification for AC/DC converters and provides recommendations for the evaluation methodology. It discusses the possible procedures and the evaluation criteria that must be specified by the system operator in coordination with the relevant TSOs.

6.6.4.1 Dynamic performance studies framework

In the specification of dynamic performance requirements specification and their evaluation, there are two critical aspects to consider. This section outlines these aspects and provide a generalization of their implications.

Test environment for dynamic performance studies

To evaluate the functionality on the DC side, the AC grid equivalent can primarily be represented by an AC voltage source with appropriate SCRs and X/R ratio values. These parameters should be adapted to replicate the various AC grid conditions that the DUT may encounter during operation. The system operator, in coordination with the relevant TSOs, should specify these values to accurately reflect the AC grid characteristics at the AC-PoC.

On the other hand, unlike the well-established methods for representing the AC grid equivalent, there is currently no standardized approach for modelling the DC grid equivalent. This absence of a defined methodology allows for a range of possibilities, which remain subject to refinement based on experience and evolving best practices. The DC grid equivalent is expected to be sufficiently representative for evaluating the vendor's C&P system and capable of capturing the key properties of the DC grid to which it will connect, while also being simple and easily adjustable.

The appropriate equivalent representations may differ depending on the type of test and other relevant factors.

Given these considerations, the generalized test environment for dynamic performance studies is illustrated in **FIGURE 37**.

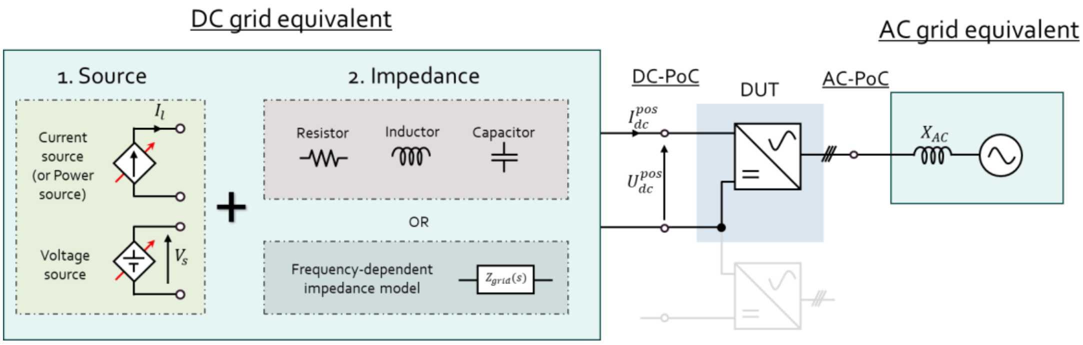


FIGURE 37 Generalized test environment for dynamic performance studies.

- Source element:

  One of the key aspects in defining the DC grid equivalent is the selection of the source element, which can be either a DC voltage source or a DC current (or power) source. This choice significantly impacts the observable dynamics during testing and the insights gained about DUT. Using a DC voltage source implies putting a primary focus on the DUT's ability to regulate current or power in response to changes in DC voltage at the DC-PoC. However, as the DC voltage is imposed by the source, the dynamic behavior of the DC voltage is suppressed by the source itself. This means that any fluctuations or variations in the DC voltages, which might occur under real operational conditions, cannot be fully assessed. Alternatively, the source element of the DC grid equivalent can be represented by a DC current or power source. This approach is useful for evaluating how the DUT manages voltage control response to changes in load, and its interaction with current or power disturbances.

- Impedance element:

The DC grid equivalent shall also include elements that replicate the impedance characteristics of the actual system as observed at the DC-PoC of the DUT. As confirmed in Section 9.5.1, DC grid impedance characteristics can vary significantly depending on the grid configuration and the design parameters of its subsystems. When constructing a grid from scratch, grid impedance characteristics are subject to high uncertainty. In this context, the findings in Section 9.5.1 are particularly relevant, as the most critical grid characteristics can be effectively captured by using two RLC combinations of a simple circuit, representing the highest and lowest DC grid stiffness. However, this remains subject to further refinement as more experience is gained in the future, and the use of more sophisticated DC grid equivalent model should not be excluded from consideration. In either case, the appropriate impedance values or profiles shall be specified by the system operator, in coordination with the relevant TSOs.

Test methods for dynamic performance studies:

According to the relevant dynamic performance requirements, appropriate test methods should be applied. Several plausible candidates exist for dynamic performance specifications and the associated compliance assessment methodologies. These are:

1. Step voltage reference response test
2. Step power disturbance response test
3. Step voltage disturbance response test
4. Step power reference response test[23]

Each of these methods serves to assess specific aspects of dynamic performance. In addition, ramp response, such as ramp voltage disturbance response or ramp voltage reference response tests, could also be considered. Furthermore, dynamic performance assessment tailored for specific event-based scenarios, such as post-fault dynamic behavior, may also be relevant (See Section 7.3.5 on post-fault active power recovery)

The four test methods listed above are described in detail in the following sections. Although the dynamic performance studies will primarily focus on DC voltage droop control, the test methodology can be directly applied to other control modes as well. **TABLE 15** provides a summary of the applicability of the tests for each control mode, with the following notations: ✓ indicates straightforward applicability, N/A signifies unequivocal non-applicability, and (✓) indicates that while applicable, its relevance is questionable.

TABLE 15: Test applicability to each DC-side control mode.

	1.Step voltage reference response	2.Step power disturbance response	3.Step voltage disturbance response	(4.Step power reference response)
DC voltage droop mode	✓	✓	✓	(✓)
Fixed DC voltage mode	✓	✓	N/A	N/A
Fixed Active power mode	N/A	N/A	(✓)	✓

[23] Step power reference response test is not directly relevant to the specification and assessment of the primary DC voltage-related mode. Article 12 of the NC HVDC outlines the requirements for active power controllability, including the control range and ramping rate requirements at AC-PoC. However, in the context of a DC grid, it is crucial to evaluate the behavior of power at the DC-PoC. Therefore, this is included here for consideration.

6.6.4.2 Step voltage reference response test

Test objectives:

The objectives of the test involve the following:

- To ensure the capability of the AC/DC converter unit to adhere to the DC voltage set-point at its DC-PoC in a steady state.
- To assess the closed-loop dynamic behavior of the DUT under varying DC grid connection conditions

Test environment:

The test shall be carried out for each of the AC/DC converter units in the relevant AC/DC converter station.

The schematic illustration of the test environment for the step voltage reference test is shown in **FIGURE 38**.

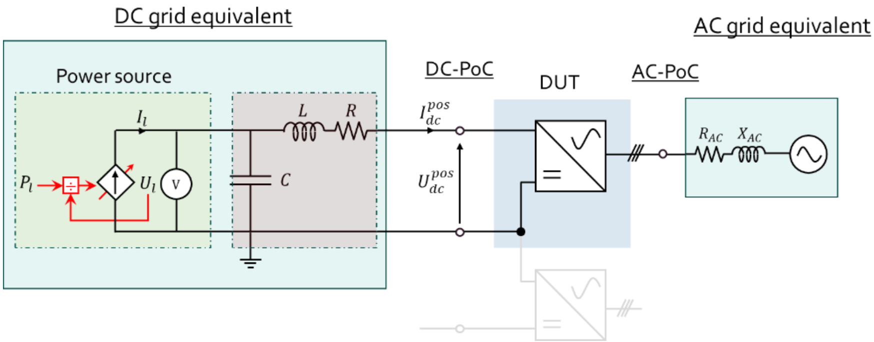


FIGURE 38 Schematic depiction of test environment for step voltage reference response test, where the DUT considered is the positive pole converter unit of an AC/DC converter station.

- AC grid equivalent:

The AC grid equivalent shall be specified by the system operator, in coordination with the relevant TSOs. A conventional approach is to represent it as a Thevenin equivalent, modelled by an ideal voltage source with appropriate SCR and X/R ratios. In that case, the specific values for SCR and X/R ratios should be determined by the relevant TSO, to accurately reflect the actual AC grid characteristics at the AC-PoC. When deemed necessary, the AC grid equivalent may also incorporate additional details, such as inertial dynamics and generic primary frequency response of the AC grid, which can be particularly pertinent for assessing the effect of GFM capabilities.

- DC grid equivalent:

The DC grid equivalent shall include a current or a flexible current source to inject/draw constant power, to replicate the initial power flow conditions for the study. Additionally, it must incorporate an impedance element to represent the adequate DC grid stiffness seen at the DC PoC. The impedance values should be selected to replicate both the highest and lowest DC grid stiffness at the DC-PoC. The system operator, in coordination with the relevant TSOs, is responsible for determining the appropriate impedance profiles for the test.

Test description:

1. Initial state:
    a. The initial power flow P_l should be set to one of the specified power flow conditions.
    b. The DC voltage at the DC-PoC of the DUT should be set to the normal DC voltage, i.e. $U_{dc}^{Set} = U_0 = 1\ \mathrm{p.u.}$
2. Without a ramp limiter on the DC voltage set point U_{dc}^{Set}, increase U_{dc}^{Set} of the DUT by ΔU_s. In the absence of data in the test sheets, the default value shall be $\Delta U_s = 0.02\ \mathrm{p.u.}$[24]
3. The test shall also be conducted with a step change in the DC voltage setpoint in the negative direction.
4. Repeat 1-3 with all the initial power conditions specified in 1.

TABLE 16 summarizes the relevant parameters to be specified by the system operator for the test scenario of the step voltage reference response test.

TABLE 16: Relevant parameters to be specified by the system operator for the scenario of the step voltage reference response test.

Symbol	Variable	Default value
P_l	Initial power flow condition	N/A[25]
U_{dc}^{Set}	DC voltage set point	N/A
ΔU_s	Magnitude of step change in DC voltage setpoint	$0.02\ \mathrm{p.u.}$

Signals to be reported

Time domain simulations must be carried out on an industry-standard EMT simulation platform. The HVDC system vendor is responsible for performing these simulations and provide the resulting time domain.

The HVDC system vendor shall provide the following signals obtained by the simulations:

- Measured signals at DC-PoC
    - Pole-to-neutral DC voltage
    - DC current
    - DC power
    - Pole-to-ground DC voltage
    - Neutral-to-ground DC voltage
- Measured signals at AC-PoC

[24] A 2% value is considered sufficient to capture the dominant DC voltage dynamics while staying within the continuous operating range. However, this value is provided as an example and is subject to agreement between the vendor and the relevant system operator.

[25] These initial power flow conditions should remain within the maximum power limits (in each direction) required of the converter station. The specific values should be determined through agreement between the vendor and the relevant TSO, based on the converter's intended purpose and desired operational capability.

- AC active power
- AC voltage

Evaluation Criteria

The evaluation criteria for the test can follow the definitions outlined IEV 351-46-12 "reference-variable response of the control system" [14].

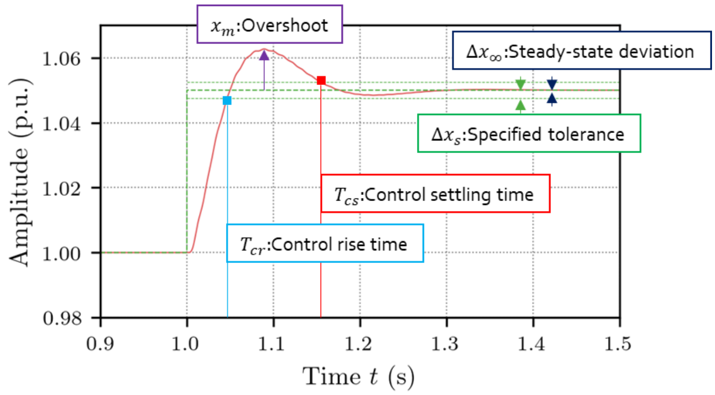


FIGURE 39 Parameter definition for the evaluation of the step voltage reference response test (The figure reproduced following the definition in IEV 351-46-12 "reference-variable response of the control system" [14].

TABLE 17 summarizes the evaluation criteria for the step voltage reference response test.

TABLE 17: Evaluation criteria for the step voltage reference response test.

symbol	variable	Corresponding variable	Default value
X_0, X_∞	Steady-state value of the controlled variable	$U_{dc}^{Set}, U_{dc,\infty}^{Set}$	$1, 1 + \Delta U_s$[26]
Δx_∞	Steady-state deviation		N/A
$2\ \Delta x_s$	Specified tolerance		$\pm 0.05\ \Delta U_s$
$\lvert x_m \rvert$	Overshoot		$\leq\ 0.2\ \Delta U_s$
T_{cr}	Control response time		$\leq\ 200$ ms
T_{cs}	Control settling time		$\leq\ 300$ ms

The DUT is considered compliant with the dynamic performance requirements if the reported signals meet the evaluation criteria specified by the system operator, in coordination with the relevant TSO.

Test demonstration:

For the demonstration purpose, **FIGURE 40** depicts the demonstration using an exemplary DUT solution, where a step change in the DC voltage set-point ($\Delta U_s = 0.02$ p. u) is applied. The initial power is set to 1000 MW in inverting mode. The impedance element in the DC grid equivalent is configured by the RLC

[26] Different voltage levels may also be considered accounting for the desired operational conditions of the DUT.

circuit with two combinations derived in the studies in Section 9.5, which represents the highest and lowest DC grid stiffness conditions. The grey area represents the forbidden regions in accordance with the default evaluation criteria metrics for the test. The **TABLE 18** summarizes the evaluation results of the test performed.

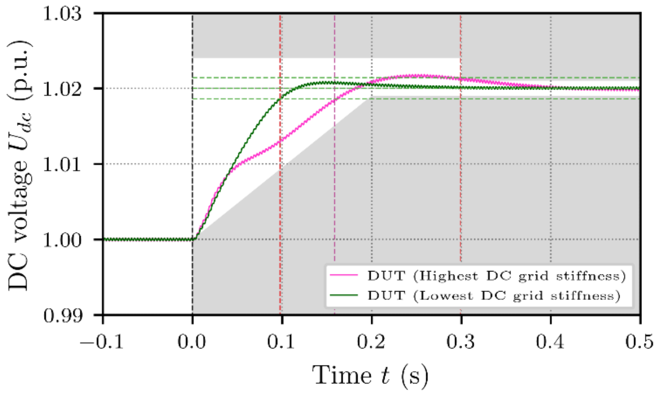


FIGURE 40 Demonstration of step voltage response test using an example DUT.

TABLE 18: Example evaluation results of the step voltage reference response test performed.

symbol	Default value	Highest stiffness	Lowest stiffness
X_∞	$1 + \Delta U_{dc}^{Step}$ p.u.	1.020	1.020
Δx_∞	N/A	0.000026	0.000047
$\lvert x_m \rvert$	$\leq\ 0.2\,\Delta U_{dc}^{Step}$	0.0018	0.0009
T_{cr}	$\leq$ 200 ms	159 ms	98 ms
T_{cs}	$\leq$ 300 ms	299 ms	98 ms

6.6.4.3 Step power disturbance response test

Test objectives:

The objectives of the test involve the following:

- To evaluate the closed-loop dynamics of the DUT under various possible operational conditions.
- To assess whether the DUT possesses sufficient disturbance rejection capability to handle worst-case disturbances.

Test environment:

The test environment remains the same as those for the step voltage reference response test. However, in this test, the power source is utilized not only to determine the initial power flow condition but also to generate the power disturbance.

Test description:

1. Initial state:
   a. The initial power flow should be set to one of the specified power flow conditions.
   b. The DC voltage at the DC-PoC of the DUT should be set to the specified value, e.g., $U_{dc}^{Set} = 1.0 \text{ p.u.}$
2. Generate a power disturbance by changing the value of P_l to $P_l + \Delta P_l$.
3. Repeat 2 with all the initial power conditions specified in 1.

TABLE 19: Relevant parameters to be specified by the system operator for the scenario of the step power disturbance response test.

symbol	variable	Default value
$\boldsymbol{P_l}$	Initial power flow condition	N/A[27]
$\boldsymbol{\Delta P_l}$	Change in power injection value	N/A[28]
$\boldsymbol{U_{dc}^{Set}}$	DC voltage set point	1.0 p.u.

Signals to be reported:

The signals to be reported remain the same as those for the step voltage reference response test.

Evaluation Criteria

The evaluation criteria for the test can follow the definitions outlined in IEV 351-46-13 (disturbance response of the control system) [15].

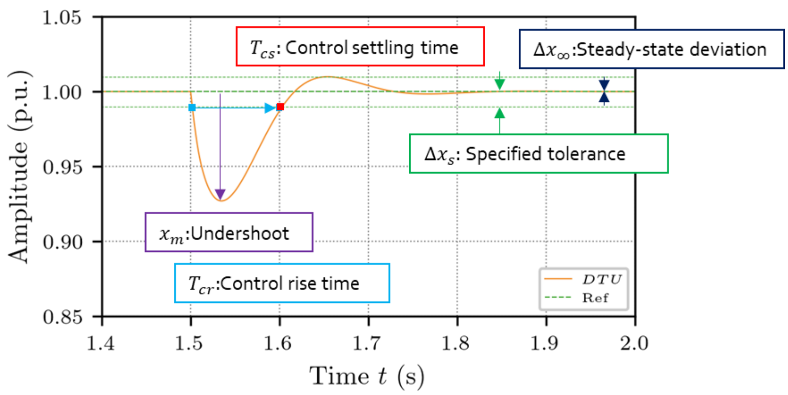


FIGURE 41 Parameter definition for the evaluation of the step power disturbance response test (The figure reproduced following the definition in IEV 351-46-13 (disturbance response of the control system) [15]"

[27] Similarly to the previous test, the specific values should be determined through agreement between the vendor and the TSO.
[28] The magnitude of the disturbance is defined by ΔP_l, with the default value left unspecified. The set of values of ΔP_l should be determined based on the agreed-upon initial power flow conditions and considering the maximum power capability of the DUT, ensuring that its operational limits are not to exceeded.

TABLE 20 summarizes the evaluation criteria for the step power disturbance response test.

TABLE 20: Evaluation criteria defining variables for the step power disturbance test.

symbol	variable	Corresponding variable	Default value
$\boldsymbol{x}$	Controlled variable	U_{dc}	N/A
$\boldsymbol{X_0, X_\infty}$	Steady-state values of the controlled variable	$U_{dc}^{Set}, U_{dc,\infty}$	N/A
$\boldsymbol{\Delta x_\infty}$	Steady-state deviation	ΔU_{dc}	N/A
$\boldsymbol{X_d}$	Desired value		N/A
$\boldsymbol{\lvert x_m \rvert}$	Over/Undershoot		$\leq 1.0\ (X_\infty - X_0)\ p.u.$
$\boldsymbol{2\ \Delta x_s}$	Specified tolerances		$\pm 0.1 * (X_\infty - X_0)$
$\boldsymbol{T_{cr}}$	Control rise time		$\leq 200\ ms$
$\boldsymbol{T_{cs}}$	Control settling time		$\leq 300\ ms$

The DUT is considered compliant if the reported signals meet the evaluation criteria specified by the system operator, in coordination with the relevant TSOs.

Test demonstration:

For demonstration purpose, **FIGURE 42** shows the step power disturbance test using the same exemplary DUT solution, where a step power disturbance of -1000 MW ($\Delta P_l = -1.0$ p.u) is applied. The initial power is set to 1000 MW in inverting mode. The impedance element in the DC grid equivalent is configured by the RLC circuit with two combinations derived in the studies in Section 9.5. **TABLE 21** summarizes the evaluation results of the test performed.

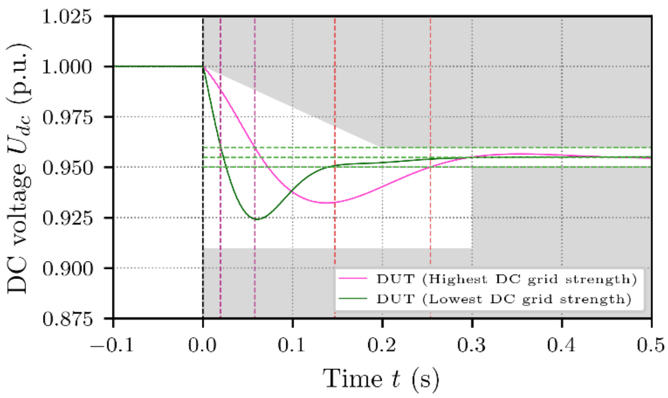


FIGURE 42 Demonstration of step power disturbance response test using an example DUT.

TABLE 21: Example evaluation results of the step power disturbance response test performed.

symbol	Default value	Highest stiffness	Lowest stiffness
$\boldsymbol{X_\infty}$	N/A	0.955	0.956
$\boldsymbol{x_m}$	$\leq 1.0\lvert X_\infty - X_0 \rvert$	0.023	0.031
$\boldsymbol{T_{cr}}$	≤ 200 ms	58 ms	20 ms
$\boldsymbol{T_{cs}}$	≤ 300 ms	254 ms	147 ms

6.6.4.4 Step voltage disturbance response test

In addition to the two previously presented test methods, which are grounded on well-established closed-loop control performance evaluation, an alternative testing approach may also be considered. As this alternative test method fundamentally differs from the prior approaches, it requires additional consideration that warrants careful attention.

Test objectives:

The objectives of the test involve the following:

- To assess the set-point tracking capability
- To assess the **open-loop** quasi-static behavior of active power response to changes in DC voltage

Test environment:

The test shall be carried out for each of the AC/DC converter units in the relevant AC/DC converter station. While the AC grid equivalent remains the same as in the two previous tests, the current or power source in the DC grid equivalent is replaced by a voltage source. The parallel capacitor connected to the voltage source should be removed, as the voltage is solely set by the connected voltage source. The voltage source is utilized to generate voltage disturbance.

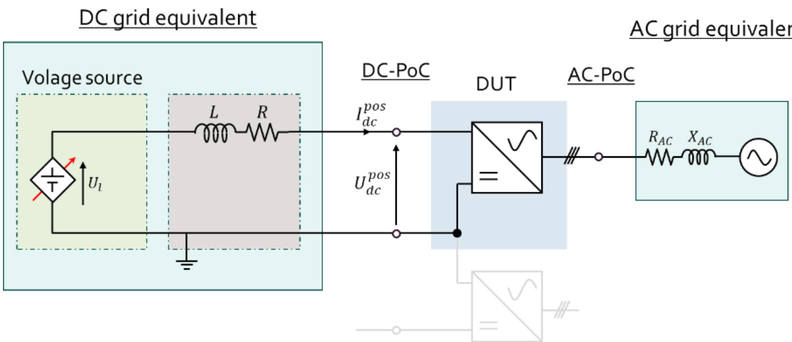


FIGURE 43 Schematic depiction of test environment for step voltage disturbance response test where the DUT considered is the positive pole converter unit of an AC/DC converter station.

Test description:

1. Initial state:
    a. The initial power flow injection P_l should be set to one of the specified power flow conditions.
    b. The DC voltage at the DC-PoC of the DUT should be set to the specified value, e.g., $U_{dc}^{Set} = U_0 = 1\ \mathrm{p.u.}$
2. Generate a voltage disturbance by changing the value of U_l to $U_l + \Delta U_l$. In the absence of a specific value, the default value shall be $\Delta U_l = 0.02\ \mathrm{p.u.}$
3. Repeat 2 with all the initial power conditions specified in 1.

TABLE 22: Relevant parameters to be specified by the system operator for the setup of the step voltage disturbance test.

symbol	variable	Default value
P_I	Initial power flow condition	N/A
ΔU_I	Change in voltage value	$[-0.02, 0.02]$ p. u.
U_{dc}^{Set}	DC voltage set point	1.0 p. u.

Signals to be reported:

The signals to be reported remain the same as those for the previous two tests.

Evaluation Criteria

The evaluation criteria for this test can be drawn on the practices in some AC-side functional specification. For instance, the specific dynamic performance requirements for FSM can be found in NC HVDC Annex II, A(1), as well as Article 71(6) [4]. The requirements for AC voltage control are outlined in article 22(3) and 71(3). For both, the requirements are predominantly characterized by activation times.

Adapting this to the DC counterpart, the evaluation criteria can be formulated as a set of activation times. The evaluation criteria defining parameters for the step voltage disturbance response test, along with its illustrative depiction, are provided in **FIGURE 44** and **TABLE 23**.

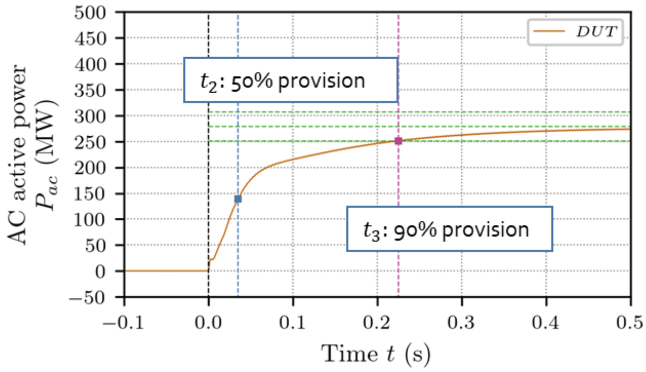


FIGURE 44 Parameter definition for the evaluation of the step voltage reference response (specifically illustrating the case where the initial power $P_I = 0$).

TABLE 23 summarizes the evaluation criteria for the step voltage disturbance response test.

TABLE 23: Evaluation criteria for the step voltage disturbance response test.

symbol	variable	Corresponding variable	Default value
t_1	Activation time		As fast as inherently technically feasible
t_2	50% provision		$\leq$ 50 ms
t_3	90% provision		$\leq$ 300 ms

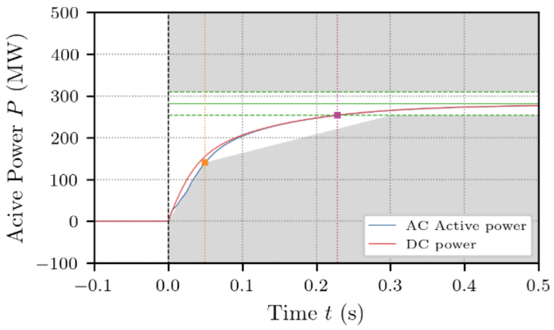
The DUT is considered compliant if the reported signals meet the evaluation criteria specified by the system operator, in coordination with the relevant TSOs.

Test demonstration

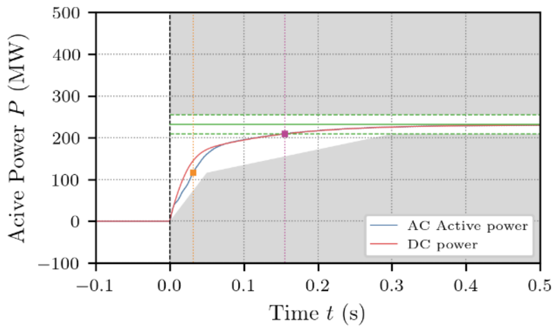
FIGURE 45 presents the step voltage disturbance response test results using the same exemplary DUT solution. In this test, a step DC voltage disturbance of 10 kV ($\Delta U_l = +0.02$ p. u.) is generated by the voltage source, with the initial power set to 0 MW. As previously noted, the impedance element in the DC grid equivalent is configured using the LR circuit, with values derived from the two combinations identified in the studies in Section 9.5.

A notable discrepancy in steady-state behavior is observed between the two cases, which is attributed to the resistance of the DC grid equivalent. This resistance influences the steady-state voltage at the DC-side connection point observed by the DUT. The dynamics immediately following the disturbance are strongly affected by the time constant of the LC circuit.

The relationship between observed dynamic behavior in this test and the actual behavior of grid remains an open question. Nevertheless, this test remains valuable for evaluating quasi-static behavior and assessing steady-state compliance for both DCVSM and LDCVSM modes.



a) The highest DC grid stiffness



b) The lowest DC grid stiffness

FIGURE 45 Demonstration of step voltage disturbance response test using an example DUT.

TABLE 24: Example of evaluation results of the step power disturbance response test.

symbol	Default value	Highest stiffness	Lowest stiffness
t_1	As fast as inherently technically feasible		
t_2	$\leq$ 50 ms	50 ms	31 ms
t_3	$\leq$ 300 ms	228 ms	155 ms

6.6.4.5 Step power reference response test

The functional specification and evaluation of active power control's dynamic performance at AC-PoC are well-established practices. The following provides a concise overview and a typical example, with the intention of extending the scope of the existing practice to incorporate quantities at the DC-PoC.

Test objectives:

The objectives of the test involve the following:

- To evaluate the ability to adjust the setpoint upon receiving an order
- To assess the set-point tracking capability
- To assess the capability of adjusting the power ramp rate

Test description:

1. Without ramp limiter
    a. increase P^{Set} of the DUT by ΔP_s.
    b. In the absence of data in the test sheets, the default value shall be $\Delta P_s = 0.1\ \mathrm{p.u.}$
2. With a ramp limiter
    a. increase P^{Set} of the DUT by ΔP_s with maximum ramp rate prescribed
    b. In the absence of data in the test sheets, the default value shall be $\Delta P_s = 0.1\ \mathrm{p.u.}$

TABLE 25: Relevant parameters to be specified by the system operator for the setup of the step power reference test.

symbol	variable	Default value
$\boldsymbol{\Delta P_s}$	Change in power set point	$+0.1\ \mathrm{p.u.}$
$\boldsymbol{\alpha}$	Maximum ramp rate	N/A[29]

Signals to be reported:

The HVDC system vendor shall provide the following signals obtained by the simulations:

- Measured signals at DC-PoC
    - Pole-to-neutral DC voltage
    - DC current
    - DC power
    - Pole-to-ground DC voltage
    - Neutral-to-ground DC voltage
- Measured signals at AC-PoC
    - AC active power
    - AC voltage
    - AC current

Evaluation Criteria

- The steady-state error of active power shall be less than 0.002 p.u.
- No disturbances shall be observed on the AC voltage
- In the test with ramp limiter, the prescribed ramp rate shall be adhered
- The DUT shall maintain stable operation without blocking or trip.

[29] The value shall be specified by the relevant operator.

6.6.5 Harmonic stability performance requirements

Small-disturbance stability, or small-signal stability of a system generally refers to how effectively each AC/DC converter contributes to the damping of small oscillations within the system. Since converters are coupled through the network, the way oscillations propagate across the system and how multiple converters interact with these oscillations significantly impact the small-disturbance stability of the system. Importantly, small-signal instability can occur at any frequency.

The dynamic performance requirements for DC voltage droop control mode or other operational modes are primarily dictated by the expected dynamic behavior of the system that they directly influence. In contrast, the stability performance requirements for an AC/DC converter should be viewed as a comprehensive evaluation of the converter's combined characteristics, including the converter's design parameters, the inner controller, and sensor delays, all of which play equally critical roles in determining its stability performance.

This section defines the harmonic stability performance requirements, along with the recommendations for the evaluation methodology and important considerations for its application.

6.6.5.1 Stability performance studies framework

This section outlines the framework for stability performance studies. Its fundamental concept aligns with traditional practices of harmonic stability studies in AC systems. The primary objectives of these studies are:

- To ensure the small-signal stability characteristic of the DUT at the DC-PoC under a range of operational conditions
- To ensure the readiness of the DUT's stability performance prior to system integration tests

Test environment for stability performance studies

The studies shall be conducted in frequency domain. For these studies, the system operator or system integrator, in coordination with the relevant TSOs, shall provide frequency-dependent impedance profiles that accurately represent the DC grid as seen from the DC-PoC in a range of possible operational conditions. The frequency range of the provided impedance shall sufficiently encompass the key dynamics where potential interactions may arise. Since the impedance of the grid is highly dependent on the grid configuration, power flow conditions, the other converter stations control modes, and other factors, the impedance profiles to be provided shall account for sufficient variations in those factors to capture a sufficient range of potential grid conditions.

Test methods for stability performance studies

The stability performance requirements of the DUT, under a range of possible operational conditions, shall be evaluated based on the Nyquist stability criterion and also validated in time domain simulations. To validate the frequency-domain stability results in the time domain, a representative DC grid equivalent is required.

The DUT will be deemed compliant if it meets the evaluation criteria specified by the system operator, in coordination with the relevant TSOs, across the range of operational conditions reflected in the grid impedance profiles.

Limitations and considerations in stability performance studies

The methodology presented includes several important considerations that require attention. One notable limitation arises when the grid is being constructed from scratch, as several subsystems may be designed in parallel during the design stage. This is in alignment with the InterOPERA context. In such cases, the grid impedance seen from a DC-PoC is dependent on the other subsystems that are still in the processes of design. In this scenario, it is a prerequisite that each vendor provides a preliminary impedance profile, as illustrated by the dashed arrow in **FIGURE 35**.

Additionally, the accuracy and applicability of the harmonic stability assessments rely on how well the obtained impedances represent various grid configurations and operational conditions observed at DC-PoC, as this variability could significantly affect the overall compliance results. Additional details can be found in Section 9.6.

While the proposed methodology focuses exclusively on behavior at DC-PoC, it is important to note that actual converters are multi-port systems. Therefore, the overall stability of the system cannot be guaranteed without considering the charcteristics of the AC grid to which each converter is going to be connected.

Given these points, it should be emphasized that the stability performance requirements and this assessment procedure for individual DUTs are primarily aimed at derisking and mitigation. Once the final C&P systems of all subsystems are provided by the respective vendors, incorporating all C&P into a detailed environment and thoroughly assessing all potential interactions based on full certainty on each subsystem, obtained by individual impedance scanning, remain crucial in ensuring the stability of the entire system.

6.7 Secondary DC Voltage Control

Like the primary AC frequency control, the primary DC voltage control is concerned with containment of DC voltage excursions and maintaining power balance in the DC grid using proportional control. Therefore, when a disturbance occurs in a DC grid, the primary DC voltage control will find a new equilibrium point, but it will be different from the pre-contingency DC voltage profile and power flow.

Similar to how secondary frequency control in AC systems corrects the area control error and restore the frequency to the nominal value after the primary frequency control action, the principal objectives of the secondary DC voltage control are [21]:

- To correct and maintain the active power interchange over the DC grid.
- To maintain or restore the power flow and DC node voltages within the specified limits.

It is imperative to acknowledge the fundamental difference between AC and DC systems. While the frequency serves as a global variable that reflects the generation and demand balance of the whole system, it is not the case in a DC grid as the DC voltage at each node varies due to the voltage drop across the cables and depends on the load flow conditions [22]. Consequently, unlike secondary AC frequency control, which dispatches power references to generators, secondary DC voltage control must transmit not only the appropriate power set-points but also the DC voltage set-points to the converter stations.

According to the optimal set-points calculated by the dedicated optimal DC power flow calculation algorithm, which takes into account the security constraints and objective function, the secondary DC voltage control ensures that the converter stations effectively track these set-points while respecting all the constraints [13].

6.8 Continuous Control Functional Requirements of Subsystems & Parameter Lists

TABLE 26 provides a comprehensive summary of the functional requirements and associated parameters related to the continuous control that subsystems must comply with, in addition to those stipulated in the NC HVDC [4]. This set of parameters and their range are preliminary proposal based on initial investigations. During Phase II of the InterOPERA project, these recommendations will undergo a thorough validation process.

TABLE 26 Continuous Control Functional Requirements of Subsystems & Parameter Lists

FR	Short description	Associated parameters, if any	Subsystem
Element status analysis	The DC grid controller shall be capable to ascertain the real-time status of every element within the HVDC system.		DC grid controller
System topology analysis	The DC grid controller shall be capable of accurately determining the actual configuration of the grid topology		DC grid controller
Element limitation analysis	The DC grid controller shall be able to comprehend the actual capabilities of each converter station within the system.		DC grid controller
DC power flow optimization	The DC gird controller shall be able to calculate the optimal DC power flow, adhering to the objective function specified by the relevant TSO.		DC grid controller
Secondary DC voltage control	See Section 6.7		DC grid controller
Ramp rate coordination	The DC grid controller shall be capable of adequately coordinating the ramp rate of individual converter stations or unit to ensure the power balance during the ramping process.		DC grid controller
Offshore power curtailment	See Section 6.4.3.5		DC grid controller

Control mode management	The DC grid controller shall oversee the coordination of the control modes and their associated parameter when there is a need, such as a change of topology, according to predefined criteria.		DC grid controller
Fixed DC voltage control mode	See Section 6.5.1.1		AC/DC converter station or unit
Fixed active power control mode	See Section 6.5.1.2		AC/DC converter station or unit
DCVSM	See Section 6.5.3.1	Static requirements: **TABLE 10**, **TABLE 11** Dynamic requirements: **TABLE 17**, **TABLE 20**, **TABLE 23**	AC/DC converter station or unit
LDCVSM-O	See Section 6.5.3.2	Static requirements: **TABLE 10**, **TABLE 12** Dynamic requirements: **TABLE 17**, **TABLE 20**, **TABLE 23**	AC/DC converter station or unit
LDCVSM-U	See Section 6.5.3.3	Static requirements: **TABLE 10**, **TABLE 13** Dynamic requirements: **TABLE 17**, **TABLE 20**, **TABLE 23**	AC/DC converter station or unit
DCVLM	See Section 6.5.3.4	Static requirements: **TABLE 10**, **TABLE 14**	AC/DC converter station or unit
PLM	See Section 6.5.3.5	P_{Max} & P_{Min}	AC/DC converter station or unit

7. DC grid protection

The protection of DC systems should follow the same objectives as in AC systems: Ensuring a reliable and secure HVDC system operation during contingencies and component failures. The deployment of a multi-terminal multi-vendor HVDC system protection presents new challenges compared to Point-to-Point HVDC systems where protection measures are turnkey solutions at the boundary of the HVDC system.

In a large scale HVDC system the shutdown of the entire system is not compliant with power system criteria which imposes the use of DC-FSDs in order to limit the impact for a single contingency event. In a multi-vendor context different subsystems need to work seamlessly together. For instance, different fault separation concepts and devices at DCSS level need to be compliant with FRT concepts of AC/DC converter stations in order to avoid unexpected loss of power. The functional framework should provide a guideline that allows different technical solutions to connect to an evolving HVDC system while ensuring a reliable and secure DC grid protection with respect to constraints at both AC and DC points of connection.

The outline of this section is as follows. The first sub-section 7.1 defines relevant terms in the context of DC grid protection. Sub-section 7.2 defines overarching protection system level requirements and system states ensuring a coordinated DC grid protection design while respecting AC and DC system boundary conditions. Sub-section 7.3 defines converter station DC-FRT requirements. DCSS fault separation requirements are defined in sub-section 7.4. Preliminary standalone compliance tests are described for converters with regards to the DC-FRT requirement and for DCSS with regards to the fault separation requirement. Section 7.6 and 7.7 discuss insulation coordination and DC system grounding in a multi-terminal multi-vendor context. Finally, sub-section 7.8 provides an overview on functional requirements related to DC grid protection with assignment to the subsystems as defined chapter 4.

A guideline on how to apply protection requirements is provided in appendix section 9.8. This includes an assessment of applicability and verifiability at the DC-PoC as well as a verification of satisfying system level behaviour with regards to pre-defined key performance indicators. A second key investigation in appendix section 9.9 assesses the compliance of temporary blocking as part of the DC-FRT specifications with regards to islanded operation of DC connected PPMs offshore.

7.1 Terminology

7.1.1 DC grid protection function definition

- **Protection :** The provisions for detecting faults or other ordinary contingencies in a power system for enabling fault clearance, for terminating ordinary contingencies and for initializing signals or indications.
- **DC grid protection scheme :** The objective of a DC protection scheme is to prevent damage to system equipment, guaranteeing human safety and to keep the power system stable by isolating only the components under fault, whilst leaving remaining part as possible in operation and preventing the system from blackout, it includes the DC grid main protection and the backup protection to ensure a safe and reliable operation of the DC grid.

- **DC grid main protection (addressing the functions of several subsystems):** The primary or main protection is designed to immediately sense and respond to faults in order to isolate the faulty part of the system from the healthy part. The DC grid is divided into fault separation zones (see FSZ below). For each zone there is a specific protective scheme. When a fault occurs in an FSZ, it is the duty of the primary or main relays and protection components to detect the fault and take inherent action to isolate the faulty element.
- **DC grid backup protection (addressing the functions of several subsystems):** The backup protection provides the backup to the DC main protection whenever it fails to operate, or it is out of service for maintenance. Different types of backup protections exist:

1. Remote backup protection: Primary and backup protection are executed at different locations.
2. Local backup protection: The backup protection is performed locally by triggering adjacent switching units located at the same DC switching station.
3. Relay backup protection: Primary and backup protection relays are connected to the same switching unit. Backup protection is activated when primary protection fails to detect the fault.

- **Fault separation zone (FSZ):** A FSZ defines a zone in which a fault current can be suppressed by operation of FSD at the borders of the FSZ. Two different types of FSZ exist (for illustration, see single-line diagram in **FIGURE 46**:
- **Selective FSZ**: Comprises a single fault isolation zone which is equal to the FSZ (see **FIGURE 46**, FSZ2 and FSZ3). Fault separation function and fault isolation function are within the same switching unit. The fault discrimination functions are redundant as they cover the same zone. After fault isolation, no reconfiguration is possible.
- **Partially selective FSZ**: Comprises several fault isolation zones which are unequal to the FSZ but included within (see **FIGURE 46**, FSZ1 including FIZ1.1 and 1.2). Fault separation function and fault isolation function may or may not be in the same switching unit. The fault discrimination functions are not redundant as they do not cover the same zone. After fault isolation, a reconfiguration is possible and reclosing of the healthy part can be considered.
- **Fault isolation zone (FIZ):** A fault isolation zone defines a zone in which a fault can be isolated by operation of an RCS at the border of the FIZ.
-

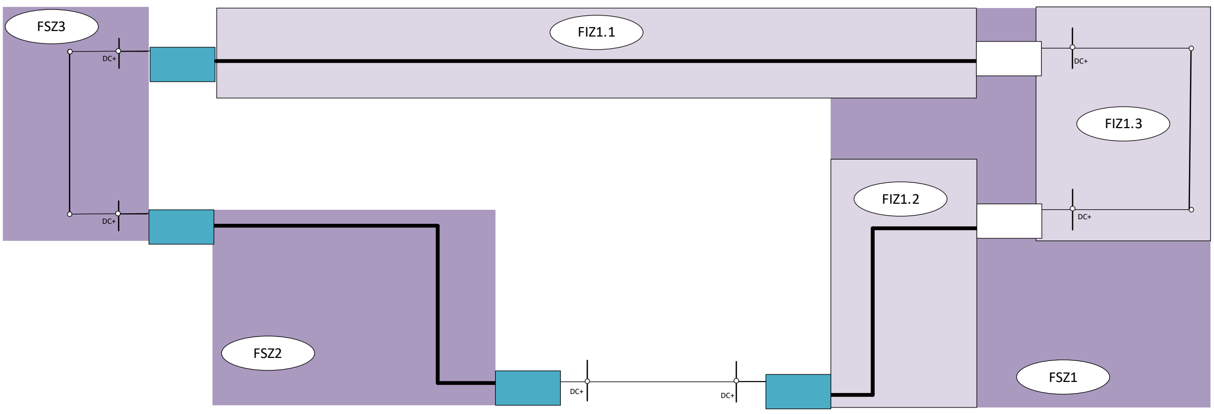


FIGURE 46 Illustration of selective FSZ (FSZ2, FSZ3), partially-selective FSZ1 including three FIZ 1.1, 1.2 and 1.3 (single pole representation)

- **DC Fault-ride-through (DC-FRT) :** Defining the required withstand capability of a converter station to remain connected during protection actions related to DC contingencies including faults, disturbances and dynamic responses.

7.1.2 Protection component definition

The following devices are of relevance for protection function executions and are part of the switching unit as defined in section 5.3.

- **Fault separation device (FSD)[30]:** Subsystem component with fault neutralization and fault current suppression capability
- **Passive fault current limiting:** Fault current limiting by passive devices, e.g. DC reactors or Superconducting Fault Current Limiters (SFCL).
- **Zone distinction device (ZDD)** [1]**:** Physical device that enables non-unit fault discrimination within a protection zone, e.g. DC reactor.
- **Residual Current Switch (RCS):** Switch with ability to break small amount of current (typically residual current) and with making current capability.

7.1.3 Switching unit protection function definition

The following protection function definitions consider a simplified FSD system level representation with ideal ON/OFF operation as shown in **FIGURE 47**. Note that the FSD is part of the switching unit. The terminology and associated times are illustrated in **FIGURE 48**.

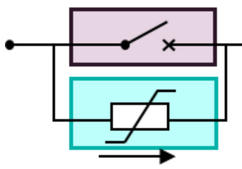


FIGURE 47 FSD system level representation consisting of main branch and energy absorption branch [23]

- **Fault detection:** Functionality to detect a fault based on local measurements of the protection relay located at unit level.
- **Fault discrimination:** Functionality to distinguish between faults inside and outside of the protection zone (located at unit level) based on local measurements only (non-unit based) or with remote end telecommunication (unit based).
- **Fault neutralization:** Fault neutralization describes the moment when the peak fault current is reached. In case of a FSD this implies that the transient interruption voltage (TIV) is sufficiently established.
- **Fault neutralization time:** The time interval between fault arrival and the instant when the fault current starts to decrease (peak fault current). Due to the TIV created by the FSD the fault is effectively neutralized and the system voltage for the healthy part of the system can start to recover [24]. The fault neutralization time includes the relay time for fault discrimination and internal current commutation time.

[30] For the first set of definitions a simple framework with focus on the main system-level functionality of the FSD is assumed (operating in ON/OFF mode)

- **Relay time:** Time interval comprising fault detection and fault discrimination time. The relay time starts with the fault arrival and ends with the reception of the trip order at the FSD [24].
- **Internal current commutation time:** Time interval between the reception of the trip order and the reach of peak TIV.
- **Fault current suppression:** Fault current suppression describes the moment when a residual current is reached.
- **Fault current suppression time:** This is the time interval between fault neutralization and the instant when the current has been lowered to residual current level (or below) [24]
- **Fault current interruption time :** Time from fault arrival until reaching residual current level.
- **Fault isolation:** Physical disconnection leading to a current zero (suppression of residual current). It should be noted that galvanic disconnection is achieved by a RCS, additional opening of disconnector switch is optional.

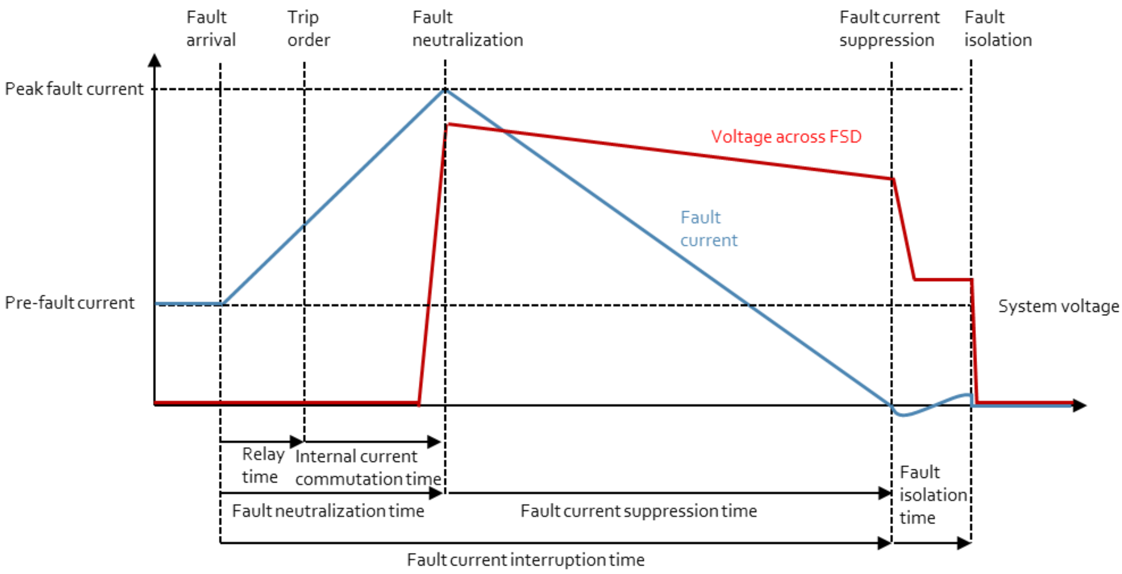


FIGURE 48 Fault current interruption process; main system functionalities of an FSD

7.2 DC system level requirements

7.2.1 Grid operating states during contingencies

Both the IEC TS 63291 and the SOGL distinguishes between normal operation, alert state, emergency state and blackout state [3] [6]. The main difference between IEC and SOGL is the time perspective. The IEC TS 63291 state definition is looking at the currently measured state of the system and whether something unplanned has happened in the past. Whereas SOGL is meant to be looking at the currently measured state of the system and making an analysis of unplanned events threatening the system stability in the future. As states are implying needs for operator actions, this makes quite a difference in the operating philosophy. **TABLE 27** provides a grid operating state description and provides high level examples of DC grid contingency scenarios and dedicated countermeasures and remediation actions without considering a particular notion of time which may be subject to further discussions.

- **Countermeasures** are all planned actions which react on all contingencies with the primary objective to keep the system within operational limits: Two baselines can be distinguished:

- Planned local protection actions when encountering ordinary contingency from the list of ordinary contingencies
- Local primary control actions releasing available reserves

- **Remediation actions** are additional actions which are activated when countermeasures have not prevented the system to enter emergency or blackout state. If in emergency state, remediation actions shall bring the system back to normal state before it enters black-out state. Examples are activation of energy absorber units and curtailment of PPMs.

TABLE 27 Grid operating states during DC contingencies, countermeasures and remediation actions

	Grid operating state description	DC grid contingency scenarios	Counter measures / Remediation actions
Normal state	Normal state means a situation in which the system is within operational security limits (no voltages or currents exceed operational limits).	Small deviations from scheduled load flow due to mismatch between scheduled and actual wind power production or ordinary contingencies without violation of operational limits.	Primary control provides local actions to avoid any violation of operational limits.
Alert state	Alert state means a situation in which the system is within operational security limits, but an ordinary contingency has been detected leading to major deviations compared to the initial power flow schedule. In alert state the system may not have sufficient primary reserves to encounter a second contingency. Remediation actions are foreseen to bring the system back to a normal operating state	All DC grid ordinary contingency scenarios (faults, unavailability of devices) including dedicated primary and backup protection sequences considering sufficient primary reserve.	Counter measures are foreseen to keep the system within operational limits (e.g. primary control ensures within the available reserves that operational voltage limits are not exceeded. Remediation actions are necessary to bring the system back to normal state (e.g. send out a new optimal operating point for the degraded system (see section 6.7, Secondary control).
Emergency state	Emergency state means a state in which one or more operational security limits are violated.	All extraordinary contingencies or ordinary contingencies if available reserves are depleted.	In emergency state, countermeasures are depleted. Immediate remediation actions may be required to avoid blackout state and to bring all system components back into operational limits. Coordinated protection actions may be necessary to avoid blackout state. Coordinated reconfiguration/ restoration towards a safe operating state may be necessary.
Blackout state	Blackout state means the state where the operation of part or all the transmission system has stopped.		Start-up of remaining DC grid

The classification of DC faults as ordinary contingencies is subject to TSO investigation of likelihood and risk assessment. The DC grid protection and other counter measures and remediation actions shall be designed such that for all ordinary contingencies both AC and DC systems do not run into emergency or blackout state. Note that the association of DC contingencies to either ordinary or extraordinary is not in the scope of this report as this is a question of power reliability impact, acceptable maximum loss of infeed and desired availability which needs to be carefully coordinated by system operators. A classification into ordinary and extraordinary contingencies for the InterOPERA demonstrator topology has been provided in [17].

Disturbances classified as extraordinary contingencies can cause the system to enter emergency or blackout state (see **TABLE 28**). In small DC grids with limited primary reserves intermediate remediation actions may be necessary if primary reserves are depleted (e.g. Energy absorber unit activation and PPM curtailment). As blackout state should be avoided, coordinated remediation actions may be necessary[31]. The protection design shall be coordinated in a way that it responds to the boundary conditions imposed by the system operators by eliminating unsafe conditions and prevent collateral damage in a safe and selective way. For this purpose, individual protection requirements need to be coordinated with each other. This concerns in particular the DC-FRT requirements of converters and the fault separation requirements of the DC switching station.

TABLE 28 System state after ordinary and extraordinary contingency and counter measures

	Ordinary contingencies	Extraordinary contingencies
System state	May result system in a system alert state (No violation of operational limits in post-fault operation) or in emergency state if countermeasures are depleted.	May result in a system emergency or blackout state (Violation of operational limits in post-fault operation)
Counter measures/	Protection sequence is foreseen, protection equipment is rated for fault separation. Primary control actions are activated (see section 6.5).	No dedicated protection sequence foreseen. Primary control actions are activated (see section 6.5).
Remediation action	If primary reserves are depleted, remediation actions such as energy absorber unit activation and PPM curtailment may be activated.	Remediation actions may be required, some active network elements may enter into limited mode (primary reserves exhausted) or disconnection (individual converters may disconnect due to DC-FRT violation).

7.2.2 Boundary conditions at AC side offshore

The state of the art for AC offshore grids is, that the offshore converter is operated in V/f control mode while PPMs operate in grid following mode. In case of offshore converter disconnection or blocking, both frequency and voltage are uncontrolled and may exceed operational limits as specified in [4]. In case of an overvoltage event, PPMs may disconnect according to AC OVRT specifications [4]. A disconnection of PPMs requires a time-consuming manual restoration sequence. Therefore, disconnection of PPMs must be considered as a permanent loss of active power. For this reason, the DC-FRT behaviour of the offshore

[31] The definition and classification of extraordinary contingencies is not in the scope of this report.

converter shall not provoke a disconnection of the PPMs by exceeding the specified OVRT limits during DC faults. Two cases must be distinguished for DC-FRT considerations:

- The converter remains in continuous operation and provides continuously a V/f-reference to the PPMs.
- The converter temporarily blocks during DC fault transients and deblocks after DC voltage recovery. When temporarily blocked, the offshore converter behaves as an uncontrolled diode rectifier and does not provide a V/f reference to the PPMs[32]. An overview of the macro-sequence is provided by **FIGURE 49**. From converter blocking to DC fault neutralization the DC voltage drop leads to a voltage drop on the AC side. After fault neutralization, DC voltage recovers leading to an overvoltage ride-through event on the AC side which persists until deblocking of converter.

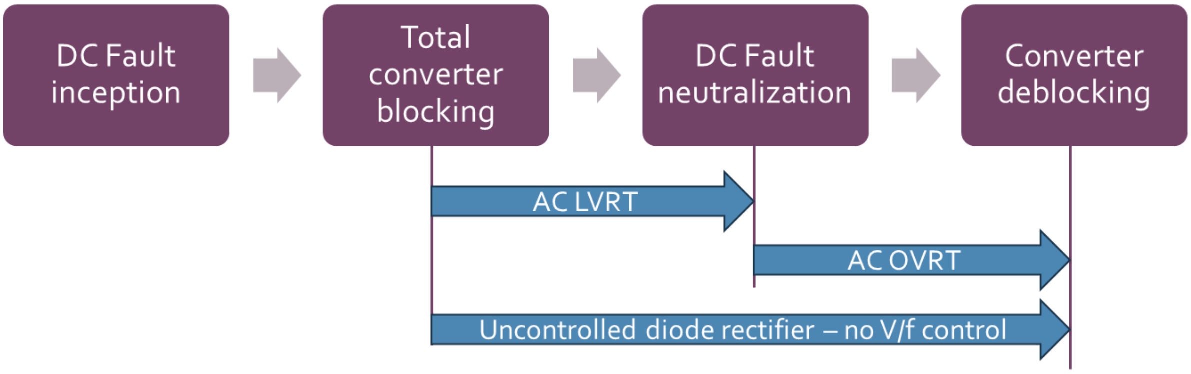


FIGURE 49 Perception of DC-FRT by PPMs in case of temporary blocking of offshore converter in V/f control

Note that in D2.2 the term "temporary islanding" is used to address DC-FRT requirements during temporary blocking of the offshore converter. In addition, alternative grid forming control concepts for PPMs have been proposed to facilitate a DC-FRT with temporary offshore converter blocking [2].

The temporary blocking of the offshore converter during DC fault transients is compliant as long as voltage and frequency ranges at the AC side do not lead to a disconnection of PPMs. To ensure this, an alignment between OVRT requirements of PPMs and DC-FRT requirements of the converter station is needed. Applicable AC requirements for offshore PPMs such as OVRT profiles and frequency deviation limits as well as other limits (e.g. loss of synchronization due to phase jumps) shall be considered and carefully assessed.

In section 9.9 an extensive investigation is carried out with focus on the compliance between the DC-FRT requirements including temporary blocking and existing AC requirements for PPMs. The overall sequence from DC fault inception to full restoration of PPMs is investigated in a step-by-step approach highlighting challenges and solutions for islanded mode operation and resynchronization. The performance of each of the proposed solutions is evaluated based on EMT simulations followed by key conclusions and recommendations.

7.2.3 Boundary conditions at AC side onshore

[32] Considering decoupled operation of positive and negative pole at the offshore side. Note that in case of coupled operation during a PtG fault, the V/f control would be ensured by the healthy pole converter.

HVDC power loss characteristics should at least comply with existing AC requirements. Any power loss in the DC grid should be less than the maximum loss of infeed for the considered AC zone. The permanent loss of active power shall comply with the Frequency Restoration Reserve (FRR) of the corresponding bidding zone (see exemplary values in **TABLE 29**). It should be noted that respecting those limits is a planning issue which depends on boundary conditions and reliabilities assumed on AC and DC side (e.g. classification of ordinary and extraordinary contingencies according to availability data and risk assessment of the relevant TSO). More explicitly, ordinary contingencies on the DC side shall respect the maximum loss of active power of surrounding AC grids and existing requirements at the AC-PoC as stipulated in [4].

TABLE 29 Boundary conditions in surrounding AC grids

Related AC parameter	Value
Maximum loss of infeed	UCTE: 3 GW Nordic grid: 1,4 GW
FRR per bidding zone	Dependent on country

7.2.4 DC grid protection coordination

As part of DC grid protection coordination, fault separation zones (FSZ) shall be defined such that all ordinary contingencies are isolated while respecting AC boundaries as defined above. The FSZ shall in particular respect the maximum loss of infeed constraints from surrounding AC grids and ensure stable DC grid operation after fault separation.

The switching units at the boundaries of FSZs shall be equipped with FSDs which are capable of separating all ordinary contingencies within a maximum fault neutralization time $T_{N,max}$.

Converters outside a fault separation zone will remain connected to the DC grid and are expected to recover and operate after fault separation[33]. The main purpose of the DC-FRT profile at the PoC of the converter is to ensure:

- Converter connection during fault separation
- Converter operation after fault recovery
- Safe disconnection of the converter in case of protection failure

FIGURE 50 provides an illustrative example on FSZ definition and operational expectations after fault separation. Faults in FSZ1 and FSZ2 are expected to be separated by associated switching units with DC current breaking capability (blue color). The converter station is outside FSZ1 and FSZ2 and is therefore expected to be operational after fault separation which is ensured by a DC-FRT profile as introduced in section 7.3. For faults in a FSZ3 the fault separation sequence involves the activation of both FSD on the DC side and the ACCB on the AC side of the converter. The activation of the ACCB is ensured by a dedicated fault detection and discrimination function for FSZ3. The example underlines the following points:

[33] Note that all elements inside a FSZ including converters are separated from the DC grid and out of operation after fault separation. In this case, the triggering of the ACCB is part of the protection sequence and shall not be confused with triggering when exceeding the DC-FRT profile which is due to protection failure

- **Converter station inside FSZ:** The DC-FRT profile does not apply for ordinary contingencies in protection zones which involve AC Circuit Breaker (ACCB) operation.
- **Converter station outside FSZ:** The converter station is expected to operate after fault separation. This involves to respect on the one hand the DC-FRT requirements and on the other hand relevant AC side requirements[34]

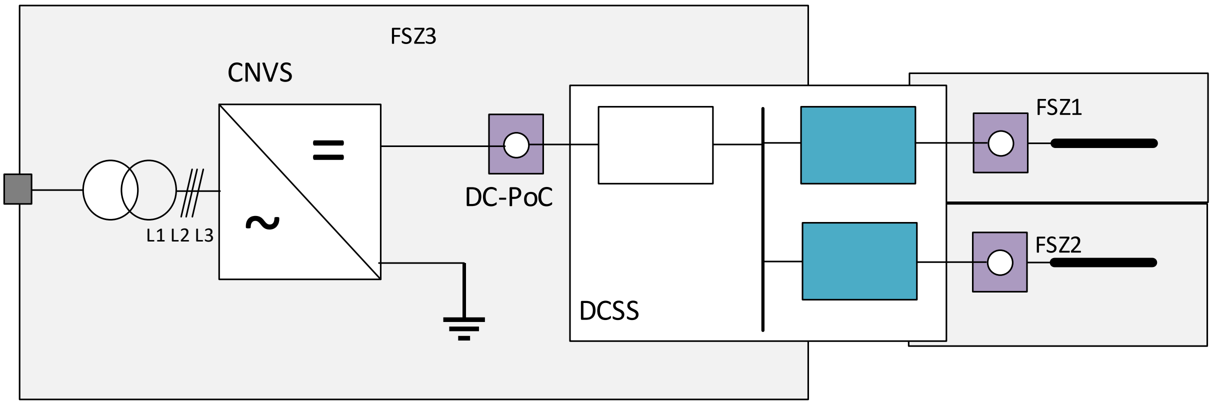


FIGURE 50 Illustrative example on fault separation zone definition and DC-FRT profile application at DC-PoC; blue and white boxes inside a DCSS indicate respectively switching units with and without FSD

The following sections 7.3 and 7.4 define respectively DC-FRT requirements for AC/DC converter station and fault separation requirements for DCSS. From the example given above, it is clear that the maximum DC system recovery time for the converter DC-FRT requirement must be at least as long as the maximum fault neutralization time $T_{N,max}$ of any FSD in the system. In other words, the converter shall not trip before expected fault neutralization time. **FIGURE 51** shows this interdependence between fault neutralization time, converter overcurrent capabilities and DC reactor size considering half-bridge converters with very limited fault current control capabilities during DC faults. Supposing a limited overcurrent capability of converters, the fault either needs to be eliminated very fast or a significant DC reactor size need to be considered to limit the increase of fault current sufficiently. To ensure a technological agnostic definition of functional requirements, the following points shall be considered:

- Fault neutralization time shall be chosen such that FSD technologies can be considered
- Overcurrent capabilities shall not be pre-set to avoid excluding some converter solutions
- DC reactor sizes shall be chosen such that dynamic control objectives are satisfied

In order to ensure an inclusive specification and design of both converter and FSDs while limiting the need for large DC inductors alternative means to ride through DC faults including temporary blocking will be considered in the DC-FRT description. Such alternatives may reduce the need of DC reactors significantly.

[34] Requirements may be different depending on onshore or offshore grid connection

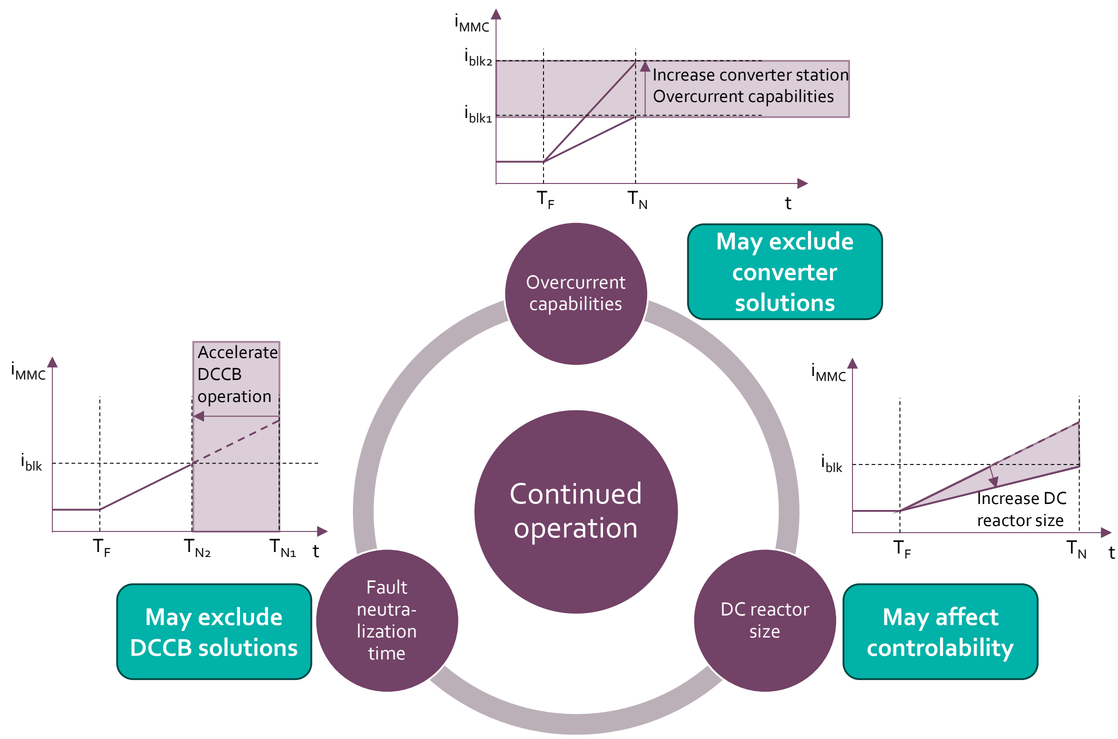


FIGURE 51 Interest of temporary blocking during DC-FRT: Interdependence between system level protection parameters considering continued operation

7.3 DC-FRT requirements of converters

Disclaimer: To ensure a certain degree of technological openness, this deliverable describes all possible ways of riding through DC faults. The relevant TSO decides whether functions such as "temporary blocking" can be used as a protective function in the event of DC faults. Especially as continuous operation in the healthy protection zones has a high priority for the TSOs and the impact on the AC grids (offshore and onshore) shall be as small as possible in order to guarantee the overall system stability. To provide a sufficient basis for such decisions, detailed information on the behavior of the converters and the resulting effects are provided in section 9.8 for the DC side and in section 9.9 for the AC offshore grid. The technical investigations provide insights on the applicability and MTDC system behaviour of the DC-FRT requirement including temporary bocking. Further investigations shall be focused for example on whether all phases are or only individual phases are blocked, how long the blocking process takes, how long it take to reach the pre-fault operating point (or the new operating point as adjusted by the grid controller) and in particular, how many converters could be affected and what is the impact for the AC on- and offshore grids. It shall be noted that temporary blocking might not be readily available in all current market solutions for AC/DC converter stations. Beyond the simulation assumptions made in the key investigations, detailed investigations might be required for some vendors before such a functionality can be offered commercially.

In the AC grid code, the FRT requirement serves to define the capability of the converter to stay connected during low voltage conditions. Based on this, a disconnection of generating or power exchanging units during protection action is avoided when outside the protection zone. The AC-FRT description is generic in the sense that it is not topology dependent and does not consider the specific performance of the AC switchgear. It neither distinguishes between a FRT curve for primary or backup protection nor between individual FRT curves for each protection zone in the AC grid. There is one single FRT curve ensuring a clear functional split between withstand capability of the generating / power exchanging unit and fault clearing of AC switchgear [4].

In the IEC TS 63291, a design / topology dependent approach for the converter DC-FRT definition has been chosen following a protection zone matrix approach. Different operational concepts for each PoC-AC and each PoC DC are defined: Continued operation (CO), Temporary stop (TS) and permanent stop (PS). For each converter in the HVDC system a protection coordination matrix is established which defines the operational behaviour requirement for each fault separation zone and each protection sequence (primary/backup) individually. Hence, the converter FRT requirement changes depending on the location of the fault and the associated protection sequence. With such a design / topology dependent approach, a DC-FRT curve would need to be defined for each operational concept and each protection sequence with a dependability between converter FRT and fault clearing. In addition, the temporary stop in the same DC grid may lead to a different state of the AC grid depending on AC system characteristics (e.g. network strength, clearing times, onshore or offshore connection).

FIGURE 52 shows an example following the design / topology dependent approach proposed by the IEC TS 63291. A converter unit is inside FSZ3 and connected to FSZ1 and FSZ2 via a DC switching station. The converter has an individual FRT requirement for each FSZ. It should remain in continued operation (CO) for FSZ1, temporary blocking (TB) is allowed for FSZ2 and a permanent stop (PS) is foreseen for FSZ3. Focusing first on FSZ1 and FSZ2, the converter FRT compliance cannot be ensured by the converter unit itself. It rather depends on the design of the individual switching unit connection FSZ1 and FSZ2. In fact, with this approach a strong coordination between the converter design constraints (e.g. overcurrent capabilities) and the switching unit design constraints (FSD operating time, fault current limiting device) is unavoidable. For a busbar fault (inside FSZ3), the converter unit is in permanent stop, meaning permanent disconnection on both AC and DC side. The definition of FSZ3 and the assignment of a converter behaviour is an example of how in a topology / design dependent approach fault separation and converter FRT definition are interdependent. A converter FRT definition for a FSZ covering the converter itself is obsolete since fault separation is handled by converter protection actions.

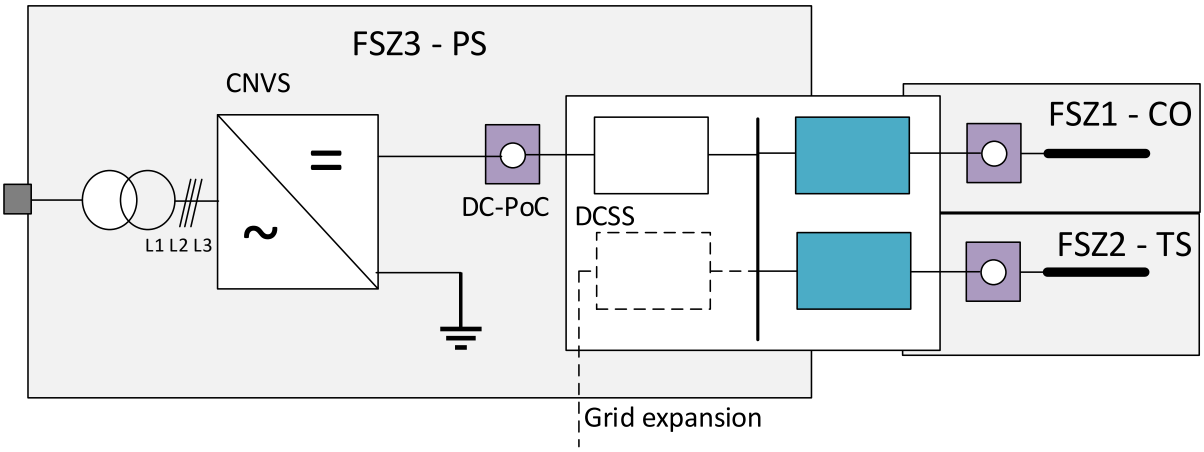


FIGURE 52 Example of design / topology dependent DC-FRT description (based on [3])

Extending this example further, a future grid expansion consisting of an additional converter connection to the same busbar as indicated by the dashed line in a design dependent approach reveals the question of inclusive grid design. To which extent does the initial design of the first converter unit (e.g. overcurrent capabilities) and the switching units (e.g. fault neutralization time, fault current limiting device and current breaking capability) restrict other subsystems with lower performance to connect at a later stage?

A design-based approach is tentative for small MTDC grid configurations as it potentially leads to an optimized design for a given sub-grid or node and connected converter stations and DC switching stations. However, a design-based approach implies a strong coordination of key design parameters between subsystem vendors. For instance, the fault current limiting devices (e.g. DC reactors, SFCL, ...) need to be coordinated between DCSS and converter station such that it corresponds to the transient withstand capabilities of the converter (e.g. overcurrent limit, energy limit, ...) with respect to the fault neutralization time of the FSD and the respective current breaking capability. Any advanced FRT functionality such as temporary blocking or energy-based control would need to be assessed individually.

Different approaches of defining DC-FRT capabilities have been discussed within the DC grid protection workstream. They differ mainly in terms of genericity (generic or design / topology dependent) and the quantity they are expressed in (DC voltage or DC current). An evaluation of different DC-FRT profiles based on the following criteria is provided in appendix 9.7. The following sub-sections describe the resulting DC-FRT profile and relevant parameters.

- **Technological agnostic:** Are the functional requirements permitting different technological solutions or are they restricting, excluding certain technologies?
- **Functional split:** Are functional description and design of subsystems independent? How to split functional responsibilities?
- **Oversizing :** Does the decoupling of subsystem requirements and the genericity / system independence generate an oversizing?
- **Standardization:** Is the DC-FRT description subsystem-dependent or generic? Do several DC-FRT profiles co-exist?
- **Verifiability :** Can the DC-FRT profile be specified at the DC-PoC based on local measurements?

The functional requirements apply at the DC-PoC of the converter station. All parameters that are defined in the following refer to verifications at the DC-PoC, DC voltage specifications are pole-to-ground voltages (see $U_{DC\text{-}FRT}$, **FIGURE 53**). It should be noted that there might be current limiting devices such as DC reactors installed as part of the converter station in order to comply with the DC-FRT profile at the DC-PoC.

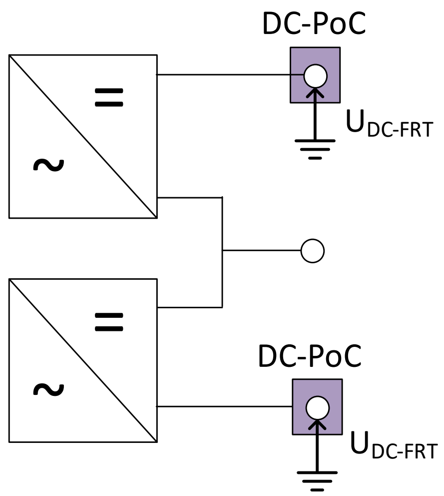


FIGURE 53 AC/DC converter station - illustration of reference point for DC-FRT definition

7.3.1 Low voltage ride-through (LVRT) requirements

Disclaimer: Different approaches of defining DC-FRT profiles have been discussed within the DC grid protection workstream. Appendix 9.7 shall be seen as a complementary section providing background information on alternative descriptions highlighting the main differences and outlining advantages and drawbacks of each DC-FRT profile. This annex documents the author's interpretation of the current status of ongoing technical discussions with regards to DC-FRT. A final assessment of the presented options must be based on technical and economical evaluations which cannot be fully concluded in the scope of InterOPERA.

To leave freedom to the vendors to come up with different design strategies, only a DC-LVRT profile is described, and no overcurrent capabilities are prescribed. The actual fault current level in the converter is left unspecified and then depends on the design strategy of the converter's vendor. It can be the result of converter control or of its protection. Converter control requirements for DC grid voltage stability may somehow frame the converter's fault current contribution during a voltage dip. But different technical solutions for converter protection may exist and lead to differentiated fault current contributions. The IGBT components are highly sensitive to overcurrents, and limits may vary depending on the vendor. To protect them, different solutions to limit the increase of converter fault current during DC faults exist:

- The limitation of current increase can be adjusted by means of fault current limiting devices such as DC reactors.
- Some sub-module topologies (e.g. full-bridge) allow to control fault currents.
- For half-bridge topology, innovative temporary blocking can further avoid damage of IGBTs by taking them out of the circuit during transients while ensuring stable operation after DC voltage recovery.

The LVRT profile that the converter shall withstand is meant to be an outer envelope including all realistic undervoltages related to faults in a DC system that do not depend on the converter fault current contribution which is vendor specific and depending on the individual technical solution. This can be at the cost of oversizing.

Connection requirement (CR): The primary requirement of the converter station during a DC-FRT is to stay connected from fault arrival to fault current suppression and to ensure stable operation after DC grid recovery. Hence, any disconnection that leads to permanent loss of active power as for instance the triggering on an ACCB shall be avoided. The connection requirement is ensured by a DC voltage FRT profile which defines a conservative outer envelope related to DC fault transients (see **FIGURE 53**, solid line). Characteristic values are listed in **TABLE 30**. Further reasoning on the determination is provided in the following sub-sections.

Operational requirement (OR): DC faults lead to transients with significant undervoltages at the DC-PoC of the converter. From fault arrival until DC voltage recovery, the converter station is mainly exposed to the fault transients with limited controllability of active power. Imposing continued operation with full controllability would impose major design constraints on the converter even though the purpose is not clear. **Therefore, the operational requirement is limited to the definition of the converter operation after DC voltage recovery: The converter shall continue stable operation after the power system has recovered following fault clearance.** The way the converter respects those requirements is a technical solution, not a requirement[35]. CO, TB or any other intermediate solution is authorized from fault arrival to DC voltage recovery as long as a trip/disconnection on AC or DC side is avoided and stable operation after voltage recovery is guaranteed.

The operational requirement is represented by the dashed lines in **FIGURE 54**. $U_{UV4\text{-}1}$ is a blocking limit under which the converter is allowed to block if no grid serving requirement until fault neutralization is prescribed (see section 7.3.10). $U_{UV4\text{-}2}$ is a voltage limit at which the converter shall be able to deblock[36]. $U_{UV4\text{-}1}$ and $U_{UV4\text{-}2}$ shall be aligned with the dynamic voltage control bands that are defined in section 6.2.2 and the diode rectifier voltage level after fault separation in case of small DC grids. In extended DC grids $U_{UV4\text{-}2}$ is linked to dynamic voltage bands. The diode rectifier voltage condition applies for small DC grids as a worst-case assumption considering temporary blocking of all converters. Note that the number of simultaneously blocking converters can be limited by applying a firewall functionality to individual switching units to ensure limited voltage drop in adjacent sub-grids. The maximum number of simultaneously blocked converters depends on the grid design and risk assessment of the relevant TSO.

It is evident that the converter shall be capable of controlling voltage and current quantities inside dynamic voltage bands and ensure stable operation with absence of blocking. Whenever the converter blocks during a DC-FRT within the CR, deblocking shall be ensured after DC voltage recovery to dynamic voltage bands within a maximum deblocking time ΔT_{dblk}. For the specification of ΔT_{dblk}, maximum fault current suppression times and converter process times for deblocking shall be considered.

Outside of dynamic voltage bands, the converter can ride through the fault by different means: CO, TB or any other intermediate solution is authorized as long as a trip/disconnection on AC or DC side is avoided and stable operation after voltage recovery is guaranteed.

[35] It should be noted that the technical solution shall be compliant with requirements that apply at both AC-PoC and DC-PoC.

[36] It should be noted that the blocking limit $U_{UV4\text{-}1}$ is optional, the converter may or may not block during DC fault transients. This depends on the technical solution and capability of the individual converter. However, if blocked the deblocking above $U_{UV4\text{-}2}$ is mandatory within ΔT_{dblk}.

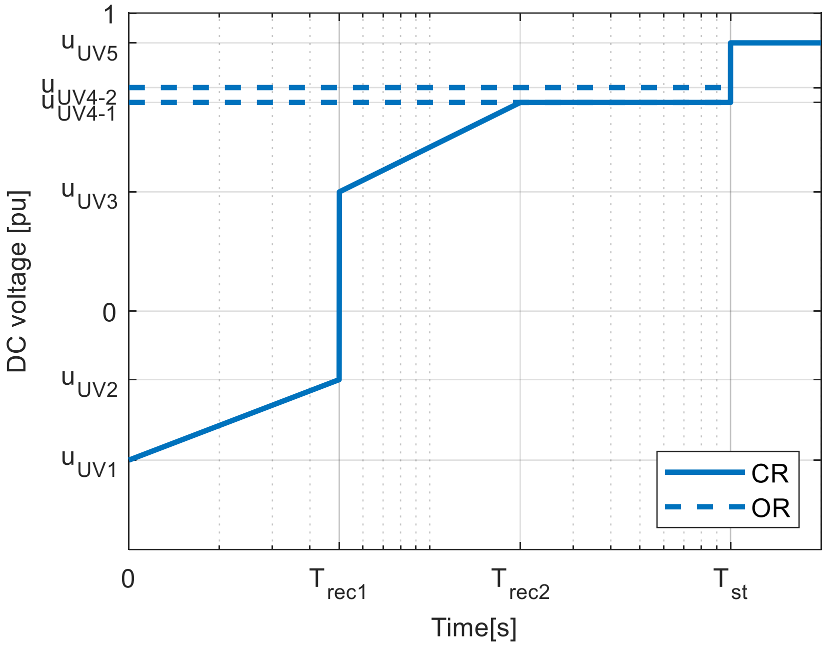


FIGURE 54 DC undervoltage FRT profile at DC-PoC for connection requirement definition, Pole-to-Ground voltages

TABLE 30 Characteristic parameters related to DC-FRT

Parameter	Require-ment	Description	Parameter definition
U_{UV1}	CR	Worst-case undervoltage related to fault arrival considering traveling wave reflection at inductive terminations. k_{TW} is an adjustment factor.	$U_{UV1} = k_{TW}\, UV_{max}$
U_{UV2}	CR	Worst-case undervoltage related to fault arrival considering traveling wave reflection at inductive terminations for distant faults considering cable damping by adjustment factor d_c.	$U_{UV2} = k_{TW}\, d_c\, UV_{max}$
U_{UV3}	CR	Partial instantaneous recovery voltage level after fault neutralization	
U_{UV4-1}	CR & OR	Optional undervoltage blocking limit outside minimum dynamic voltage bands U_{min}^{Dyn} considering a security margin k^{Dyn}. In the transient region, the converter is allowed to block below this limit.	$U_{UV4-1} = k^{Dyn}\, U_{min}^{Dyn}$
U_{UV4-2}	OR	Deblocking threshold after full system voltage recovery to minimum dynamic voltage bands	$U_{UV4-2} = U_{min}^{Dyn}$

		U_{min}^{Dyn}. If the converter is blocked in the transient region, the converter shall deblock above this voltage limit. The deblocking shall be ensured within a maximum deblocking time ΔT_{dblk}.	
U_{UV5}	CR	Full voltage recovery to minimum static voltage bands[37] U_{min}^{Cont} considering a security margin k^{Cont} to avoid unwanted and irreversible converter disconnections.	$U_{UV5} = k^{Cont}\, U_{min}^{Cont}$
T_{rec1}	CR	Maximum partial voltage recovery time related to fault neutralization time[38] $T_{N,max}$ considering a security margin T_b (buffer time). Note: The maximum fault neutralization time may include backup protection. In case of backup protection T_{rec1} would be at least two times the maximum fault neutralization time of the FSD	$T_{rec1} = T_{N,max} + T_b$
T_{rec2}	CR	Maximum full voltage recovery time to dynamic voltage bands	/
T_{st}	CR & OR	Maximum full voltage recovery time to static voltage bands	/
ΔT_{dblk}	OR	Maximum deblocking time after system voltage at DC-PoC reaches dynamic voltage bands. For the specification of ΔT_{dblk}, maximum fault current suppression times and converter process times for deblocking shall be considered.	/

Exceptions

There are exceptions where the DC-FRT profile does not apply, mainly when the activation of the ACCB is part of the protection sequence and a dedicated fault detection and discrimination function is foreseen to immediately trigger the ACCB.

- **Converter station inside FSZ:** The DC-FRT profile does not apply for ordinary contingencies in protection zones which involve ACCB operation. For such faults there shall be dedicated detection function → Immediate trip (see illustrative example in **FIGURE 50**).
- **Internal converter station faults:** The DC-FRT profile does not apply → Immediate trip
- **Backup protection sequences** which lead to an isolation of the converter unit

[37] Static voltage bands to be aligned with static voltage control bands, see section 6.2.
[38] Fault neutralization time includes both relay time and Internal current commutation time

7.3.2 LVRT parameter description

7.3.3 From fault arrival to fault neutralization

This sub-section focusses on characteristic parameters during transients and more precisely from fault arrival to fault neutralization.

T_{rec1}

The maximum fault neutralization time $T_{N,max}$ characterizes the maximum time between fault arrival and full establishment of the Transient Interruption Voltage (TIV) of the FSD including the relay time for fault discrimination. T_{rec1} shall be defined by the system planner in a way that the desired system behaviour is reached while opening up for FSD solutions with different performances. For the definition of T_{rec1} the following points shall be considered:

- Maximum fault neutralization time of a FSD for primary protection
- Maximum fault neutralization time of a FSD for backup protection (if applicable)
- Buffer time (Security margin)

U_{UV1} & U_{UV2}

The LVRT profile should represent an outer envelope including all realistic undervoltages related to faults in a DC system that the converter shall withstand without depending on the specific converter fault current contribution which is vendor specific and without depending on the individual technical solution[39]. The DC-LVRT profile is described based on undervoltages related to fault transients. Considering a DC fault, the most severe voltage drop is not caused by the closest fault but by a fault on a conductor due to traveling wave reflection at the terminal [25]. **FIGURE 55** compares voltage and current evolution for a fault at the cable termination and a distant fault on the cable. The distant fault provokes a voltage reversal at the cable termination which leads to a temporarily steeper increase of fault current.

[39] Connection requirement and associated withstand capabilities mean to avoid any disconnection, the operation itself during fault transients is not specified. For instance, temporary blocking, fault current control or any other mean to withstand the fault transients are allowed.

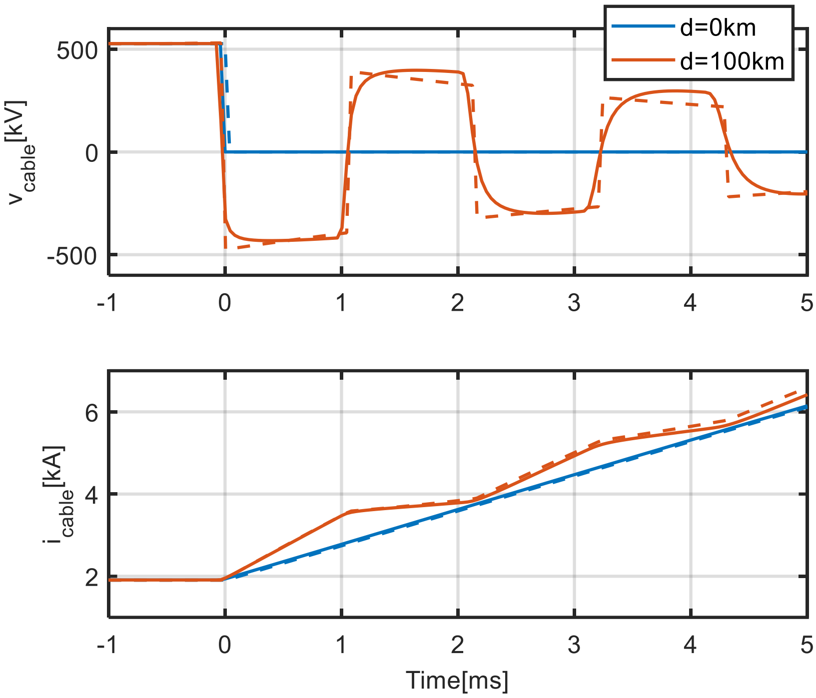


FIGURE 55 Comparison between close fault (blue) and distant cable fault (red); Voltage drop at cable termination (top), DC current evolution (bottom); solid line: frequency dependent cable model, dashed line: traveling wave approximation [25]

Theoretically, the traveling wave reflection at a conductor termination may lead to severe voltage drops of up to 2pu. This gives a first boundary for a conservative outer voltage envelope at the DC-PoC[40] from fault arrival to fault neutralization. It should be noted that a minimum impedance between the DC-PoC of the converter and the fault is not specified. This is mainly due to the fact that the main requirement of the DCSS is to separate the fault in a given time $T_{N,max}$ but a specific device to limit the increase of fault current is not imposed (e.g. a DC reactor). At this stage, it would not be appropriate to restrict the fault current limiting to a specific device or value. With this in mind, the outer voltage band due to fault transients at the cable termination shall be considered as a withstand requirement at the converter DC-PoC. The outer voltage envelope has been assessed by using a simplified traveling wave generating model for various fault distances as shown in **FIGURE 56** for $T_{N,max}$=5ms (more information on the model is provided in [25]). Even though the approach is simplified, and the values have pure illustrative purposes, it shows how an outer voltage envelope for the DC-PoC of the converter can be defined between fault arrival and fault neutralization independently from the converter type. The converter type, rating or control may or may not have an influence on the actual voltage at the DC-PoC but this does not change the outer envelope related to DC fault transients. This outer envelope related to fault transients is represented in the DC-FRT profile shown in **FIGURE 57**.

[40] A requirement on a specific fault current limiting device (type and minimum value) is not defined at DCSS level.

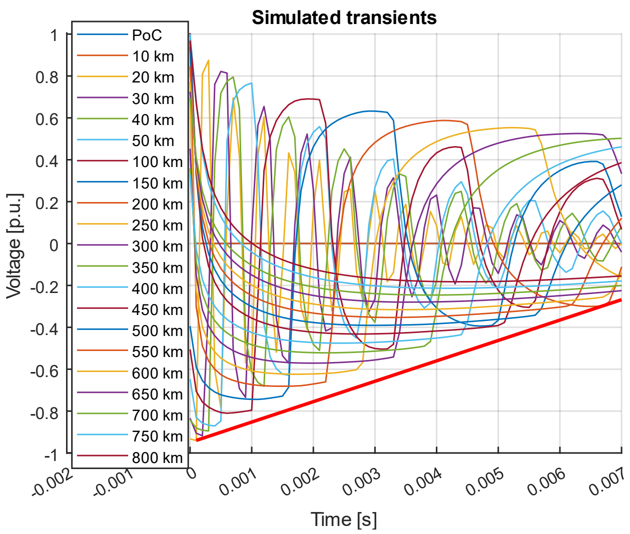


FIGURE 56 Investigation on outer DC voltage envelope using a simplified traveling wave generating model with variation of fault distance for T_{rec1}=7ms (example)

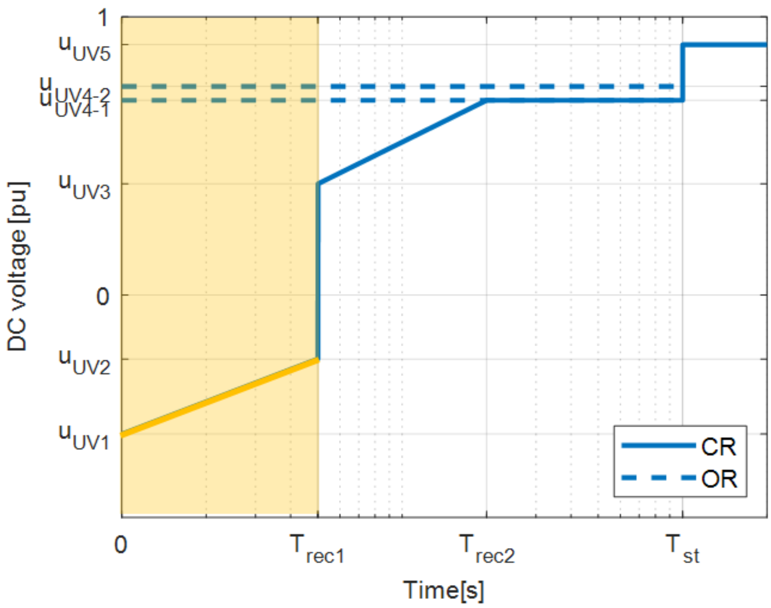


FIGURE 57 Outer voltage envelope defining the converter withstand capability at the DC-PoC from fault arrival to T_{rec1}

Minimum impedances or other considerations which lead to a narrower voltage band during fault transients for U_{UV1} and U_{UV2} may be considered by an adjustment factor $k_{TW} < 1$. For U_{UV2} a damping coefficient of the cable d_c shall be considered. The adjustment factor k_{TW} shall ensure that U_{UV1} and U_{UV2} provide a realistic outer envelope for DC system undervoltages before fault neutralization.

$$U_{UV1} = k_{TW}\, UV_{max}$$

$$U_{UV2} = k_{TW}\, d_c(T_{Nmax})\, UV_{max}$$

7.3.4 Maximum recovery time to dynamic and static voltage bands

DC voltage recovery starts with the full establishment of the TIV. For converters in close vicinity of the fault the imposed TIV leads to an instantaneous increase of voltage at the DC-PoC. For distant converters the voltage drop is likely to be less severe, but the voltage recovery time is longer. The DC-FRT profile shall provide an envelope for both cases, avoiding unnecessary disconnections of converters.

The DC voltage recovery process is specified by the following parameters:

- **U_{UV3} (T_{rec1}):** Minimum voltage recovery level at fault neutralization. In order to keep the voltage FRT profile as simple as possible, there is no time frame associated leading to a vertical representation.
- **$U_{UV4\text{-}1}$**: Optional undervoltage blocking limit outside dynamic voltage bands (see dynamic control bands, section 6.2.2) considering a security margin k^{Dyn}. In the transient region, the converter is allowed to block below this limit.

$$U_{UV4-1} = k^{Dyn}\, U_{min}^{Dyn}$$

- **$U_{UV4\text{-}2}$ (T_{rec2}):** Deblocking threshold after full system voltage recovery to dynamic voltage bands (see dynamic control bands, section 6.2.2). If the converter is blocked in the transient region, the converter shall deblock above this voltage limit. The deblocking shall be ensured within a maximum deblocking time ΔT_{dblk}. (see dynamic control bands, section 6.2.2).

$$U_{UV4-2} = U_{min}^{Dyn}$$

- **U_{UV5} (T_{st}):** Voltage recovery to static voltage bands (see static voltage band ranges, section 6.2.1). A security margin according to the static voltage band can be applied by k^{Cont} to avoid unwanted converter disconnections.

$$U_{UV5} = k^{Cont}\, U_{min}^{Cont}$$

7.3.5 Post-fault power recovery

After DC voltage recovery to dynamic voltage bands, a new post-contingency operational set-point is defined by the P-Vdc characteristic (see section 6.5).Post-fault power recovery requirements shall be coordinated with dynamic response requirements as described in section 6.6.

7.3.6 Converter compliance testing for DC-FRT

This section is intended to provide a guideline to test converter DC-FRT compliance in a standalone test. The expectation on the DC grid equivalent in the context of DC-FRT is to capture the most influential properties of DC fault transients in a generic way while not being restricted to a specific topology or grid design. It is evident that any simplification of the DC grid will inevitably result in the loss of some of the grid specific information or individual subsystem design parameters. An analogy to AC-FRT requirements and dedicated standalone tests with AC Thévenin equivalent can be drawn.

The development of the DC grid equivalent for DC-FRT compliance testing is based on several assumptions which will be detailed in the following. **FIGURE 58** shows an exemplary part of a DC-grid consisting of a converter station with an equivalent DC side inductance L_{dcMMC} connected to a DCSS three additional feeders connecting to other parts of the grid via DC switching units. Inside the switching unit two elements are highlighted in particular as being relevant for protection functions: The DC reactor

Ldc SU as a mean to limit the increase of fault current and the switchgear to connect or disconnect each of the feeders.

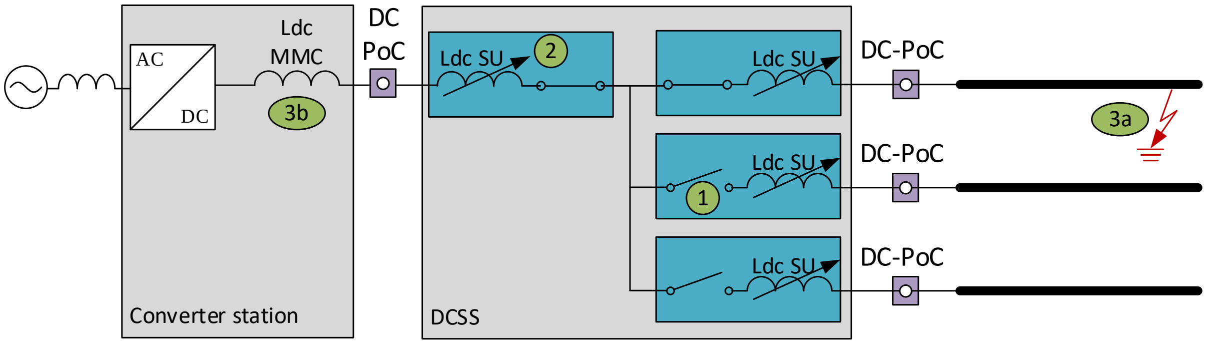


FIGURE 58 Assumptions for converter station standalone test development and DC grid equivalent definition

The numbers in green colour indicate the assumptions and simplifications which will be detailed further below.

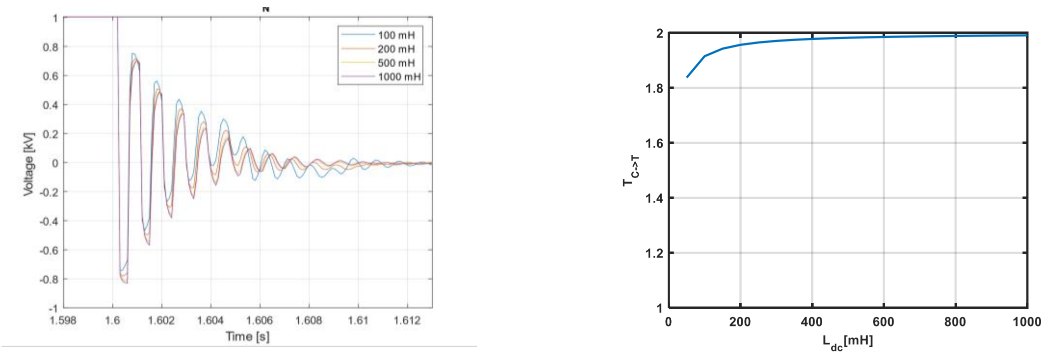
1 The DC-FRT profile shall be applicable for all possible grid configurations. The lowest voltage support and the highest current increase of the converter is expected when adjacent lines are not connected, for example due to maintenance.

2 The DC-FRT test circuit of the converter is functionally decoupled from the DCSS and does not consider any design assumptions of the DC switching station as an input. The DC reactor inside the DCSS is essentially designed to allow fault current interruption without prescribing a fault current limiting requirement (see section 7.4) The worst-case assumption for the converter DC-FRT voltage profile is to have no DC inductance inside the DCSS, for example due to very fast FSDs or other means of fault current limitation. The voltage profile directly applies at the DC-PoC of the converter, no minimum DC impedance is considered between the fault and the converter.

3 DC fault transients

(a) Cable characteristics: Some parameters have an important impact on the damping of the traveling waves leading to a reduction of amplitude of fault transients. The most influential parameter is the screen resistivity and thickness as well as permeability. The DC voltage envelope shall be defined considering cable properties with the lowest damping coefficient [26]. It should be noted that the voltage profiles in this section are obtained based on model assumptions. They could be refined based on cable data from manufacturers.

(b) Distant cable faults may provoke more severe voltage reversals compared to solid faults at the terminal due to the reflection of traveling waves at the converter termination. An approximation of the equivalent impedance can be made based on an RLC circuit as described in [27]. With increasing DC inductance, the transmission coefficient is approaching a value of 2 resulting in a significant amplification of the incoming voltage surge. A transmission coefficient of 2 is considered as a worst-case assumption to guarantee an outer envelope.



(a) (b)

FIGURE 59 (a) Impact of DC inductor size on voltage transients at cable termination after fault at 40km distance; (b) Transmission coefficient approximation at DC-PoC depending on the equivalent DC inductance of the converter; characteristic impedance of DC cable assumed to be 35Ω, $Z_T \approx \omega L$

Considering this, a preliminary minimum test circuit for DC-FRT compliance testing can be defined as depicted in **FIGURE 60**. On the AC side, the system strength and short-circuit ratio shall be represented by an AC Thevenin source. On the DC side a controlled voltage source shall emulate a DC voltage step of pre-defined amplitude $u_{min,avg}$ with a duration of the DC voltage recovery time T_{rec1}. The amplitude is depending on the recovery time as shown in **FIGURE 61**. It is determined by integrating the observed fault transients at the DC-PoC over the DC voltage recovery time. The minimum undervoltages have been obtained simulating various fault distances on a DC cable and selecting the lowest average voltage.

$$u_{min,avg} = \frac{1}{T_{rec1}} \int_{t_1}^{t_1+T_{rec1}} v_{dc}\, dt$$

In the current test set-up, the DC grid impedance is equal to zero. However, the converter DC-FRT only applies for DC faults outside of the converter's own fault separation zone. Consequently, for every fault that is relevant for converter DC-FRT, there is a fault separation device in between the respective converter and the fault location. Depending on the fault current limitation device of the DCSU vendor there may be an inductance inside the DCSU which is currently not considered. Thereby both inductance value and fault neutralization time are assumed as a worst case. If a minimum inductance can be foreseen by the system operator for a given fault neutralization time in the future, this could be considered in the standalone test as a DC grid impedance. This could potentially reduce the design constraints of the converter, imposed by this superposition of both worst-case assumptions.

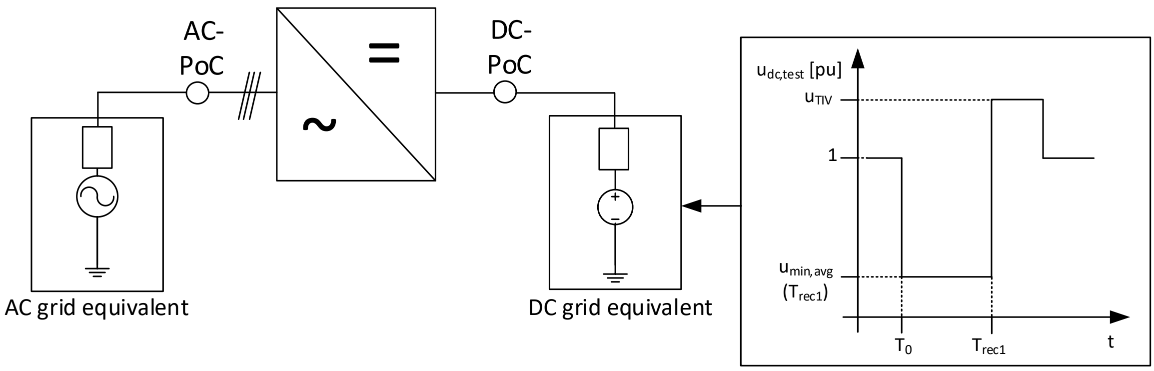


FIGURE 60 Minimum test circuit for converter FRT compliance testing at DC-PoC. All electrical components of the converters including potential DC reactors are considered in the test circuit

Taking hypothetically an example of T_{rec1}=7ms, a voltage step with an amplitude of -0.25pu of DC voltage would be applied to the DC-PoC of the converter over a time of 7ms. The overall goal of the DC-LVRT compliance test is to prove compliance with both the connection requirement and the operational requirement, meaning no trip of ACCB and stable operation after DC voltage recovery.

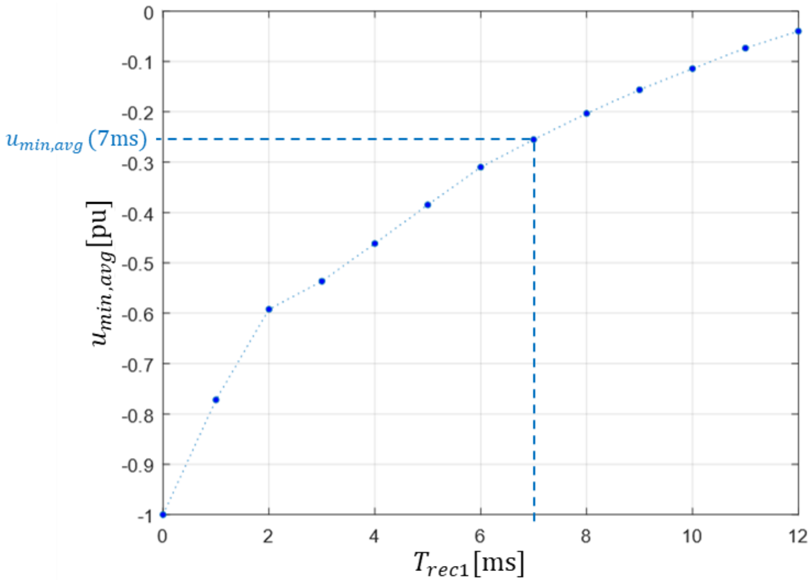


FIGURE 61 Average undervoltage amplitude for DC-FRT compliance testing depending on T_{rec1}; example (blue dashed): Minimum average voltage $u_{min,avg}$=-0.25pu for T_{rec1}=7ms

Different technical solutions inside design space of functional framework

The overall goal of the DC-FRT definition is to describe the requirements in a most technology-agnostic way. The following examples as listed in **TABLE 31** illustrate at a high level how different technical converter solutions (non-exhaustive) meet the requirements.

Converter 1 has no temporary blocking function and no fault current control function.

The requirement of staying connected and ensuring stable operation after fault neutralization can be achieved by proper sizing of the converter DC inductance L_{dcMMC} such that the overcurrent is kept below the IGBT overcurrent capabilities (vendor specific).

Converter 2 has no temporary blocking function but can control fault currents (e.g. due to full-bridge topology).

Due to this functionality, the requirement of remaining connected and ensuring stable operation can be ensured without a specific fault current limiting device and AC side controllability is ensured as well.

Converter 3 has a functionality of temporary blocking, meaning fast deblocking of blocked sub-modules after fault neutralization.

The converter can ensure to continue stable operation after the DC-FRT and fulfils requirements at AC-PoC.

TABLE 31 Example of different technical solutions for converter stations (non-exhaustive)

Converter Technical solution	1	2	3

Temporary blocking function	No	No	Yes
Fault current control function (e.g. Full-bridge topology)	No	Yes	No

7.3.7 Guidelines for DC reactor sizing

Disclaimer: In the presented framework, the choice and the design of fault current limiting devices is subject to the vendor. The following examples tend to provide a guideline for DC reactors inside a converter without advanced functionalities to ride through DC faults. It is further assumed that the converter behaves as a constant DC voltage source. Those guidelines can only serve as an indication where a hypothetical DC overcurrent limit is considered, the actual arm current limit could be different.

To obtain an estimation of the DC reactor the following equation has been used. In this assumption the DC voltage of the converter is assumed to be of rated value $v_{dc,r}$ riding through a voltage step characterized by $u_{min,avg}$ as described above. The results are shown in **FIGURE 62**.

$$L_{MMC} \geq \frac{v_{dc,r} - u_{min,avg}(T_{rec1})}{Idc_{Max,CO} - i_{dc,r}} T_{rec1}$$

- $Idc_{Max,CO}$ is a hypothetical DC overcurrent limit of a converter
- T_{rec1} is the DC voltage recovery time
- $v_{DC,r}$ and $i_{\mathrm{DC,r}}$ are system parameters representing respectively reference DC voltage and DC current. The reference voltage shall represent the upper limit of the steady-state system voltage range (see U_{cont}^{max}, **FIGURE 15**). In this example the values are respectively 525kV and 2kA.
- $u_{min,avg}(\mathrm{T_{rec1}})$ is the step voltage applied to the fault part DC grid equivalent. The amplitude depends on the voltage recovery time (see **FIGURE 61**)

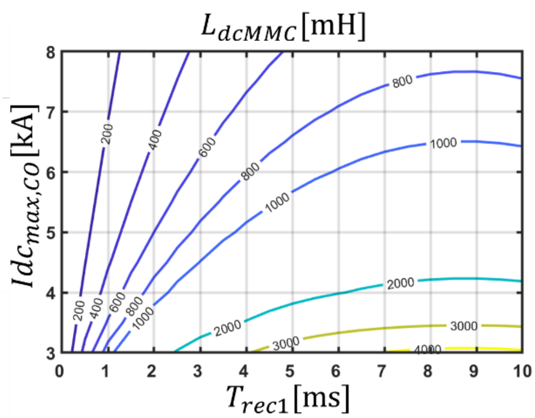


FIGURE 62 Minimum equivalent converter DC inductor size L_{dcMMC} depending on DC voltage recovery time T_{rec1} and maximum overcurrent capability $Idc_{Max,CO}$ considering a rated current of 1,9kA

7.3.8 OVRT requirements

Similar to the LVRT definition, the overvoltage ride through (OVRT) requirements are intended to provide a framework of converter withstand capabilities. An outer envelope of overvoltage levels and time frames related to all critical but planned events in a DC grid shall be specified at the DC-PoC of the converter (see **FIGURE 53**). The converter shall withstand the OVRT specifications while remaining connected and ensure stable operation during the OVRT-event.

All overvoltage levels are defined with reference to ground but not all pole-to-ground overvoltages lead to higher stresses of the converter unit itself. In fact, the actual converter unit voltages stresses are measured with reference to the neutral. This is illustrated by the following non-exhaustive list of critical events for transient and dynamic overvoltage level determination.

Overvoltage on healthy pole during a PtG fault: A PtG fault leads to an inherent increase of the fault current in the faulty pole. The earth return current leads to a conduction of the neutral-to-ground arresters. The voltage level in the neutral rises to the arrester clamping voltage. The offset on the neutral is directly reflected to the healthy pole resulting in an overvoltage with an offset of the arrester clamping voltage. The overvoltage persists until fault current suppression. Note that the pole-to-neutral voltage of the converter unit is not affected by this event.

Overvoltage during fault current/load current suppression: The fault current suppression by an FSD requires to impose a TIV which is higher than the rated DC voltage provoking a decrease of fault current. In case of load current suppression, the conductor under load at the remote end of the FSD imposes an offset to the TIV of the FSD. The voltage across a fault current limiting device (FCLD) such as a DC reactor needs to be considered when assessing realistic overvoltages during current suppression. Further investigation will be included in the final version of the report. It should be noted that this event affects both pole-to-ground and pole-to neutral voltage stresses.

Loss of load: An unexpected loss of load leads to an inherent mismatch between power infeed and export. The imbalance is compensated by reserves of adjacent converter stations and energy absorption devices if reserves are depleted. The converter stations are exposed to dynamic overvoltages during such a loss of load event. It should be noted that this event affects both pole-to-ground and pole-to neutral voltage stresses.

Operation after contingency: After fault separation, the operational voltages may be different to pre-fault set-points which is mainly due to droop adjustments. The converter station is expected to operate in the specified voltage ranges until secondary voltage control frees-up the voltage reserves (see static voltage bands, section 6.2).

The OVRT profile is shown in **FIGURE 63** and characteristic values are given in **TABLE 32**.

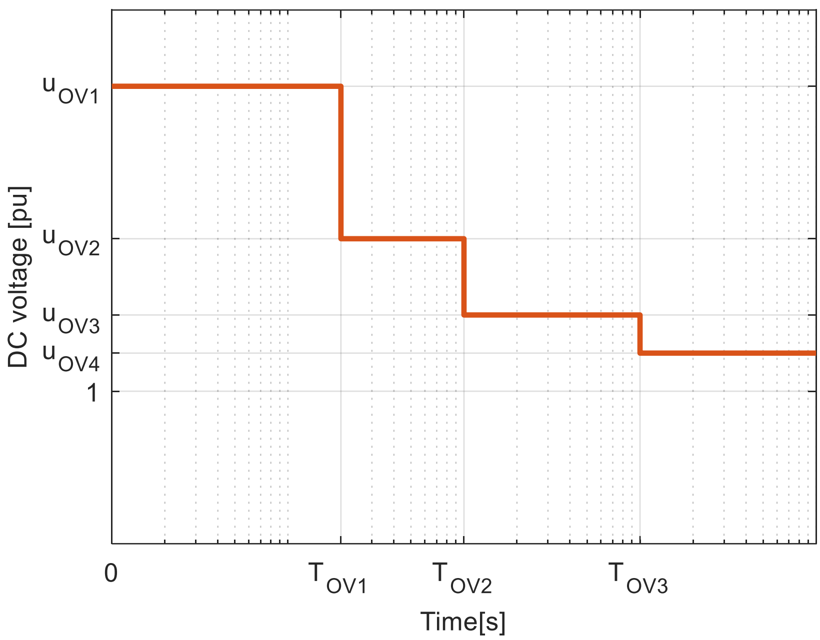


FIGURE 63 OVRT profile for the AC/DC converter station at the DC-PoC (indicative)

TABLE 32 OVRT parameter description for the AC/DC converter station at the DC-PoC (indicative)

Parameter	Description
U_{OV4}	Overvoltage withstand capability related to static voltage bands (see section 6.2)
U_{OV3}	Overvoltage withstand capability related to static continuous voltage bands (see section 6.2)
U_{OV2}	Overvoltage withstand capability related to dynamic voltage bands
U_{OV1}	Overvoltage withstand capability related to transient overvoltages
T_{OV1}	Time frame related to transient overvoltage events
T_{OV2}	Time frame related to dynamic overvoltage events
T_{OV3}	Time frame related to static overvoltage events (Primary control → secondary control)

As stated above, the OVRT profile is a mean to specify overvoltage withstand capabilities of the converter. However, the definition of protective actions when exceeding the OVRT is less evident compared to LVRT, where an inherent action is to trip the ACCB to suppress the fault current. The trip of the ACCB in case of OVRT may not be an effective action since the overvoltage on the DC side will persist. Hence, the overvoltage protection shall be foreseen on the DC side.

7.3.9 On-site application of DC-FRT profile

On-site, the DC-FRT profile is a means for the converter to detect abnormal DC fault transients that are outside the specified times and amplitudes in which the DC grid protection is supposed to operate. This section is intending to clarify on the application and verification of the DC-FRT profile in an MTDC system.

A fault or a contingency in the DC grid results in a voltage deviation at the DC-PoC of the converter. This will determine the triggering time t_0. **FIGURE 64** shows an illustrative undervoltage event of oscillatory behaviour, where multiple transitions between undervoltage and normal voltage bands occur. If not specified, different interpretations for the triggering and reset of an undervoltage event in case of oscillatory behaviour are possible.

- **Trigger voltage level:** Defined as the voltage level at which an undervoltage event is detected by the converter and from which measurements at the DC-PoC are verified against the DC-FRT-profile. The trigger voltage level shall be equal to the highest undervoltage threshold (in this case U_UV5).
- The **reset level** is defined as the minimum voltage recovery level after a LVRT event and associated minimum time from which a new DC-FRT event is considered to occur.
- The **reset time** shall allow to clearly distinguish between a new LVRT event and for instance oscillatory behaviour. An example of possible recurrent LVRT events in a short time frame is a tentative of reclosing after an overhead line fault considering a de-ionisation time of several hundreds of milliseconds. In case of a persistent fault, the reset time shall allow to consider the sub-sequent LVRT event as an independent event.
- The **maximum number of recurrent ride through events** shall be specified and coordinated at least with the number of reclosing tentatives of FSDs.

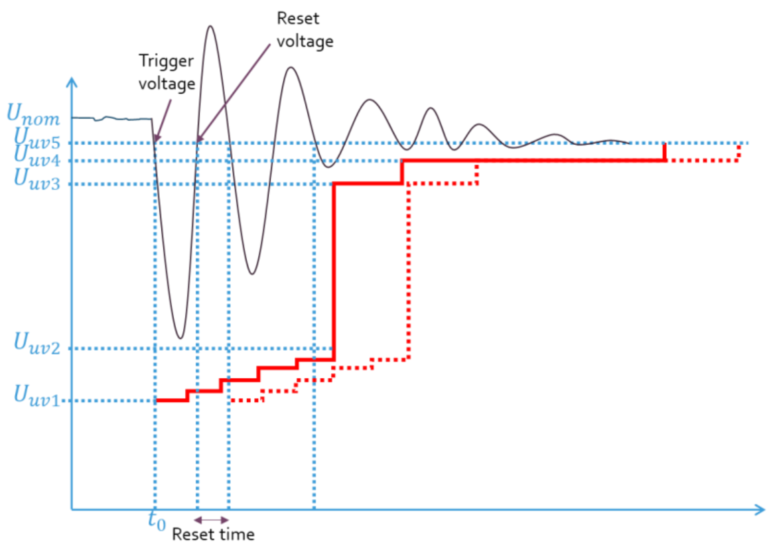


FIGURE 64 Illustration of trigger voltage level, reset voltage and reset time for on-site DC-FRT verification; in this example, the LVRT profile is shown in a discretised format

7.3.10 Grid-serving requirements

Grid-serving requirements describe converter functionalities which support the DC grid during a transient event before fault neutralization. In AC, such functions are specifically designed for the event of a fault (such as reactive current injection for voltage support). Grid-serving requirements may also exist during the DC-FRT of a converter, which would require a certain level of controllability during a DC fault. The need for grid serving requirements and possible definitions could be investigated considering the existing framework of DC grid protection related requirements.

7.4 Fault separation requirements (DCSS)

7.4.1 Software requirements

Protection relays are defined per protected section or zone and not per feeder, they can have access to multiple local current and voltage measurements of multiple switching units. DC fault detection and discrimination functions are defined at unit level. The DC fault detection and discrimination functions shall cover all ordinary contingencies as specified by the relevant TSO. Fault detection and discrimination shall be ensued within a relay time which, together with the FSD operation time, does not exceed the maximum fault neutralization time. If a minimum time between detection (pre-activation) and discrimination is required, this needs to be specified. If the border of a FSZ is on the AC side (e.g. ACCB) or at converter level, a fault detection and discrimination shall be foreseen to activate the fault separation function of such devices.

An overview on communication interfaces related to DC grid protection is provided in **FIGURE 65**. It should be noted that this is a functional view which does not represent the individual system component deployment which might be different.

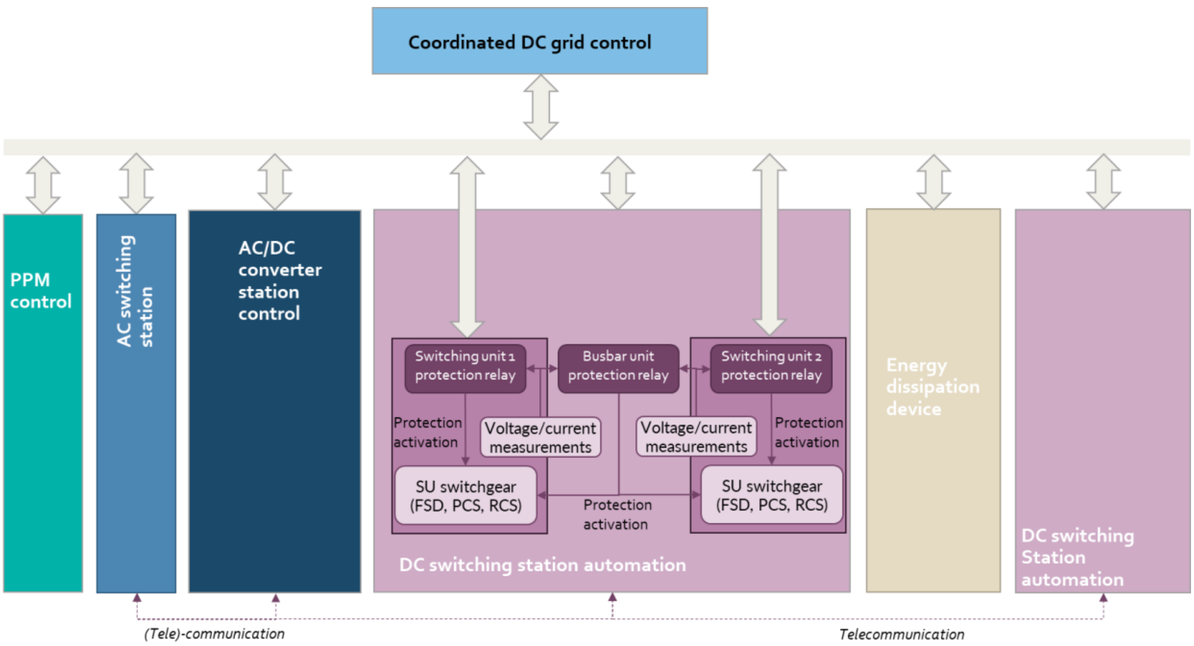


FIGURE 65 Communication interfaces between functional levels for DC grid protection; fault detection/discrimination at unit level, (Tele-)communication between subsystems at station level

Fault detection and discrimination is located at unit level (i.e. switching unit or busbar unit) whereas (tele-) communication interfaces between sub-systems are at station level (e.g. between two DCSS). In practical application, different protection relays may require access to measurement of several devices at field level. For example, protection relays in busbar units will request tripping of the relevant switching units. A switching unit shall be able to send status updates to the DC switching station. If remote information or measurements are needed for the purpose of backup protection, additional fast (tele-) communications with remote end switching stations shall be foreseen.

7.4.1.1 DC fault detection and discrimination

HV pole

The objective of fault discrimination is to distinguish between a fault inside or outside a specified part of an HVDC grid either for fault separation or for fault isolation. A fault separation zone (FSZ) defines a zone in which a fault current can be suppressed by operation of the FSD at the borders of the FSZ. Two different types of FSZ exist: Selective and partially selective (see definitions in section 7.1).

When defining functional requirements related to fault discrimination, the existence of different protection zones shall be considered. It shall be further distinguished between fault discrimination requirements for fault separation and fault isolation as they are not equally critical.

Primary protection for fault separation shall be based on non-unit[41] algorithms whenever technically feasible in order to reduce the relay time. Zone distinction devices (ZDD), e.g. DC reactors, shall be designed accordingly. Non-unit fault discrimination shall be considered as a design criterion for protection zoning. Possible exceptions are an FSZ with several local measurements (e.g. DC busbar), primary protection during maintenance (aggregation of two primary protection zones) and fault isolation.

Backup protection sequences for fault separation at remote ends without telecommunication[42] are technically challenging. For the time being the option of having communication is maintained but communication delays shall be as small as technically possible (e.g. telecommunication via fibre optic link). An overview is provided by **TABLE 33**.

Non-unit fault discrimination is not mandatory for fault isolation because it is less time critical and may be technically challenging. However, whenever technically feasible non-unit fault discrimination shall be prioritized in order to limit horizontal telecommunication interfaces between subsystems.

The method of fault discrimination (non-unit, unit) shall be specified for all relevant protection zones according to the list of ordinary contingencies (including primary and backup protection).

TABLE 33 Authorization of telecommunication for fault discrimination; X: Not allowed, (X): if non-unit protection not technically feasible (intertripping), O: Allowed

	Fault separation	Fault isolation
Primary protection (local)	X	(X)
Backup protection	(X)	O

[41] Non-unit: Single ended fault discrimination without communication; Unit: Double-ended fault discrimination with communication

[42] The term telecommunication is only used for remote-end communication, unit-based algorithms at a busbar are considered local

DMR

The detection and discrimination of DMR faults is less time-critical compared to HV pole faults. A DMR fault may result in a ground return current but the overall system operation is ensured. Therefore, the fault detection and discrimination shall be ensured but in a less restrictive time frame compared to HV pole faults. A unit-based principle relying on communication may be used considering the fact that the detection of DMR faults may be more challenging compared to HV pole faults. This is mainly due to the limited voltage drop in the neutral system which might result in small or even no increase of currents in case of a fault[43].

7.4.1.2 Auto-reclosing

A reclosing after fault current suppression[44] supposes that the faulty element has been isolated and that parts of the FSZ are healthy. Two main reclosing sequences can be distinguished: Auto-reclosing and coordinated reclosing (see **FIGURE 66**). The preferred reclosing sequence shall be specified for each fault separation zone.

The term auto-reclosing is defined as an autonomous reclosing sequence by the switching unit. Dedicated timers for protective auto-reclosing shall be specified and backup actions for the case of auto-reclosure on a fault shall be specified. The maximum number of protective auto-reclosing attempts shall be specified and the energy rating of relevant components (e.g. surge arresters) shall be designed accordingly. The FSD shall be designed for a dedicated reopening sequence in case of persistent fault.

Coordinated reclosing sequences (e.g. for partially selective FSZ) shall be specified at DC grid control level.

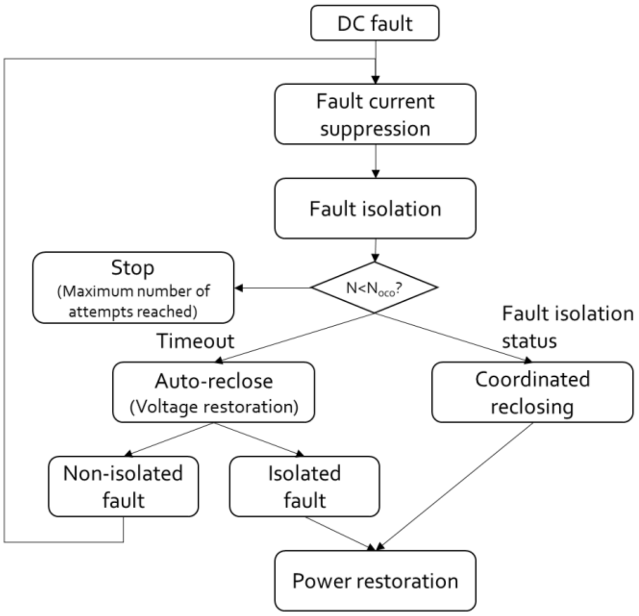


FIGURE 66 Example of reclosing sequences after fault current suppression

7.4.1.3 Monitoring and status for DC grid protection

[43] A fault on an unloaded DMR may lead to zero fault current.

[44] Note that auto-reclosing is not limited to overhead line faults but could also be required in cable based grids (e.g. in case of partially selective FSZ)

The FSD is part of a switching unit. The FSD may be triggered due to a local request by a protection relay or by a global request from the DCGC (corresponding to an open command, as defined in Section 5.3.3). If the FSD trip is issued by a local protection relay, this information is reported to the DCSS and DCGC layers. Beside of the close open and close status, an intermediate state "status closed – FSD activated" is defined for protection sequences. Open commands are distinguished from trip commands such that FSD technologies may apply fault current separation or load current separation sequences (with reduced TIV if applicable).

- Status closed – FSD not activated
- Status closed – FSD activated: Activation of FSD is an intermediate step which lead to fault current separation without galvanic isolation (RCS closed). Possibility to go back to status "closed – FSD not activated" if an auto-reclosing is performed (e.g. in case of an Open-Close-Open sequence (OCO)).
- Status open: Achieved once the RCS has successfully opened providing a galvanic isolation.[45]

Converter operational states to be reported to the DCGC:

- Blocked state[46]
- ACCB activation / trip
- Normal operation

7.4.2 Hardware requirements

7.4.2.1 DC fault separation

The fault current evolution due to a DC fault is highly transient and has various influencing factors such as topology, converter ratings and the type of transmission line. In addition, the presence and sizing of DC reactors or other fault current limiting devices has an important impact on the evolution of fault currents. The DC reactor can be seen as a multi-purpose device ensuring both protection zone distinction and fault current limiting. The choice of fault current limiting devices shall be compliant with the performance of the FSD in terms of current breaking capability and operating time.

The switching unit and more precisely the FSD shall be rated such that it can interrupt all fault currents related to ordinary contingencies as specified by the relevant TSO within the maximum time $T_{N,max}$. A specific list of ordinary contingencies is subject to failure mode analysis and dedicated risk assessment of the relevant TSO. In this context, $T_{N,max}$ may be specified for both primary and backup protection sequences[47].

The FSD shall be equipped with a sufficient energy rating to absorb the maximum energy due to faults. The number of OCO sequences N_{OCO} as specified by the TSO shall be considered for energy absorption rating. If $N_{OCO}>1$, the maximum reclosing time shall be respected. Due to the high interdependencies of fault neutralization time, fault limiting device and current breaking capability, it is recommended to design them in a coordinated way ensuring fault current interruption for all relevant ordinary

[45] Note that an operation of RCS might be required for certain FSD solutions to proceed to auto-reclosure.
[46] For the reporting of a blocked state permanent blocking and temporary blocking shall be distinguished. For temporary blocking no particular action from the DCGC is expected since the converter deblocking is based on local measurements.
[47] Note that $T_{N,max}$ imposes both hardware and software requirements on the FSD as it includes the relay time for fault detection and discrimination. More information is provided in the relevant section.

contingencies[48]. Note that the device for fault current limiting is not specified in order to ensure an inclusive and technology-agnostic description of the functional requirements according to the system needs. From a protection perspective several combinations of protection equipment ratings are possible. However, the impact on the DC grid controllability should be thoroughly investigated to ensure stable operation. Relevant parameters should be specified in a coordinated and compatible way. Functional requirements related to fault separation shall be specified at switching unit level.

7.4.2.2 DC fault isolation

DC fault isolation describes the sequence of physical isolation of the faulty device by operating the RCS after fault current suppression. With the opening of the RCS, the fault current decreases from residual current level to zero current.

Functional requirements regarding residual current breaking capabilities in terms of amplitude and time shall be specified.

7.4.2.3 Auto-reclosing

Hardware requirements related to auto-reclosing shall be specified at switching unit level. The maximum number of auto-reclosing attempts shall be specified. Relevant switchgear and pre-insertion devices shall be designed accordingly.

7.4.2.4 Current withstand capabilities

During DC faults the DC switchgear could be exposed to very high fault currents while the primary or backup protection is operating. The DC switchgear inside a DCSU shall have an overcurrent withstand capability corresponding to the expected fault current amplitudes and durations during protection sequences. It should be noted that the tripping of the ACCB might be part of a protection sequence related to DC faults which might entail longer durations compared to protection actions on the DC side.

7.4.3 Compliance test for DC fault separation

Disclaimer: This standalone test is related to the DC fault separation requirement which could be assigned to a DCSU. It should be noted that other requirements such as maximum current withstand requirements in closed state could be assigned to the same or adjacent DCSU which might require separate compliance tests.

The obvious requirement for switching units inside a DC switching station with fault current breaking capability is to achieve fault current suppression for all associated DC faults considered as ordinary contingencies as specified by the relevant TSO. The expectation on the DC grid equivalent is to capture the most influential properties of DC fault transients in a generic way while not being restricted to a specific topology or grid design. It is evident that any simplification of the DC grid will inevitably result in the loss of some of the grid specific information or individual subsystem design parameters. The standalone tests shall provide a test environment which ensures to verify fault current suppression

[48] This deviates from IEC TS 63291 where a separate specification of fault current limiters and FSD capabilities is proposed.

capability for the relevant types of faults considered as ordinary contingencies. The following simplifications and assumption are made.

1 The DCSS has several DC-PoCs. In case of a fault outside of the DCSS, at least one PoC is connected to the faulty part of the system whereas the remaining PoCs are connected to the healthy parts of the DC grid. For faults within the DCSU all PoC are connected to the healthy system. In an expandable DC grid, the detailed characteristics of each of the feeders might not be known in a planning stage.

2 The maximum increase of fault current occurs when all feeders are connected. As a worst-case assumption in terms of fault current contributions, the healthy part of the DC grid can be represented by an ideal DC voltage source of rated value.

3 DC fault transients

3.1 Cable characteristics: Some parameters have an important impact on the damping of the traveling waves leading to a reduction of amplitude of fault transients [26]. The most influential parameter is the screen resistivity and thickness. The DC voltage envelope shall be defined considering cable properties with the lowest damping coefficient [26] .

3.2 Distant cable faults may provoke more severe voltage reversals compared to solid faults at the terminal due to the reflection of traveling waves at the converter termination. An approximation of the equivalent impedance can be made based on an RLC circuit as described in [27]. With increasing DC inductance, the transmission coefficient is approaching a value of 2 resulting in a significant amplification of the incoming voltage surge. A transmission coefficient of 2 is considered as a worst-case assumption to guarantee an outer envelope (see **FIGURE 60**).

The DUT can be either the DCSS as a whole or an individual switching unit. In the following, standalone test circuits for both DUTs will be defined. It should be noted that the tests are limited to primary protection scenarios. Tests for fault current interruption during backup protection could be specified in addition. The DUT shall be able to handle current interruption according to the defined backup protection strategies.

7.4.3.1 Standalone test for a DC switching unit

A DC switching unit (DCSU) connects external or internal units A and B (see section 5.3.1). Examples for internal units and external units are respectively busbar units and transmission units. For external fault current interruption compliance testing the DC grid equivalent shall represent one of the connected units under fault condition and the remaining units in normal condition. To test internal faults, both units shall be represented under normal conditions. It is recommended to execute at least one standalone test for each of the connected units. A generic standalone test circuit of a DCSU is shown in **FIGURE 68** where one side is connected to DC grid equivalent representing the faulty part and the other side is connected to a DC grid equivalent representing the healthy part. The step voltage of the faulty part is characterised by a voltage step in dependence of the fault neutralization time T_N of the device under test as defined in **FIGURE 67**. This is because the average step voltage may be more severe for faster fault neutralization times. Hence, the test ensures to represent the most severe current increase during the fault neutralization time of the individual DUT.

The test objective is to demonstrate fault current interruption capability within both the specified fault neutralization time $T_N \leq T_{N,max}$ and the current breaking capability i_{cbc}[49]. For a successful compliance test it is expected that the DUT imposes a transient interruption voltage (TIV) at the latest at T_N. The test shall demonstrate successful fault current suppression to residual current.

The faulty part DC grid equivalent consists of a controlled DC voltage source which emulates the outer envelope of fault transients depending on the fault neutralization time T_N of the DUT.

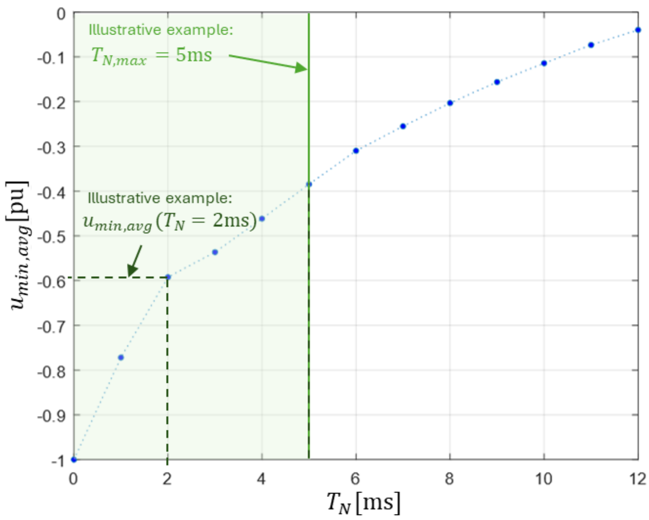


FIGURE 67 Average undervoltage depending on the fault neutralization time of the DUT; Example shows a step voltages of (-0.6pu) applied to the standalone test circuit for a DUT with a fault neutralization time of T_N=2ms considering a maximum fault neutralization time of $T_{N,max}$=5ms

Note that the voltage test profile depends on the unit the DCSU is connected to:

- If the faulty part represents a transmission unit $u_{min,avg}$ shall represent an outer envelope of traveling wave propagations. The step voltage level $u_{min,avg}$ shall be chosen based on **FIGURE 61** while considering T_N.
- If the faulty part represents a busbar unit, $u_{min,avg}$ is equal to zero representing a solid fault.

The healthy part DC grid equivalent is represented by an ideal DC voltage source of reference voltage and an equivalent DC grid impedance. The reference voltage shall represent the upper limit of the steady-state system voltage range (see U_{cont}^{max}, **FIGURE 15**). The DC grid impedance could incorporate effects of different DC grounding schemes and dedicated grounding resistances or minimum DC grid impedances if applicable. In this framework it is assumed that the worst case in terms of fault current increase is covered when considering ideal grounding (0Ω).

[49] It should be noted that fault discrimination is not part of the fault separation test. The relay time for fault discrimination is considered as an additional delay with regards to the internal current commutation time of the DUT

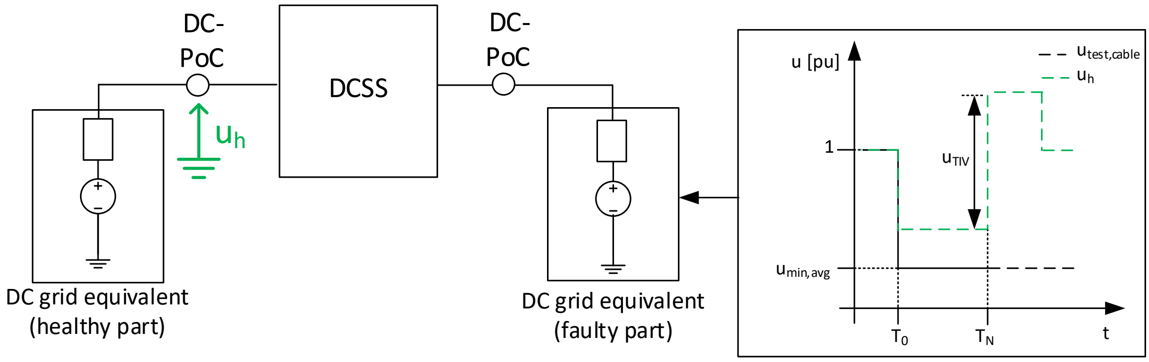


FIGURE 68 Standalone test circuit for fault current interruption considering a DC switching unit as DUT; $u_{dc,test}$: Voltage test profile corresponding to outer envelope of cable fault transients or solid fault depending on connected units, u_h: Indicative expected transient interruption voltage profile imposed by the DUT

7.4.3.2 Standalone test for a DC switching station

In this setup the DC switching station is considered as the subsystem to be tested. The DCSS is likely to integrate several DCSU between two points of connection. The DCSUs may be designed either all equal or with different performances according to the requirements for each of the DCSU. It is possible that some DCSU are equipped with a FSD whereas others are not. The standalone test shall be applied to all DCSU inside a DCSS with fault current interruption. Different to the individual testing, the DCSS vendor can make use of the fault current limiting devices in adjacent feeders as they are part of the test circuit as shown in **FIGURE 69**. In a) an example of a DCSS as a 4-feeder configuration is shown where three out of four DCSU have a fault current interruption capability indicated in blue colour. If all DCSU are identical, an aggregation to an equivalent is possible, where the equivalent inductance can be formulated as $L_{dc,eq} = \frac{L_{dc,SU}}{n}$ with n being the number of adjacent feeders. The representation of the healthy and faulty part DC grid equivalent is identical to the individual testing of a DCSU. The fault current interruption shall be demonstrated for:

- Faults in external units the DCSS is connected to
- Internal faults, for example a fault on an internal busbar unit

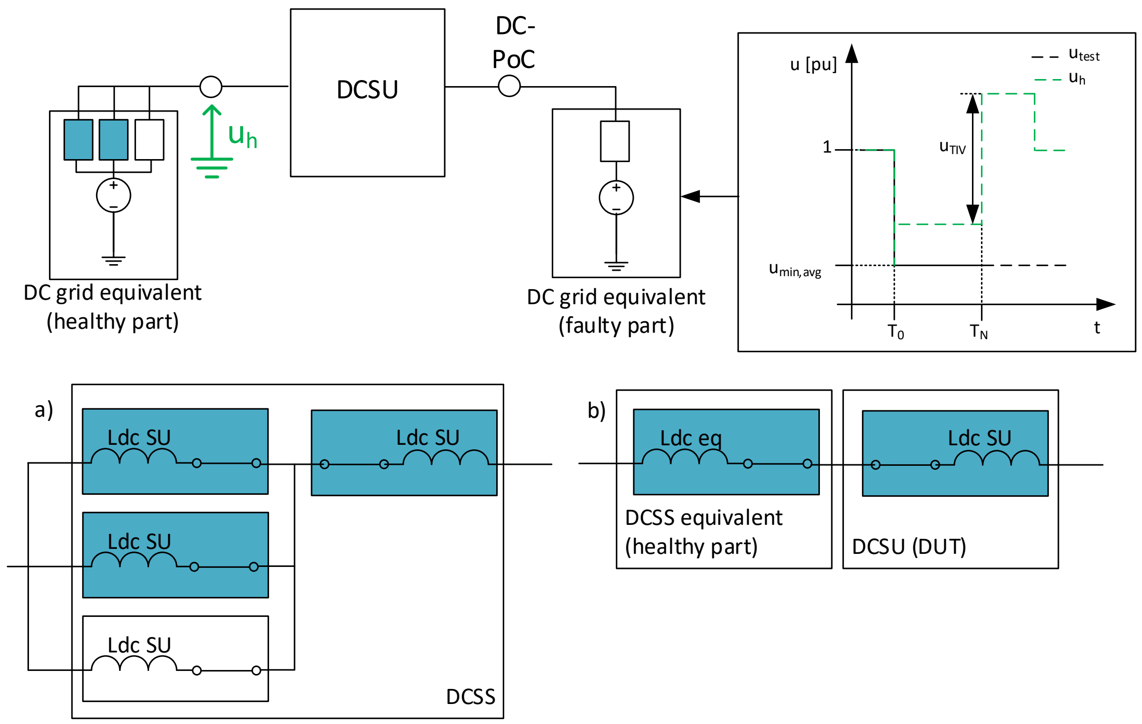


FIGURE 69 Standalone test circuit for fault current interruption considering a DC switching station as DUT, left side connected to healthy part DC grid equivalent, right side connected to faulty part DC grid equivalent; a) Example of a DCSS as a 4-feeder configuration, b) Aggregation of healthy feeders to a single equivalent of the DCSS considering all feeder being designed equally

7.4.3.3 Guidelines for DC reactor sizing

Disclaimer: The choice and the design of fault current limiting devices is subject to the vendor. The following examples tend to provide a guideline for DC reactors inside a DCSU or a DCSS considering different fault neutralization times on the one hand and different current breaking capabilities on the other hand. Those guidelines can only serve as an indication and are specific to a DC reactor as fault current limiting device. To obtain the DC reactor with respect to a given current breaking capability and fault neutralization time, the following equation has been used. The results are shown in **FIGURE 70**.

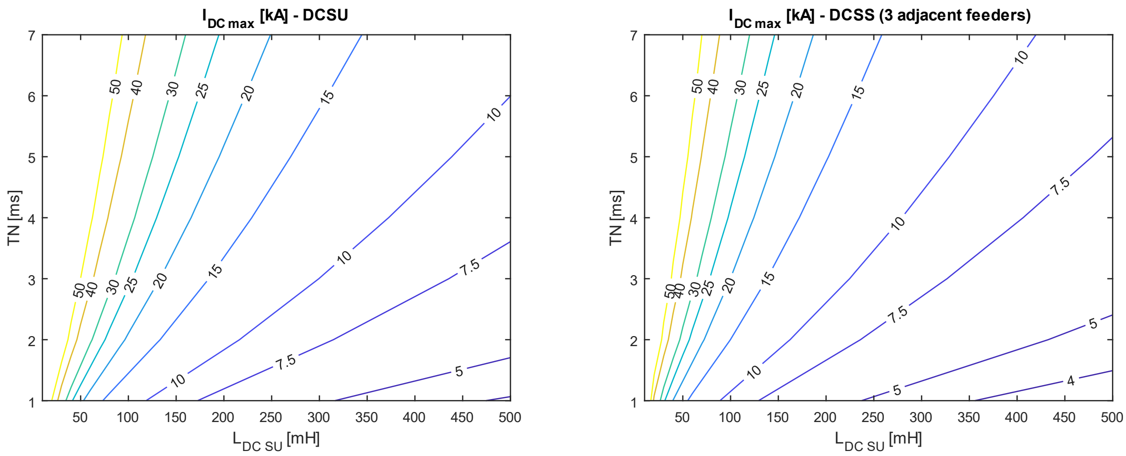
- i_{cbc} and $\mathrm{T_N}$ are respectively the current breaking capability and fault neutralization time, those parameters are specific to the DUT.
- $v_{DC,r}$ and $i_{\mathrm{DC,r}}$ are system parameters representing respectively reference DC voltage and DC current. The reference voltage shall represent the upper limit of the steady-state system voltage range (see U_{cont}^{max}, **FIGURE 15**). In this example the values are respectively 525kV and 2kA.
- $u_{min,avg}(\mathrm{T_N})$ is the test voltage applied to the fault part DC grid equivalent (see **FIGURE 67**)
- n is the number of adjacent feeders equipped with equal DCSUs

For standalone test of individual DCSU (see section 7.4.3.1)

$$L_{DC\,SU} \geq \frac{v_{DC,r} - u_{min,avg}(\mathrm{T_N})}{i_{cbc} - i_{\mathrm{DC,r}}} \cdot \mathrm{T_N}$$

For standalone test of DCSS with equally equipped DCSUs (see section 7.4.3.2)

$$L_{DC\,SU} \geq \frac{v_{DC,r} - u_{min,avg}(\mathrm{T_N})}{(i_{cbc} - i_{\mathrm{DC,r}})(1 + \frac{1}{n})} \cdot \mathrm{T_N}$$



(a) (b)

FIGURE 70 Definition of minimum DC reactor sizes depending on fault neutralization time T_N and current breaking capability i_{CBCi} (a) DUT: DCSU, (b) DCSS with equally designed switching unit, four feeders

Standalone test validation

The following study aims to validate the standalone test definition and in particular the assumptions with regards to healthy and faulty grid representation. Therefore, the current and voltage levels found in a multi-feeder DCSS will be compared to those in the standalone test.

The proposed model of the multi-feeder DCSS is presented in **FIGURE 71**. It is composed of a DCSS with 4 feeders, each feeder connected to a cable and each cable connected to an ideal source. The study is assuming a DCSS with all DCSU having an exemplary fault neutralization time of 5 [ms]. Then, 2 variations as shown in **TABLE 34** will be tested against the standalone test. Case 1 considers equally long cables of 800km connected, whereas case 2 considers variable lengths of adjacent cables.

TABLE 34 Cases proposed for the standalone test validation

Case	L2	L3	L4	Converter
1	800km	800km	800km	disconnected
2	100km	400km	800km	disconnected

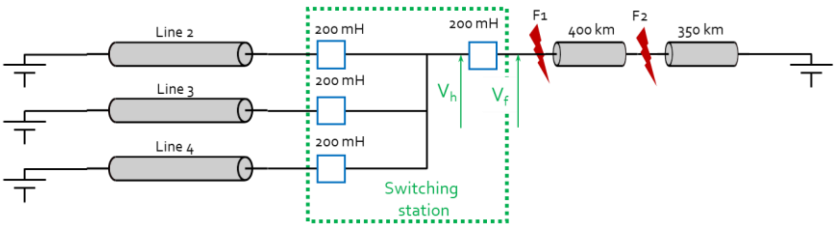


FIGURE 71 Model used to validate the standalone test. A T_N of 5 [ms], and a DCR per DCSU of 200 [mH] are fixed (equivalent of a $I_{CBC} \approx 15$ [kA] following **FIGURE 70**).

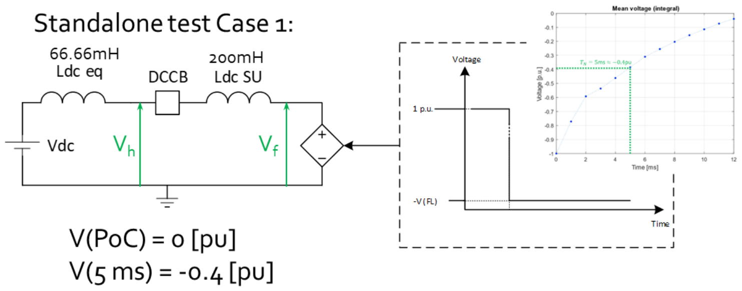


FIGURE 72 Standalone test for a converter station with $T_N = 5$[ms], and V=-0.4[pu]. As an illustrative example, the test is also performed with V=0[pu] to be compared to a fault at the PoC. However, the standalone test used to size a DCSU should use $V(T_N)$.

The standalone test is presented in **FIGURE 72**. Assuming that the DCSS is provided by a single vendor, the healthy side impedance is the equivalent impedance of the known adjacent feeders ($L_{dc\ SU}/3$). The faulted side follows a voltage drop depending on T_N. For a $T_N = 5$ [ms], the equivalent voltage is -0.4 [pu] (see **FIGURE 67**). These hypotheses are presented in Section 7.4.3.2. The standalone test setup is also used in this example with $V = 0$ [pu] to be compared to a fault at the PoC (f1 in **FIGURE 71**). Only the standalone test for case 1 is considered.

The results of this verification are presented in **FIGURE 73** and **FIGURE 74**.

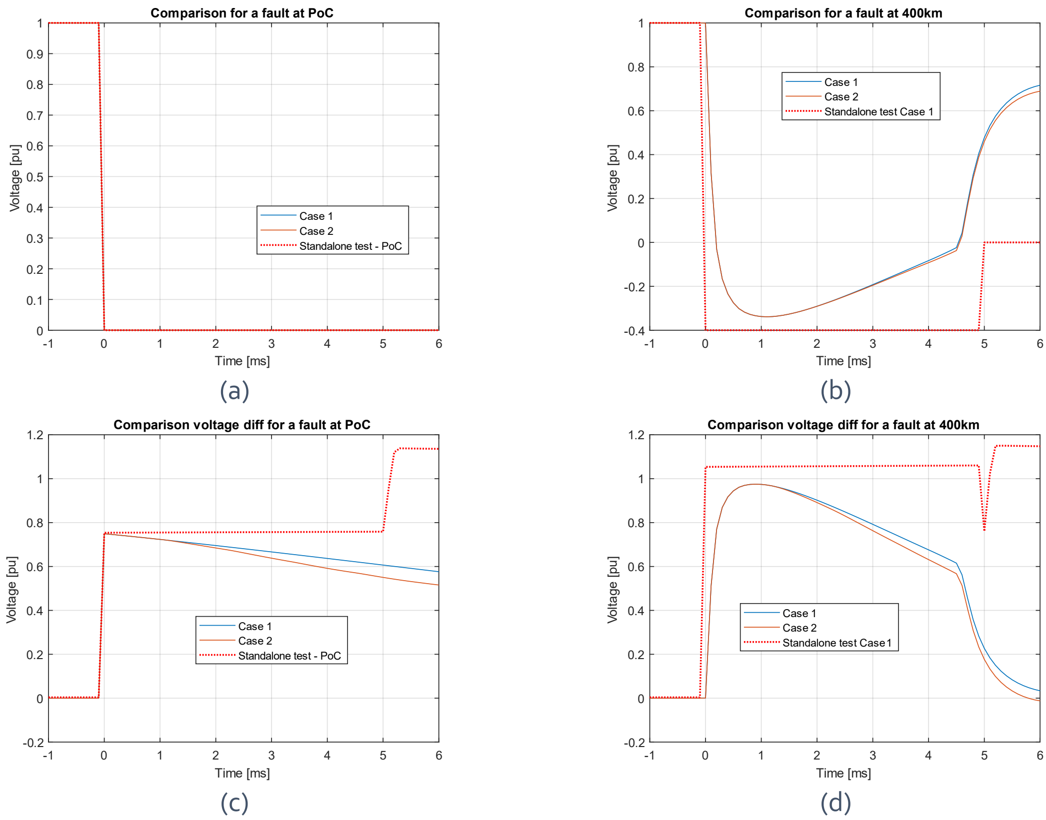
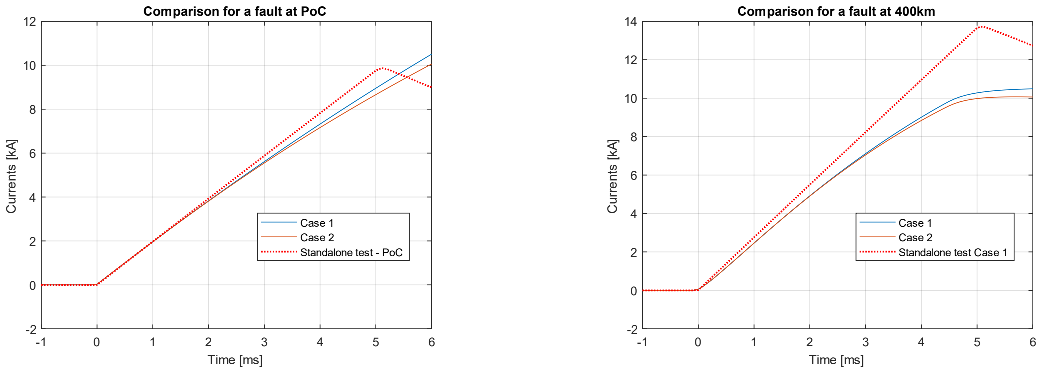


FIGURE 73 Voltage comparison between the standalone test for case 1 and the test system. (a) Voltage at V_f for fault at f1, (b) voltage at V_f for a fault at f2, (c) voltage across the DCSU under test (V_f-V_h) for a fault at f1, and (d) voltage across the DCSU under test (V_f-V_h) for a fault at f2.



(a) (b)

FIGURE 74 Current comparison between the standalone test for case 1 and the results of the 4 cases proposed for (a) fault at the PoC (f1), and (b) fault at 400[km] (f2)

FIGURE 73a presents the voltage at V_f of the DCSU under test (DCSU connected to L1) for cases 1 and 2 and the applied voltage on the standalone test. For this case, there is no difference between the voltages applied, at the faulted side (V_f). The voltages at the terminals of the DCSU under test are presented in **FIGURE 73**c. The difference between the applied voltage on the standalone test and the test system is evidenced. The voltage difference can be explained by two main factors: the simplifications of DC grid equivalent of both, healthy and faulty sides.

Healthy DC grid equivalent: In the standalone test the healthy grid is represented by an ideal stiff DC voltage source and the equivalent impedance of adjacent switching units. In the test system, the stray capacitance of the adjacent cables is limited, leading to a decrease of voltage over time. The cable length has an impact on the equivalent stray capacitance. The decrease of voltage over time is more important for case 2 representing shorter cable lengths. However, regarding **FIGURE 74**a, there is a small difference between the fault current measured in the standalone test (red dotted line) and the test system (blue line). Furthermore, while changing the test system conditions (case 2) the current remains comparable to the current imposed in the standalone test.

Faulty DC grid equivalent: In the standalone test the faulty grid is represented by an equivalent voltage. **FIGURE 73**b and **FIGURE 73**d show the voltages at the faulted line side (V_f) and the voltage across the DCSU under test for a fault at 400 [km]. In this case, there is a noticeable difference between the voltage used in the standalone test and the voltage measured in the test system. This is mainly due to the conservative assumptions made for the standalone test, which provide the worst conditions to size the DCSU ensuring interoperability (see Section 7.4.3). This difference is also noticeable when comparing the currents (red dotted and blue lines) in **FIGURE 74**b. However, for the sake of this study the voltage and currents gaps are considered to be acceptable, ensuring a generic standalone test definition without depending on the actual design of the DCSU under test.

7.5 Coordination between DC-FRT and fault separation requirements

The DC voltage recovery time needs to be carefully coordinated with the maximum fault neutralization time leading to the minimum requirement $T_{rec1} \geq T_{N,max}$. It is evident that the DC voltage can only recover after relevant protection actions have effectively separated the fault from the healthy part of the system.

In that sense, T_{rec1} and $T_{N,max}$ are global parameters for a given HVDC grid or sub-grid. This means that for all converters in a subgrid, the same DC-FRT profile is prescribed for converters and the same maximum fault neutralization time need to be respected by all DCSS vendors.

A sub-grid is characterized by being connected to other sub-grids with different functional specifications at one or several connection points. Assuming an HVDC grid which consists of two subgrids connected via one connection point as shown in **FIGURE 75**, it is possible to have different protection requirements defined for the upper and the lower sub-grid as long as they are identical within the subgrid.

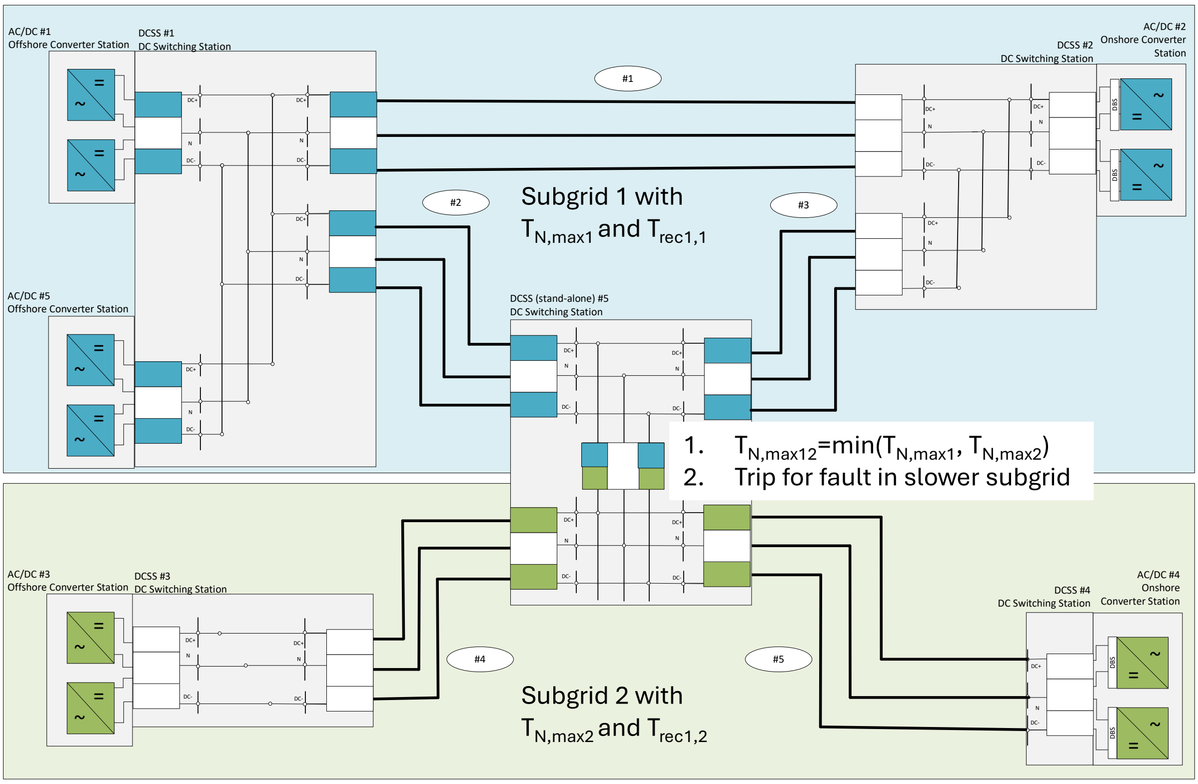


FIGURE 75 Definition of $T_{N,max}$ and T_{rec1} as a global parameter of individual subgrids with a $T_{N,max12}$ at the connection point being the minimum out of both $T_{N,max}$ to be compliant with both voltage recovery times T_{rec1} of sub-grids.

In the following preliminary recommendations for additional requirements at connection points are considered.

- All DCSUs in subgrid 1 and subgrid 2 need to neutralize the fault within a time equal or faster than T_{Nmax1} and T_{Nmax2} respectively. In both subgrids, the minimum condition applies: $T_{rec1,1} \geq T_{N,max1}$ and $T_{rec1,2} \geq T_{N,max2}$.
- When connecting those two grids, the FSDs at such connection points need to ensure at least that the lower fault neutralization time out of both sub-grids is respected (1).
  - The DCSU at the connection point need to operate as a primary protection device to separate the subgrids for any fault in the subgrid with high fault neutralization time (2). The DCSU could be reclosed after after fault neutralization in the subgrid under fault. In this case, no support from the adjacent subgrid can be expected and the subgrid shall be able to reach normal operating conditions when separated. The dedicated protection relay shall be able to detect all faults in the subgrid.

> If the fault occurs in the subgrid of fast fault neutralization time, the DCSU at the connection point does not need to operate for primary protection purpose but could be foreseen as a backup protection.

This ensures that the DC voltage recovery time in both subgrids is respected for any fault in the interconnected system. It should be noted that other requirements may need to be defined to ensure the interoperability between two functionally independent subgrids.

7.6 Insulation coordination

Insulation coordination involves the selection of insulation levels of HVDC components and the choice of equipment (e.g. surge arresters) that minimize the impact of overvoltages resulting from switching operations, faults and lightning impulses.

Within T2.1 a screening of the state of the art of insulation coordination and the existing standards was carried out and is provided hereafter. No functional requirements are proposed at this stage. Ongoing challenges are pointed out and guidelines for continuing the study on the subject are provided. Insulation coordination studies and related simulations are not scope of this section.

7.6.1 State of the art

IEC standards

IEC standard 60071-1 [28] defines the term insulation coordination as follows: "selection of the dielectric strength of equipment in relation to the operating voltages and overvoltages which can appear on the system for which the equipment is intended and taking into account the service environment and the characteristics of the available preventing and protective devices".

IEC 60071-1 applies to high voltage three-phase AC systems and it specifies the procedure for the selection of the rated withstand voltages for the phase-to-earth, phase-to-phase and longitudinal insulation of the equipment. It also gives the lists of the standard withstand voltages from which the rated withstand voltages should be selected.

Regarding the insulation coordination for HVDC system, the reference standard was the IEC 60071-5 "Procedures for high-voltage direct current (HVDC) converter stations" which covered LCC converter station type (VSC were excluded). Due to the increasing number of HVDC projects based on VSC converters, in October 2016, IEC Technical Committee 28 (Insulation co-ordination) established AHG 8 (Ad hoc group 8) to make the roadmap for HVDC system insulation co-ordination standards. A new series standard for HVDC system has been established:

- **IEC 60071-11** [29]: "Definitions, principles and rules for HVDC system"; It specifies the principles on the procedures for the determination of the specified withstand voltages, creepage distance and air clearances for the equipment and the installations of these systems.
- **IEC 60071-12**: [30] " Application guidelines for LCC HVDC converter stations". This part of IEC 60071 applies guidelines on the procedures for insulation co-ordination of line commutated converter (LCC) stations for high-voltage direct current (HVDC) project, whose aim is evaluating the overvoltage stresses on the converter station equipment subjected to combined DC, AC power frequency, harmonic and impulse voltages, and determining the specified withstand voltages for equipment.

- **IEC 60071-13**: "Application guidelines for VSC HVDC converter stations", not yet available.
- **IEC 60071-14**: "Insulation co-ordination for AC/DC filters", not yet available.
- **IEC 60071-15**: "Insulation co-ordination for DC transmission line", not yet available.

IEC 60071-11 currently stands as the reference document regarded as the state of the art for HVDC insulation coordination. It is noteworthy that, despite the initiation of this new series of standards for HVDC systems, a standard for HVDC switching stations is not anticipated.

Voltage levels

In IEC 60071-11 it is mentioned that the nominal voltage, nominal current and insulation levels for HVDC system are not yet as standardized as the AC system. **FIGURE 76** shows an extract of the annex C of IEC 60071-11 which proposes indicative insulations levels for DC voltages between 200 kV and 800 kV for outdoor installation.

Table C.1 – Typical DC voltages and switching/lightning impulse withstand voltage

Typical DC voltage kV	Presumed rated switching impulse withstand voltage kV (peak value)	Presumed rated lightning impulse withstand voltage kV (peak value)
200	550	550
		650
250	550	550
		650
	650	650
		750
320	650	650
		750
	750	750
		850
	850	850
		950
400	850	850
		950
	950	950
		1 050
		1 175
500/525[a]	950	950
		1 050
	1 050	1 050
		1 175
	1 175	1 175
		1 300
		1 425
600	1 175	1 175
		1 300
	1 300	1 300
		1 425
	1 425	1 425
		1 550
800	1 550	1 550
		1 675
	1 675	1 675
		1 800
		1 950
The corresponding values shall be chosen depending on the specific system configuration.		
[a] Either of 500 kV or 525 kV is applicable.		

FIGURE 76: Extract of Table C.1 of Annex C, IEC-60071-11, Typical DC voltages and switching/lightning impulse withstand voltage

General procedure for insulation coordination

The IEC60071-11 proposes a general procedure for the choice of voltage insulation levels for AC system, see **FIGURE 77**. Voltage stresses can be minimized by using surge arrester, insertion resistors in switching devices, DBS, controlled closing, low impedance grounding, etc.

FIGURE 77: Simplified view of procedure for the determination of voltage withstand levels coordination procedure proposed by the IEC 60071-11

The amplitude, shape, and duration of voltage stresses are generally determined using system transient analyses. Transient analysis results should identify voltage stresses as depicted in **FIGURE 78** for pole-to-ground, pole-to-pole, pole-to-neutral, neutral-to-ground overvoltages and longitudinal overvoltages (voltage appearing between open switch contacts). EMT simulations will be required to quantify transient overvoltages within the system. Due to the limited experience with MTDC grids, special attention will be required to accurately model the HVDC system equipment as well as the AC side and determine the appropriate level of possible modelling simplification.

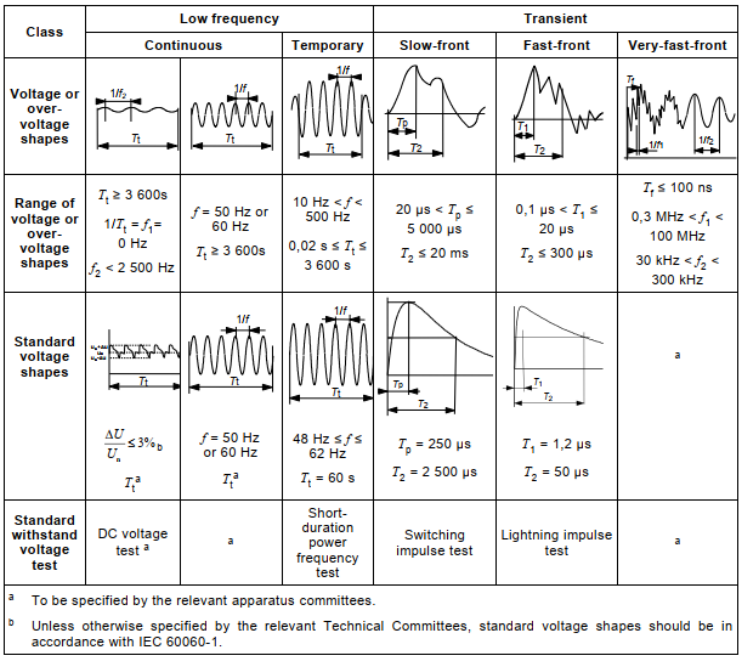


Table 1 – Classes and shapes of overvoltages, standard voltage shapes and standard withstand voltage tests

Class	Low frequency			Transient		
	Continuous		Temporary	Slow-front	Fast-front	Very-fast-front
Voltage or over-voltage shapes						
Range of voltage or over-voltage shapes	$T_t \geq 3\ 600$s $1/T_t = f_1 =$ 0 Hz $f_2 < 2\ 500$ Hz	f = 50 Hz or 60 Hz $T_t \geq 3\ 600$s	10 Hz $< f <$ 500 Hz 0,02 s $\leq T_t \leq$ 3 600 s	20 μs $< T_p \leq$ 5 000 μs $T_2 \leq$ 20 ms	0,1 μs $< T_1 \leq$ 20 μs $T_2 \leq$ 300 μs	$T_f \leq$ 100 ns 0,3 MHz $< f_1 <$ 100 MHz 30 kHz $< f_2 <$ 300 kHz
Standard voltage shapes	$\frac{\Delta U}{U_n} \leq 3\%$ [b] T_t [a]	f = 50 Hz or 60 Hz T_t [a]	48 Hz $\leq f \leq$ 62 Hz T_t = 60 s	T_p = 250 μs T_2 = 2 500 μs	T_1 = 1,2 μs T_2 = 50 μs	a
Standard withstand voltage test	DC voltage test [a]	a	Short-duration power frequency test	Switching impulse test	Lightning impulse test	a

[a] To be specified by the relevant apparatus committees.

[b] Unless otherwise specified by the relevant Technical Committees, standard voltage shapes should be in accordance with IEC 60060-1.

FIGURE 78: Classes and shapes of overvoltages (Table 1 of IEC-60071-11)

The standard IEC 60071-11 defines the maximum overvoltages that would be limited by the surge arresters considering the corresponding Switching Impulse Protective Level (SIPL), lightning impulse protective level (LIPL) and Steep-Front Impulse Protective Level (STIPL). A margin between the maximum calculated overvoltages to be expected (considering the protecting devices) and the equipment withstand level is proposed by the standard. Those margins consider several aspects such as data and model limitations, surge arrester ageing and characteristics tolerances and are shown in **FIGURE 79**. It is worth to note that the way aging of the equipment is managed (decrease of the withstand voltage versus time) is not clear in DC. The choice of lightning impulse and switching impulse withstand level of subsystem, see **FIGURE 6**, should at the end be higher or equal to the Required Switching Impulse Withstand Voltage (RSIWV) as per IEC 60071-11, Required Lightning Impulse Withstand Voltage (RLIWV), Required Steep-Front Impulse Withstand Voltage (RSTIWV). **FIGURE 80** shows an example of a solidly earthed system with correctly dimensioned arresters for the different overvoltage regions: the arresters limit the slow front, fast front and temporary overvoltages below the equipment withstand voltages.

Table 3 – Indicative values of ratios of required impulse withstand voltage to impulse protective level

Type of equipment	Indicative values of required impulse withstand voltage/impulse protective level[a, c]		
	RSIWV/SIPL	RLIWV/LIPL	RSFIWV/STIPL[b]
AC switchyard – busbars, outdoor insulators, and other conventional equipment	1,20	1,25	1,25
AC filter components	1,15	1,25	1,25
Transformers (in oil)			
line side	1,20	1,25	1,25
valve side	1,15	1,20	1,25
Converter valves	1,15	1,15	1,20
DC valve hall equipment	1,15	1,15	1,25
DC switchyard equipment (including DC filters etc. and DC reactor)	1,15	1,20	1,25

[a] Indicated values are stated for general design objectives only. Appropriate final ratios (higher or lower) can be selected according to the chosen performance criteria.

[b] STIPL for LCC valve arresters.

[c] Indicative ratios are on the basis that any equipment is directly protected with a surge arrester.

FIGURE 79: Table 3 IEC-60071-11, Indicative values of ratios of required impulse withstand voltage to impulse protective level

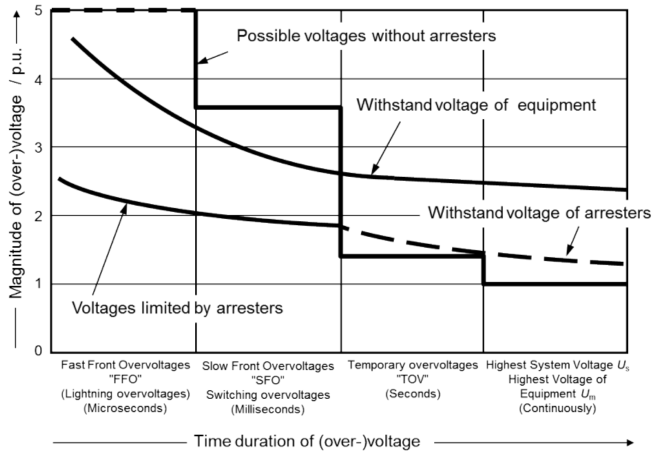


FIGURE 80: from IEC-60099-05 [31], example of a solidly earthed system with correctly dimensioned arresters.

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General principles for the application of surge arresters

The principle of insulation coordination for a power system is given in the standard IEC 60071-11. The IEC 60099-5, "Surge arresters – Part 5: Selection and application recommendations" proposes general principles for the application of surge arrester coordination for AC system, see **FIGURE 81**. Selecting a surge arrester for a specific application is a compromise between its protective level, TOV capability and energy dissipation capability [32]. Increasing the TOV capability (e.g. higher SA rated voltage) increases the possibility of the SA to survive temporary system overvoltages but reduces the margin of protection provided by the SA for a given insulation level. Higher SA energy rating reduces the risk of failure, but it means increased cost.

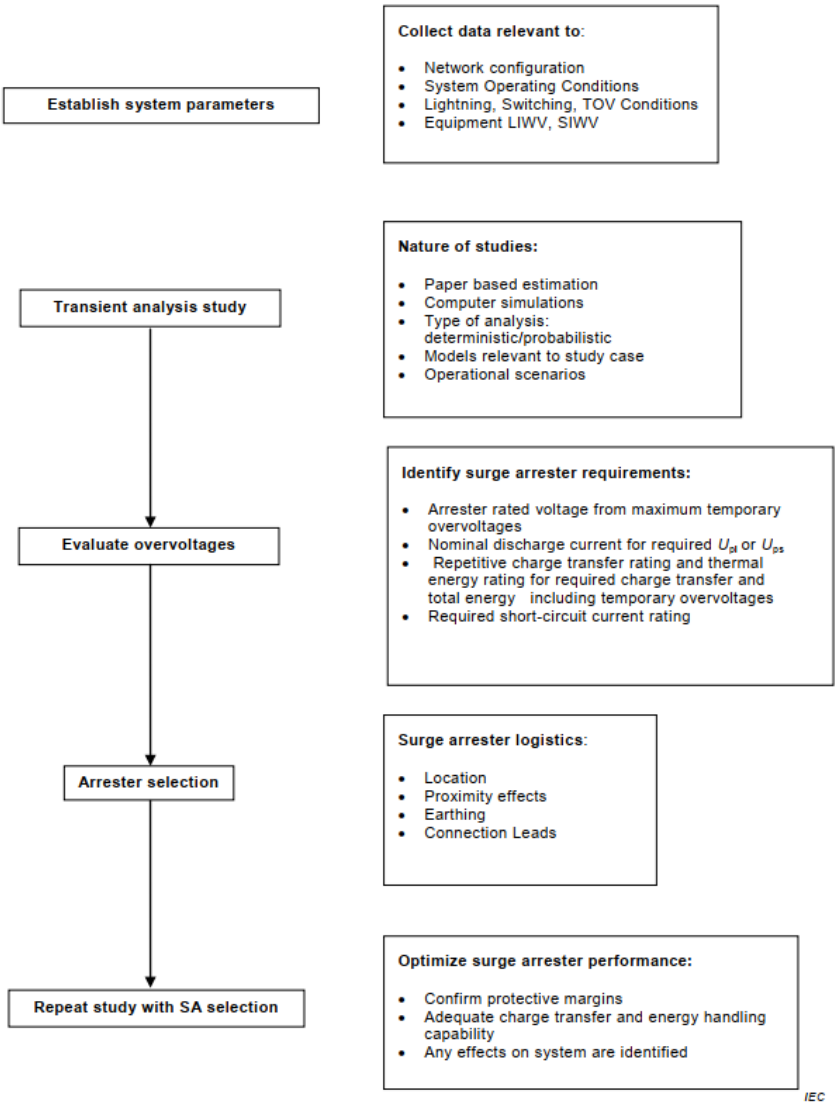

FIGURE 81: IEC-60099-05, Typical procedure for a surge arrester insulation coordination study for AC system.

FIGURE 81 shows the procedure for SA rating selection for AC system as proposed by [32].

- Choice of Uc: the SA continuous operating voltage, For AC system, Uc is defined as the designated permissible rms value of power-frequency voltage that can be continuously applied between the SA terminals[50].
- Choice of Ur: the SA rated voltage, Ur, is the maximum permissible rms. value of power-frequency voltage between its terminals at which it is designed to operate correctly under temporary overvoltage conditions. It is worth noting that different SA could have same continuous operating voltage Uc but different rating voltage Ur if they are designed for the same system voltage but they for different TOV amplitude and duration.
- Choice of SA protective level: as already mentioned above, the protective level of the SA has to be chosen by means of insulation coordination procedure as proposed by IEC 60071-1. The most important parameters relevant in this process are the prospective amplitude of overvoltages, number and position of SA, the insulation level of protected equipment, safety margin for equipment insulation.
- Selection of energy capability: the energy stresses for temporary, slow front and fast front overvoltages has to be calculated as a function of the arrester protective level and current duration. IEC 60099-5 introduced two ratings regarding energy absorption capabilities from 2014 forth on. The repetitive charge transfer rating, which defines the maximum charge transfer of a single impulse or multiple impulses within 2 seconds the arrester can handle. The thermal energy absorption, which a surge arrester can absorb within 3 minutes. Both ratings have to be ensured during insulation coordination processes.

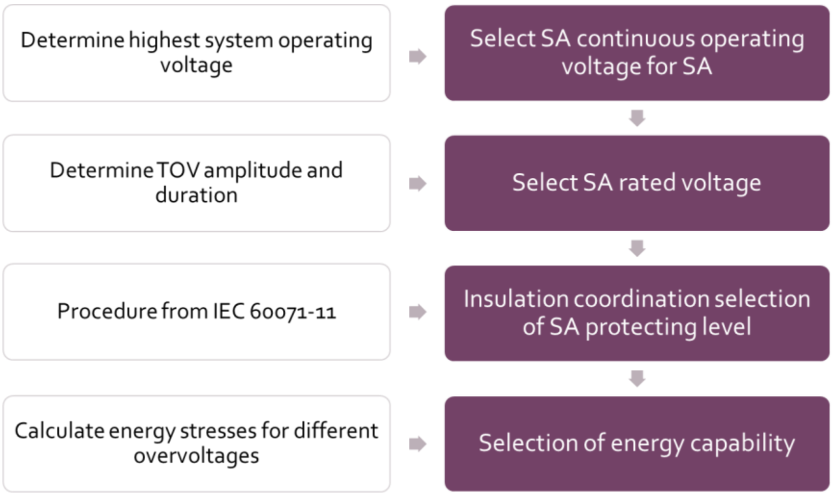

FIGURE 82: Procedure for surge arrester choice, based on [32]

TB CIGRE 471

The CIGRE Working Group B4.71 "Application guide for the insulation coordination of Voltage Source Converter HVDC (VSC HVDC) stations", will deliver a Technical Brochure TB 471. The document will present typical causes of overvoltages within a VSC converter station and will include a section regarding surge arrester arrangement within the station. Nevertheless, the insulation coordination related to multi-terminal HVDC grids based on bipolar configuration and including DC circuit breakers is not covered.

[50] Note that for DC system, the relevant IEC standard is the IEC 60099-9: Metal-oxide surge arresters without gaps for HVDC converter stations.

Identified gaps

The following are a list of identified gaps of existing literature toward the definition of a methodology and rules for insulation coordination for MTDC HVDC grids:

- The insulation coordination methodology for HVDC system proposed within IEC 60071-11 is directly derived from the AC insulation coordination. The application of this methodology for future HVDC grid based on bipolar system need to be reevaluated considering the framework of multi terminal and multi vendor DC grid.
- Values for switching and lightning impulses withstand levels for HVDC components are not yet standardised. In the offshore context this is particularly important for HVDC cable, for which temporary overvoltages withstand levels are not yet standardised.
- There are no rules that clearly state the adequate placement of surge arresters within the grid, neither who has the responsibility to define it.
- An exhaustive mapping of possible voltage stresses that can occur within a bipolar HVDC grid, including switching actions for load or fault current interruption by DC circuit breakers is missing in literature.

7.6.2 Discussions

This section covers a selection of drivers and problems that can be further investigated to help defining a methodology for insulation coordination for MTDC grids.

Grounding

The type of grounding of neutral of the system has a direct impact on the insulation coordination for poles and DMR. A higher grounding resistance and surge arrester protective level at the neutral leads to higher temporary overvoltages at the poles and DMR.

Cable OV

Cables are considered one of the weak points in HVDC subsystems when it comes to dielectric insulation withstand. The CIGRE Technical Brochure TB 852, titled "Recommendations for Testing DC Extruded Cable Systems for Power Transmission at a Rated Voltage up to and Including 800 kV," outlines the tests to be performed to ensure temporary overvoltages for the cables:

- Switching impulse same polarity
- Switching impulse opposite polarity
- Lightning impulse
- Very slow front Temporary Over Voltage (TOV)
- Very slow front TOV with chopped tail
- Zero crossing damped temporary overvoltage

TB 852 primarily focuses on point-to-point HVDC symmetric monopolar systems. Therefore, additional research is recommended for multi-terminal HVDC grids based on bipolar systems. It is important to note that, at present, the quantification of parameters of temporary overvoltages are not standardized, and different HVDC point-to-point systems may have different parameters. As an illustrative example, **FIGURE 83** shows the very slow temporary overvoltage profile and parameters proposed in TB 852.

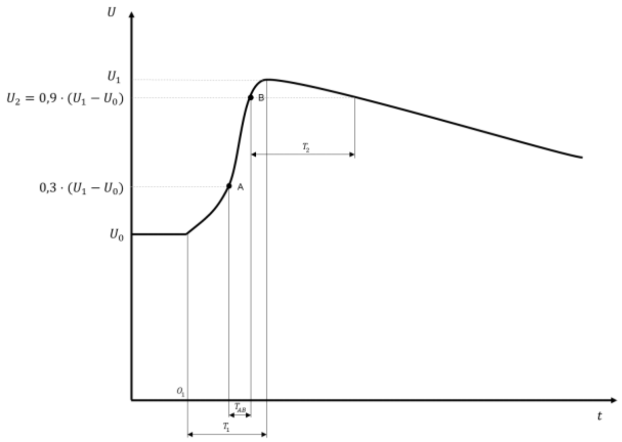

FIGURE 83: Very slow temporary overvoltage profile and parameters proposed in TB 852

The overvoltages profiles proposed by the TB 852 are very specific to point-to-point systems and cannot be used directly. Nevertheless, they could be used as starting point for insulation coordination studies for MTDC grid, and, on the other way, the insulation coordination studies can give recommendation for cable overvoltages withstand.

Interface between insulation coordination and converter OVRT specifications

Section 7.3.8 outlines the OVRT requirements at the converter's DC-PoC. It specifies that the converter must remain connected during the OVRT (refer to OVRT profiles in **FIGURE 63**) while remaining connected and maintaining stable operation during the OVRT event. The OVRT profile is associated with overvoltage profiles that may occur within the system and could, therefore, be related to the insulation coordination of subsystems. It is important to note that insulation coordination concerns the equipment's dielectric strength, while OVRT concerns the converter stable operation during overvoltage events. A relevant question might be: what is the impact of the OVRT profile on insulation coordination, and vice versa? **FIGURE 84** presents potential options for selecting the transient overvoltage SA protection level in relation to the transient OVRT profile. In this example SA protective level can have two options:

- In option 1 the SA protective level is higher than the transient OVRT profile, which means that SA is not activated during transient overvoltages that could impact the stable operation of the converter. In practice, it means that the SA do not play a major role to ensure that the overvoltage transients are below the OVRT profile.
- In option 2 the SA is activated during the transient OVRT and therefore it plays a role to limit the transients. It could be argued that if the SA limits the transient overvoltage than it could be reasonable to set the SA protective level to the OVRT profile as shown in option 3.

Option 1 is the recommended choice. For transient overvoltage conditions, the SA should not interfere with the OVRT profile. The surge arrester role is to protect the system components by handling dielectric stress, while the OVRT profile ensures that the converter remains connected during these transient events. Each function addresses different aspects of system performance and protection, and they should operate independently of one another. It is worth noting that the surge arrester should not be designed to be active during the U_{OV1} overvoltage to limit unnecessary energy requirements/stresses on the arrester. However, if the U_{OV1} is high, the arrester can conduct and this must be taken into account on the design of the SA.

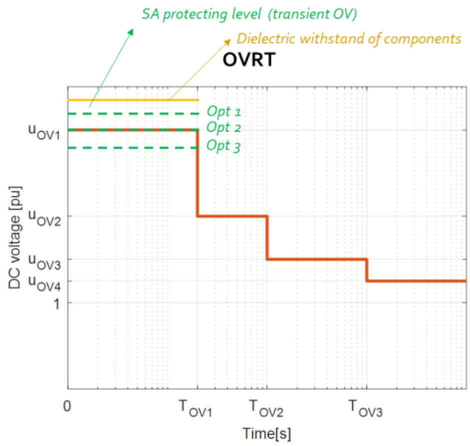

FIGURE 84: Example of possible options for the choice of the transient overvoltage SA protective level versus the transient OVRT profile.

SA protective level and placement

The choice of the SA placement will impact the system overvoltages as already mentioned above. Annex A of IEC 60071-11 shows a typical arrangement of SA within a bipolar converter station; however, there is currently no common consensus on the placement of SA within multi-terminal HVDC grids. Determining who will be responsible for the choice of SA protective level and placement within the grid and possibly within the subsystem is an important question that needs to be addressed. Inadequate choice of SA protective level and placement could lead to uneven SA energy absorption and damage the equipment (the impact of energy sharing between arresters throughout the system is due to slow front overvoltages). The number of surge arrester within the system (and within the subsystems) should be carefully evaluated and optimized, as the presence of each pole-to-ground surge arrester introduces an additional potential weak point (risk of insulation failure), i.e. having too many surge arresters could ultimately reduce the overall reliability of the system. On the other hand, IEC 60071-2 mentions that for lightning and fast front transients (usually not a consideration of cable and indoor systems) surge arresters offer a limited protection range, typically spanning from a few meters to several tens of meters, and they should be installed as close as possible to the equipment requiring protection. The key question related to SA protective level and placement could be formulate as well: if the vendor defines SA placement and protection levels based on standardized levels (withstand levels and minimum margins), can we be certain that there will be no issues with energy sharing among the SAs?

7.6.3 List of identified scenarios that can generates overvoltages

A mapping of the overvoltage scenarios that can appear in a multi terminal DC grid in bipolar configuration with DMR is shown in **TABLE 35**. Type of overvoltage are based on Table 1 of IEC-60071-11, see **FIGURE 78**.

TABLE 35: Proposal of mapping of overvoltage scenarios for poles and DMR. Where multiple types of overvoltage are indicated, detailed EMT simulations are needed to determine which type is actually seen for each event.

Event	Type of Overvoltage	Consequences / Comments
Continuous Operating DC Voltage Range - poles	Low frequency - Continuous	This is not really an overvoltage, but it is dimensioning for the pole to ground SA. Thermal stress should be lower than a certain threshold during normal operation.

Continuous Operating DC Voltage Range - neutral	Low frequency - Continuous	Stress on neutral to ground SA during normal operation
Pole to ground fault	Transient - Fast-front Transient - Slow-front Low frequency - Temporary	Pole to ground overvoltage, due to the opening of the DCCB. Pole to neutral overvoltage. Healthy pole to ground overvoltages, as consequence of possible neutral voltage shift, depending on the value of the grounding resistance.
Pole to DMR fault	Transient - Fast-front Transient - Slow-front Low frequency - Temporary	Pole to ground overvoltage. Pole to neutral overvoltage. Healthy pole to ground overvoltages Consequences are probably similar to pole to ground fault.
Pole to pole to ground fault	Transient - Fast-front Transient - Slow-front Low frequency - Temporary	Pole to neutral overvoltage. It is supposed that those type of fault will not produce overvoltages on the poles, but they could produce higher overvoltages on DMR because of the short circuit current contribution coming from both poles.
Opening of more than one DCCB during pole to ground fault	Transient - Slow-front	Pole to ground overvoltage. In this situation two DCCBs are opening at the same time, due for example to a sympathetic trip.
Harmonic overvoltage	Low frequency - Temporary	Pole to ground overvoltage
DCCB opening - load current	Transient - Slow-front	Pole to ground overvoltage. Situation in which the DCCB is activated to open a load current and the total TIV (e.g. 1.5 pu) is imposed.
Single phase to ground fault (AC valve side transformer)	Transient - Slow-front Low frequency - Temporary	Pole to ground overvoltage. Pole to neutral overvoltage. Neutral to ground voltage.
Loss of load	Low frequency - Temporary Transient - Slow-front	Pole to ground overvoltage. Pole to neutral overvoltage.
Converter blocking	Low frequency - Temporary	Pole to ground overvoltage. Pole to neutral overvoltage.
Operation after contingency	Low frequency - Temporary	Pole to ground overvoltage. Pole to neutral overvoltage.
Lightning	Transient - Fast-front	Pole to ground overvoltage. Pole to neutral overvoltage. Neutral overvoltage. Not applicable for 100% based cable system. Investigation of LI overvoltages and related insulation coordination requires different models and methodologies.

The mapping is intended to be a first proposal and could be used as input for the insulation coordination methodology, see **FIGURE 85**.

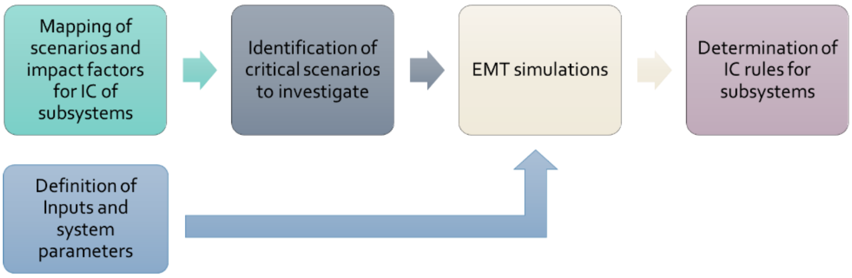

FIGURE 85: Methodology applicable for the determination of insulation coordination rules for the subsystems.

7.6.4 Conclusions

A review of the state of the art of insulation coordination for HVDC systems has revealed that while standards and literature exist for point-to-point HVDC systems, there remains a significant gap in the development of rules and procedures for insulation coordination in multi-terminal DC grids. The methodology for insulation coordination can be based on the procedure outlined in IEC 60071-11; however, further analysis is required to validate its applicability to HVDC grids that include DC circuit breakers. Specifically, the following critical issues must be addressed: the determination of switching and lightning impulse withstand voltages for HVDC equipment, and the assigning of responsibility for defining surge arrester protection levels and their optimal placement. This is even more challenging in a multi-vendor context. is important to note that even if a new series of standards for HVDC systems has been initiated, a standard for HVDC switching station is not foreseen. As a next step, it is proposed to undertake a thorough identification of all potential transient overvoltage scenarios that may arise within a DC grid.

7.7 DC system grounding

Basics of neutral system grounding for HVDC grid based on bipolar with metallic return architecture have been reported in section 6.6 of [33] and main conclusions are reported hereunder.

- The grounding of neutral shall provide a reference voltage for the neutral of the stations.
- Typically, only one station has the neutral grounding solidly (or through a grounding resistor Rg or impedance Zg) connected to earth. This grounding connection should be realised within a switching station to be independent on the availability of connected converter stations. Only when disconnected from the DC grid (STATCOM), a converter station may utilize a reference to ground of its own.
- Temporarily, multiple solid grounding points can be tolerated, after a fault or during a reconfiguration two stations can have the neutral grounding solidly connected to earth. For example, the load current can flow through the ground for few seconds.
- Typically, the steady state current through the ground should not exceed few Amps.
- The solidly grounded station can have a grounding resistance, for example of 10-20-50-100 ohm to avoid the problem of non-zero current crossing at the AC side grid during a SPG fault at valve side.

- All switching stations need to have the neutral point grounded through a SA to limit overvoltages in case of faults. SA installed in converter stations should be coordinated with the DCSS SA such, that they do not impact the rating of the DCSS SAs. The neutral surge arrester shall be designed to ensure limited steady state current through the earth during unbalance operation and to limit overvoltages during faults.
- To allow redundancy, all stations can switch from solidly grounded neutral to a neutral point grounded through a SA and viceversa.

7.7.1 Impact of grounding resistance during pole to ground fault

In the event of a pole-to-ground fault, the grounding resistance has a significant influence on the fault current as well as the resulting voltage shifts and overvoltages. In this section the focus will be on the overvoltages and shall be illustrated usinig the exemplary DC grid shown in **FIGURE 86**.

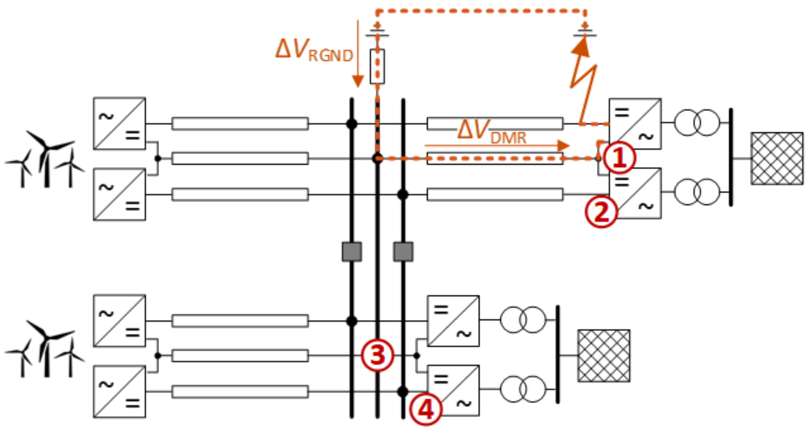

FIGURE 86: Example Grid with pole to ground fault and grounding via resistor in central DC Switching station. The fault circuit via ground and the grounding resistor is shown in orange.

The DC grid is grounded via a grounding resistor in the central DC switching station and by surge arresters in every converter station. A pole-to-ground fault is considered at the positive pole of a remote onshore converter connect via 300 km of cable. The value of the grounding resistance will be varied to exemplarily show the influence on overvoltages at the points (1) – (4).

For pole-to-ground-faults, the fault circuit closes through the ground via the grounding resistor, resulting in a voltage drop ΔV_{RGND} across the grounding resistor and ΔV_{DMR} along the DMR cable route. These voltage drops can influence the voltages in the whole system which will be shown exemplarily for points (1)-(4). These points focus solely on the converter and the switching station; however, voltages along the cables may be higher due to the superposition of traveling waves.

For point (1), the neutral bus of the onshore converter, the potential will jump initially as the positive converter pole is pulled to ground potential and the converter is still injecting its full voltage. The voltage at point (1) would then be determined by the voltage drops across the grounding resistor and DMR cable as long the fault is not cleared by DC and AC circuit breakers after ~100 ms if no arrestors were present in the neutral. However, in the exemplary DC grid the converter neutrals are grounded via surge arresters, designed to limit the voltage to 100 kV. The voltage at point (1) is shown in **FIGURE 87** a) for different values of the grounding resistor.

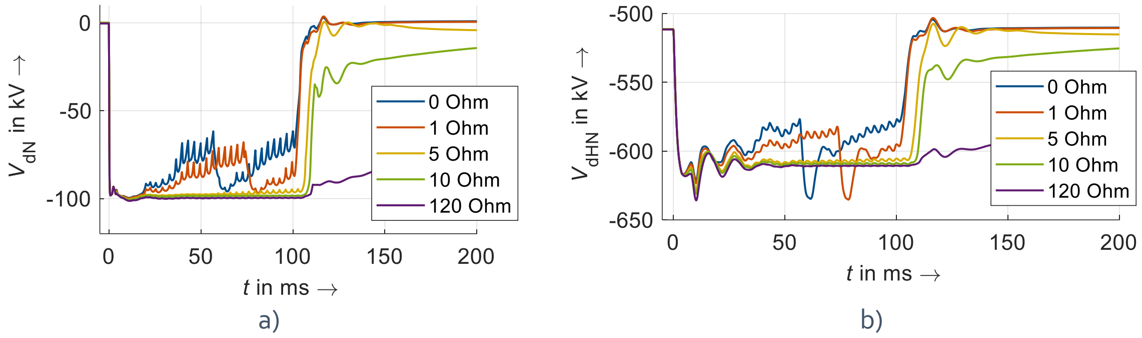

FIGURE 87: Effect of the grounding resistor on overvoltages at the converter station during a pole-to ground-fault
a) Neutral-to-ground voltage at point (1) in **FIGURE 86**
b) Pole-to-ground voltage in the healthy negative pole (point (2) in **FIGURE 86**)

It can be seen that the arrester responds in all cases and limits the voltage to -100 kV. The arrester remains active until fault clearing for all cases but very small values of the grounding resistor (0 Ω and 1 Ω). While the overvoltage is the same for higher values of the grounding resistor, the value grounding resistor greatly influences the energy absorption capacity of the neutral arresters at point (1).

The pole-to-ground fault in the positive pole also effects the voltage in the healthy negative pole due to the voltage shift in the neutral bus. This leads to overvoltages as shown in **FIGURE 87** b). The overvoltages are mostly limited by the neutral arresters. Thus, the maximum overvoltage is roughly the same for all values of the grounding resistor.

Overvoltages occur not only in the faulty bipole but also in the healthy parts of the DC system as all use the same grounding point in the central DC switching station. Thus, the voltage rise ΔV_{RGND} across the grounding resistor is manifested in the DMR throughout the entire system. This voltage rise depends on the size of the grounding resistor as depicted in **FIGURE 88** a). Only for solid grounding (0 Ω if resistance of grounding system is neglected) no voltage shift occurs.

The voltage shift in the DMR also affects the pole-voltages and leads to overvoltages in the negative pole as show in **FIGURE 88** b).

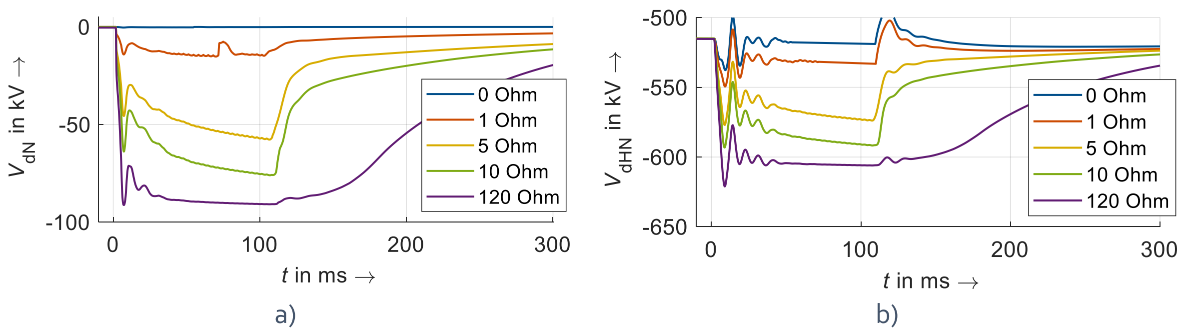

FIGURE 88: Effect of the grounding resistor on overvoltages in the healthy parts of the DC grid during a pole-to ground-fault
a) Neutral-to-ground voltage in the central DC switching station (point (3) in **FIGURE 86**)
b) Pole-to-ground voltage in the negative pole (point (4) in **FIGURE 86**)

The effects seen in this exemplary DC grid can be summarised as follows:

- During a pole-to-ground-fault a voltage shift occurs in the neutral pole at the affected converter station due do voltage rises over the grounding resistance and DMR cable. The voltage shift is limited by the neutral arrester and thus the same for all values of the grounding resistance.
- The voltage in the healthy negative pole is shifted accordingly leading to an overvoltage
- The voltages in the healthy parts of the DC network are also affected. The voltage shift and overvoltages are directly influenced by the value of the grounding resistor

7.7.2 Summary selection of grounding system

As shown in the previous sections, several effects must be considered when selecting a value for the grounding resistance, as shown in **FIGURE 89**.

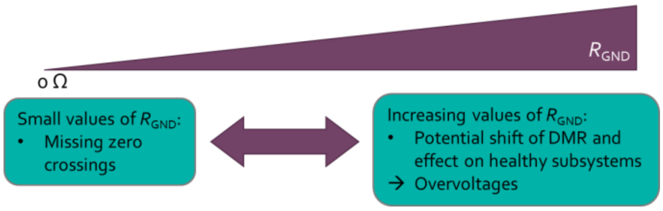

FIGURE 89: Trade-off when selecting a value for the grounding resistance R_{GND}

For solid grounding and small grounding resistances, missing zero crossings occur in the AC circuit-breaker in the event of SPG fault at valve side or converter internal faults. This can be avoided with higher grounding resistances, but for these resistances higher overvoltages occur in the DC system in the event of pole-to-ground faults. Especially the impact on the voltage in the healthy parts of the DC grid increases with increasing grounding resistance.

The possible range of the grounding resistance for all topologies must be made known to the subsystem designer. This can also happen by the specification of neutral voltage and current ranges and requirements on the allowable ranges for grounding resistances in the subsystem.

7.8 DC grid protection Functional Requirements of Subsystems & Parameter Lists

TABLE 36 provides a comprehensive summary of the functional requirements and associated parameters related to DC grid protection that subsystems must comply with.

TABLE 36 Functional requirements for DC grid protection

Functional requirement	Short description	Associated parameters	Subsystem
DC-FRT connection requirement	The AC/DC converter station shall stay connected during DC fault separation according to DC-LVRT profile	**FIGURE 54** **TABLE 30** **FIGURE 64**	AC/DC converter station
DC-FRT operational requirement	The converter shall continue stable operation after the power system has recovered following fault separation.	**FIGURE 54** **TABLE 30**	AC/DC converter station
DC-OVRT requirement	The AC/DC converter station the converter station shall stay connected during overvoltage events defined by the DC-OVRT profile	**FIGURE 63** **TABLE 32**	AC/DC converter station
Fault separation HV & neutral	The switching units at the boundaries of HV FSZs shall be equipped with an FSD which is capable of interrupting DC fault current related to all ordinary contingencies within a maximum fault neutralization time $T_{N,max}$.	$T_{N,max}$	Switching unit
Fault separation AC/DC converter station	AC/DC converter stations at the boundary of a FSZ shall ensure fault separation by its own means or by activation of the adjacent ACCB.		AC/DC converter station
Fault isolation HV & neutral	The switching units at the boundaries of an FIZs shall be able to isolate all ordinary contingencies within a maximum fault isolation time.	Residual current interruption level, Fault isolation time	Switching unit
Fault current withstand requirement	Subsystems shall withstand fault currents in terms of amplitude and duration while primary or backup protection is operating.	Overcurrent amplitude, overcurrent duration	AC/DC converter station, DCSS
Fault discrimination FSZ – primary	Each subsystem at the border of a FSZ shall ensure fault discrimination for fault separation based on local measurements without telecommunication, ZDDs shall be designed accordingly. The relay time shall be coordinated with the internal commutation time of the related FSD to comply with the maximum fault neutralization time for main protection.	$T_{N,max}$ (T_{relay}, T_{op})	Switching station / switching unit, AC/DC converter station

Fault discrimination FSZ – backup	Each subsystem at the border of a FSZ shall ensure fault discrimination for fault separation which shall be based on local measurements if technically feasible. The relay time shall be coordinated with the internal commutation time of the related FSD to comply with the maximum fault neutralization time for backup protection.	$T_{N,max}$ (T_{relay}, T_{op})	Switching station / switching unit
Fault discrimination FIZ	Fault discrimination for fault isolation shall be ensured telecommunication.	$T_{N,max}$ (T_{relay}, T_{op})	Switching station / switching unit
Fault discrimination neutral path	Fault discrimination on the DMR pole shall be ensured within the specified time.		Switching station / switching unit
Tele-communication	In case of unit-based fault discrimination, a telecommunication interface with remote-end subsystems shall be provided. Signals and communication protocol shall be coordinated.		Switching station / switching unit
Protective auto-reclosing	In case the switching unit is required to have the ability to re-energize the healthy part of the FSZ, the number of OCO sequences N_{OCO} and associated maximum reclosing time shall be respected in case of a persistent fault. The energy absorption rating shall be designed accordingly.	N_{OCO}, T_C	switching unit
Coordinated reclosing	Communication interfaces for coordinated reclosing of several subsystems shall be provided. Switching units shall be able to receive reclosing commands.		Switching station / switching unit
Monitoring	States related to protection sequences shall be reported to the DCGC	converter station: Blocked state, ACCB activation DCSS: FSD activation / deactivation	Switching station AC/DC converter station

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9. Appendix

9.1 Functional Requirements at AC connection point

The functional requirements that the HVDC system and each of AC/DC converter station or unit within the system must satisfy are comprehensively stipulated in [4]. The following provides a concise summary of these requirements, with references indicated.

- Active Power Controllability (Article 13): The AC/DC converter shall be capable of regulating the active power up to the value in the active power control range in compliance with the performance requirements specified by the relevant TSO.
- Ramping Rate of Active Power Change (Article 13): The AC/DC converter station shall be capable of adjusting the ramping rate of active power variations within their technical capabilities according to the instructions sent by the relevant TSO.
- Frequency Sensitive Mode (FSM) (Article 15): The HVDC system shall be capable of responding to frequency deviations in each connected AC network by adjusting the active power transmission in accordance with the parameters specified by each TSO within the ranges specified.
- Limited Frequency Sensitive Mode – Overfrequency (LFSM-O): In addition to the requirements specified for FSM, when operating in LFMSM-U, the HVDC terminal shall be capable of adjusting active power frequency response to the AC network or networks according to the parameters specified for LFSM-U by the relevant TSO.
- Limited Frequency Sensitive Mode – Underfrequency (LFSM-U): In addition to the requirements specified for FSM, when operating in LFMSM-U, the HVDC terminal shall be capable of adjusting active power frequency response to the AC network or networks according to the parameters specified for LFSM-O by the relevant TSO.
- Short Circuit Contribution during AC Faults (Article 19): If specified by the relevant system operator, the AC/DC converter shall have the capability to provide fast fault current at the AC side connection point in case of symmetrical faults in accordance with the specified requirements.
- Reactive Power Control Mode (Article 22): The AC/DC converter station shall be equipped with different reactive power control modes, as specified by the relevant system operator in coordination with the relevant TSO.
- AC Voltage Droop Control Mode (Article 22): When operating in the AC voltage droop control mode, the AC/DC converter station shall be capable of contributing to voltage control according to the parameters specified by the relevant TSO.
- Dynamic AC voltage control (VDE-AR-N Section 10.1.9): In case of large AC voltage deviation, the AC/DC converter station must be capable of contributing to voltage control by rapidly injecting reactive power, as specified by the relevant system operator in coordination with the relevant TSO.
- Frequency Control (Article 16): If specified by the relevant TSO, the AC/DC converter shall be equipped with an independent control mode to modulate the active power output depending on the frequencies in order to maintain stable system frequencies.

- Priority to Active or Reactive Power Contribution (Article 23): The AC/DC converter station or unit shall be equipped with a control function logic to prioritize either active or reactive power contribution during low or high voltage operation and during faults for which fault-ride-through capability is required. If priority is given to active power contribution, its provision must be established within a time from the fault inception as specified by relevant onshore TSO.
- Post fault active power recovery (Article 26): The AC/DC converter station shall be capable of restoring active power after a fault in AC network in compliance with the allowed time and levels of AC voltage and active power recovery specified by relevant TSO(s).
- AC Fault Ride Through Capability (Article 25): The AC/DC converter station or unit shall remain connected and continue stable operation when its connection point voltage stays within the specified voltage-time series profile.
- Priority Ranking of Protection and Control (Article 35): The control scheme of protections and control devices consisting of different control modes, including settings of the specific parameters, shall be organized in compliance with the following priority ranking, listed in decreasing order of importance:
  - Connected AC network system and HVDC system protection; (interpreted as this includes DC voltage droop mode)
  - active power control for emergency assistance;
  - synthetic inertia, if applicable;
  - automatic remedial actions, including blocking FSM, LFSM-O, LFSM-U
  - LFSM;
  - FSM and frequency control; and
  - power gradient constraint
- Power Oscillation Damping Capability (Article 30): The HVDC system shall be capable of contributing to the damping of power oscillations in connected AC networks. The control system of the HVDC system shall not reduce the damping of power oscillations.

9.2 Examples of Multi-Segment Droop Characteristics with Varying Power Setpoints

The following illustrates several multi-segment droop characteristics based on the functional specifications established in Section 6.5. Note that the selection of these parameters depends on the system and is subject to the discretion of the system operator. Thus, the values utilized in the following demonstration are only indicative.

First, the influence of the power set-point on the multi-segment droop characteristic is demonstrated. The following figures illustrate how variation in set-point, specifically [+1.0, +0.5, 0, -0.5, -1.0] p.u, affects the shape of the droop characteristic. All associated parameters, such as the voltage levels and droops, are summarized on top of each figure and remain consistent across all figures.

The power set-point plays a crucial role in determining the available headroom capacity in each direction. When the set-point is close to the maximum or minimum power limit, power voltage response along the specified droop may soon exceed the power transmission capability. As mentioned in the functional requirements for each mode, namely, DCVSM, LDCVSM, and DCVLM, the active power shall be constrained by the maximum and minimum active power transmission capacity. Consequently, the droop characteristics of those mode shall cease progression upon reaching these maximum and minimum power limits.

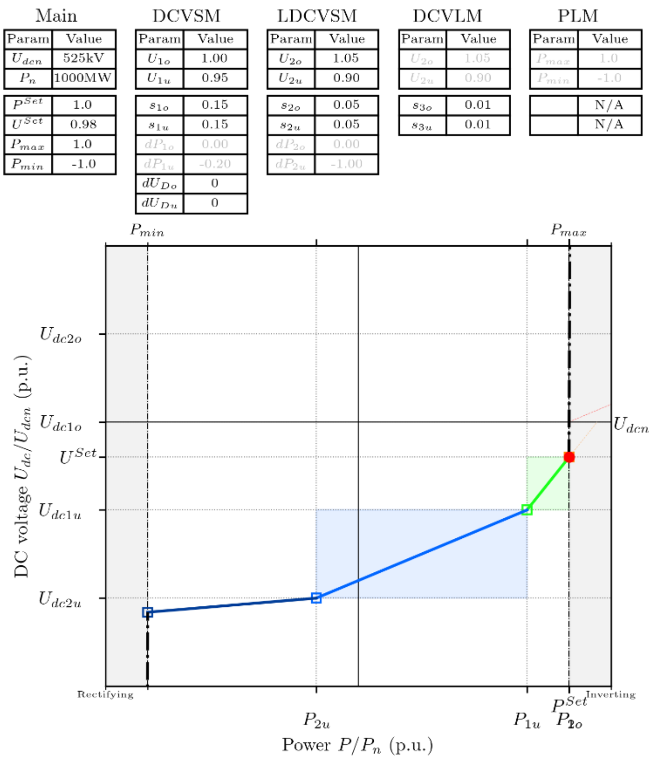


FIGURE 90: Multi-Segment Droop Characteristics Illustration with Setpoint [P^{Set}, U^{Set}] = [+1.0, 0.98].

An observation across the figures indicates that certain slopes associated with the droop characteristics of specific modes may not appear, depending on the power set-point. Each droop characteristic determines the power deviation associated with the respective section. Consequently, if these deviations accumulate to the extent that they reach the maximum or minimum power transmission capacity, no remaining capacity is available to accommodate certain modes.

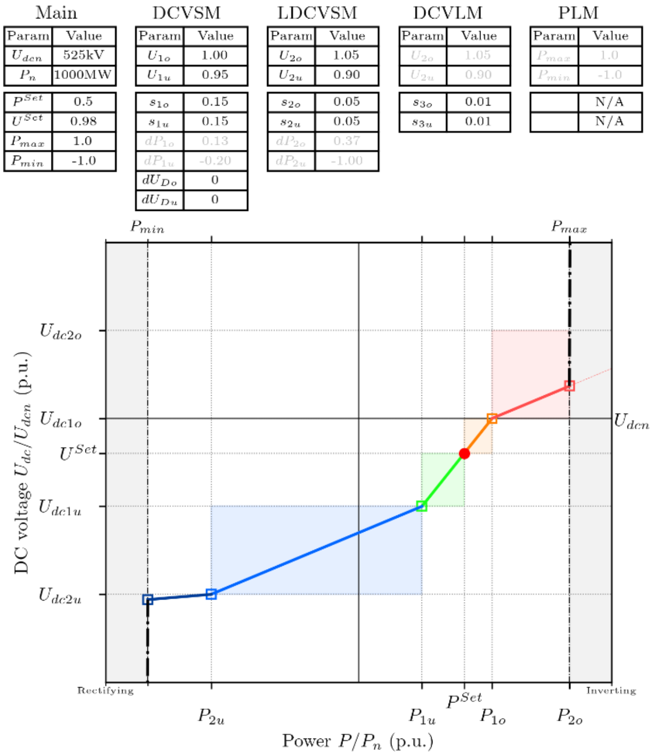


FIGURE 91: Multi-Segment Droop Characteristics Illustration with Setpoint [P^{Set}, U^{Set}] = [+0.5, 0.98].

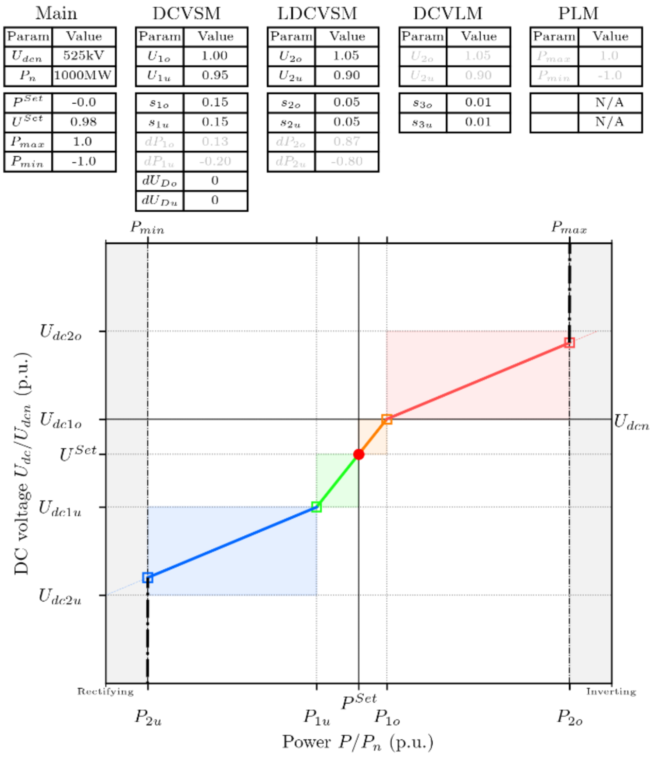


FIGURE 92: Multi-Segment Droop Characteristics Illustration with Setpoint [P^{Set}, U^{Set}] = [0.0, 0.98].

A noticeable difference can be observed between **FIGURE 92** and **FIGURE 93**. In **FIGURE 92**, the maximum transmission capacity is fully exploited before the multi-segment droop characteristic reaches the overvoltage level U_{dc2o}. However, in **FIGURE 93**, the full power capacity is not exhausted at U_{dc2o}, where power reaches P_{2o}. This suggests that in case where a large headroom capacity is available, depending on the selected droops, the full power capacity may not be fully utilized before reaching Udc2o.

Given that exploiting the full power capacity is not stipulated as mandate condition for LDCVSM-O and -U, a countermeasure is necessary to immediately utilize the available capacity once U_{dc2o} is exceeded. This is the role expected of DCVLM.

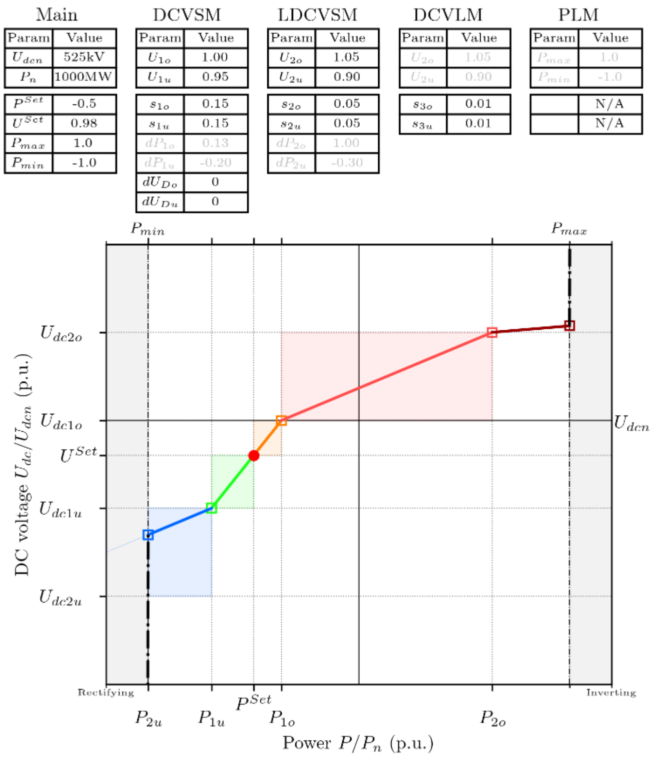


FIGURE 93: Multi-Segment Droop Characteristics Illustration with Setpoint $[P^{Set}, U^{Set}] = [-0.5, 0.98]$.

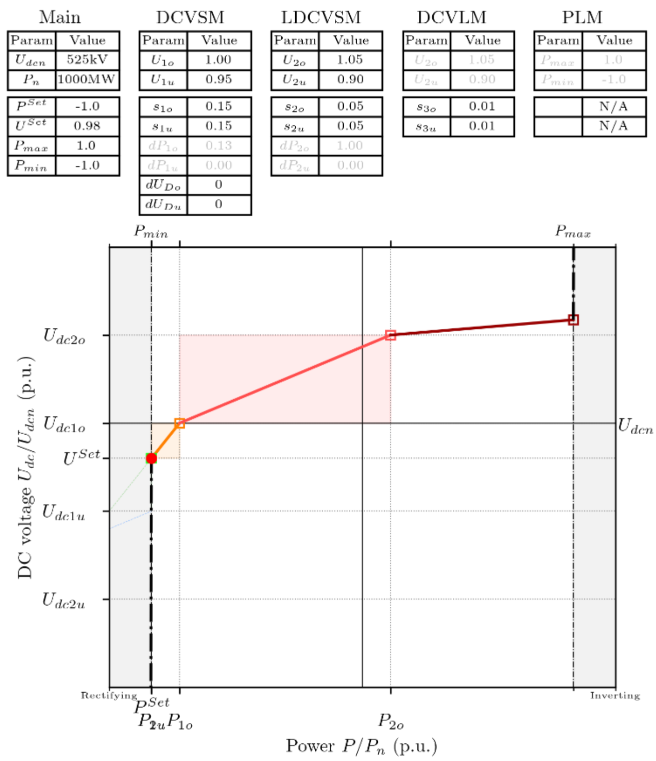


FIGURE 94: Multi-Segment Droop Characteristics Illustration with Setpoint $[P^{Set}, U^{Set}] = [-1.0, 0.98]$.

9.3 Alternative DCVLM definition

This section introduces an alternative definition of the DCVLM mode that was discussed within the Continuous Control Workstream of InterOPERA Task 2.1. This alternative definition was collectively acknowledged as a valid option.

The following provides a detailed description of this alternative definition and associated advantages.

FIGURE 34 and **TABLE 14** illustrate the DCVLM capability and parameter definitions under the alternative DCVLM definition.

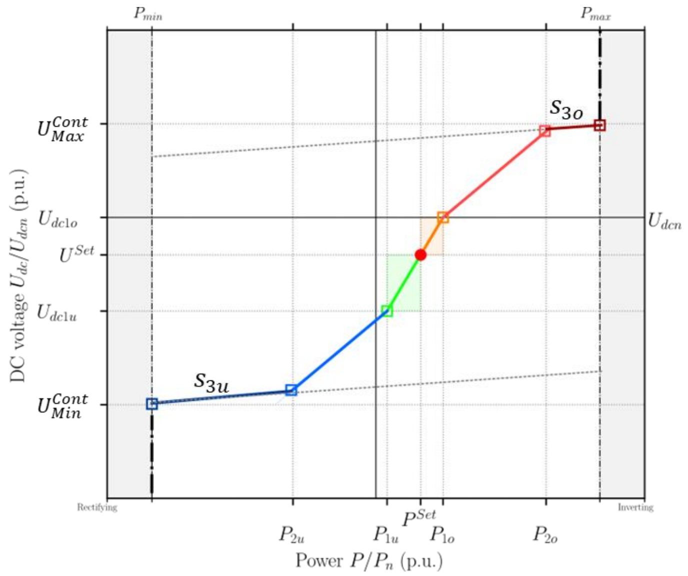


FIGURE 95: Droop capability of an AC/DC converter station or unit in alternative DCVLM definition.

TABLE 37: Parameters for active power voltage response in DCVLM.

Variables	Definitions	Unit
s_{3o}	droop at overvoltage	$\mathrm{p.u.}$
s_{3u}	droop at undervoltage	$\mathrm{p.u.}$
U^{Cont}_{max}	maximum continuous operating DC voltage	$\mathrm{p.u.}$
U^{Cont}_{min}	minimum continuous operating DC voltage	$\mathrm{p.u.}$

Activation of DC Voltage Limiting Mode

DC Voltage Limiting Droop Mode shall be activated when the voltage reaches the slopes positioned below U^{Cont}_{max} and above U^{Cont}_{min}, with these slopes characterized by the droops s_{3o} and s_{3u}.

In this alternative DCVLM definition, the trigger voltages are determined by the intersection points of the LDCVSM characteristics and the slopes defined for the DCVLM. This ensures that the converter's operational range remains confined within the voltage band defined by U^{Cont}_{max} and U^{Cont}_{min}. Consequently, the triggering conditions for DCVLM become functions of the converter's set-points and the droops assigned to other modes, such as DCVSM and LDCVSM.

Concerns in the Current DCVLM Definition

In the current formulation, the DCVLM is primarily viewed as a security backup, activated only when the defined voltage bands are exceeded due to unforeseen circumstances, and when the converter still has available headroom capacity. Although deviations beyond these bounds are expected to be marginal and can be limited to the upper threshold determined by the DCVLM droop[51], the actual exceeding voltage levels are not universally fixed and left undefined in the current framework.

It is important to note that U_{max}^{Cont} and U_{min}^{Cont} should not be interpreted as the voltage levels beyond which the converter ceases operation. Additional voltage withstand capability limits above and below these thresholds are necessary to account for certain contingency scenarios, such as DBS activation. However, the current formulation does not clearly stipulate the relation between the droop characteristic and the converter design constraints.

Advantages of the Alternative DCVLM Definition

This alternative DCVLM formulation provides several key advantages:

1. **Operational Boundaries Alignment**: By confining the operation within U_{max}^{Cont} and U_{min}^{Cont}, this formulation establishes a clear and direct link between the voltage bands and the converter's designed operational voltage range, within which the converter must be capable to operate with its full capacity.
2. **Efficient utilization of voltage capability:** This alternative formulation eliminates the need for additional voltage levels beyond U_{max}^{Cont} and U_{min}^{Cont}. This allows for full utilization of the converter's designed voltage capability of a converter, which may be under-utilized in the current formulation.

Implementation Considerations of the Alternative DCVLM Definition

Since the triggering conditions in this alternative formulation are not universally fixed and depend on the set-point, which may vary during operation, the following additional considerations may be required:

- **From the TSO Perspective**: The TSO must take into account the more complex DCVLM activation logic in performing contingency analyses and determining the droop parameters.
- **From the Vendor Perspective**: Vendors must implement the activation logic within the controller to adapt to the varying nature of the triggering conditions.

9.4 Implementation options of DC voltage droop controller and recommendations for droop selection

The stability of the system is determined by the dynamic response of each AC/DC converter and their interactions through the network. In a multi-vendor and multi-terminal DC grid, each converter controller would likely be unique to each vendor, reflecting different control design concepts. Moreover, the complexity of converter controller, especially those involving IP-sensitive solutions, challenges the application of conventional control design procedures in a single vendor system. Therefore, the established static requirements for the primary DC voltage control must be complemented by appropriate dynamic requirements such that the risk of interoperability issues in a multi-vendor HVDC systems can be minimized.

[51] E.g., with $s_{3o} = 0.5\%$, the theoretical maximum exceeding voltage is $s_{3o} * 2\mathrm{pu} = 1\%$.

In this section, the implementation of DC voltage droop controller, the crucial element that characterize the system dynamics is first discussed. Then, the principal determinant factors that shall be considered in selecting the droop are discussed.

9.4.1 DC Voltage Droop Controller Implementation

First, recall that the DC voltage droop is formally defined as the ratio between the steady-state DC voltage deviation to the steady-state change in the active power of the converter, which can be mathematically expressed by

$$k = \frac{\Delta U_{dc}}{\Delta P} = \frac{U_{dc} - U_{dc}^{Set}}{P - P^{Set}}.$$

However, the actual implementation of droop controller is subject to arbitrary manipulation because the governing equation is fully determined by the specified droop k, set-points U_{dc}^{Set} and P^{Set}, and local measurement, U_{dc} and P. This gives a rise to a flexibility in the derivation of different control laws from the same definition in the above equation.

In **FIGURE 96**, the proportional action by droop acts on the mismatch between the DC voltage setpoint and the measured DC voltage, modifying the active power reference which interfaces with the subordinate control layer. Assuming the power reference tracking capability of the AC power controller in steady state, the control law of this option can be expressed by:

$$P^{Ref} = \frac{1}{k}\left(U_{dc} - U_{dc}^{Set}\right) + P_{ac}^{Set} \Rightarrow P_{ac}$$

In **FIGURE 97**, on the other hand, the proportional action of droop acts on the mismatch between the active power setpoint and the measured value, modifying the DC voltage reference which is interfaced with the subordinate control layer. Assuming this time the DC voltage reference tracking capability in steady-state, the control law for this configuration can be given by

$$U_{dc}^{Ref} = k(P - P^{Set}) + U_{dc}^{Set} \Rightarrow U_{dc}$$

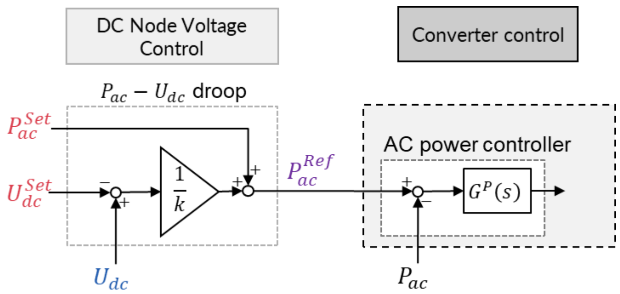


FIGURE 96: Droop implementation option 1.

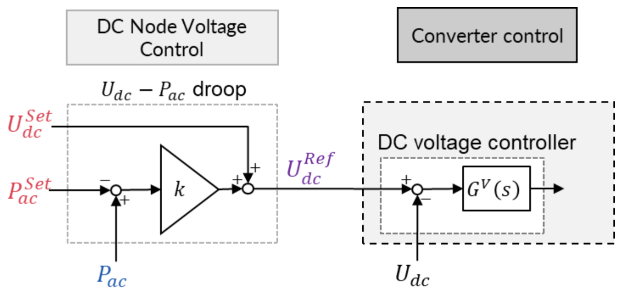


FIGURE 97: Droop implementation option 2.

The aforementioned examples theoretically demonstrate that two implementation options can both comply with the static behavioural requirement and will behave similarly in the static sense. However, the underlining difference of the cause-effect relation between the DC voltage and power could result in possible discrepancies when dynamic aspects are considered.

One such example is the implication of the droop gain as both a steady-state indicator and control parameter that impacts the dynamic response of the converter. **FIGURE 98** illustrates a use case of a three terminal DC system comprising the two DC voltage droop implementations described (Station 1 operating with option 1 and Station 2 operating with option 2), while Station 3 operates in constant power mode. The response, depicted in **FIGURE 99**, shows that the two implementations can co-exist in one DC grid in stable manner and that both lead to the same steady-state response (with the same droop gain for both stations, the two stations equally share the contribution to the primary DC voltage control). Nevertheless, due to the different implementation, the dynamic response of power for the two stations are different.

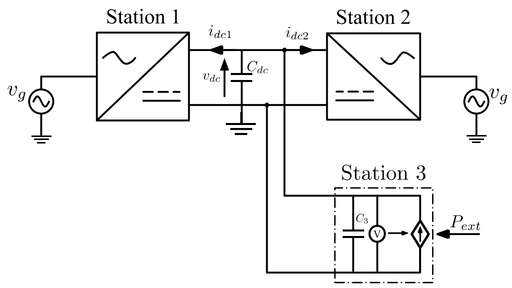


FIGURE 98: An exemplary three-terminal DC grid with Station 1 in Droop control option 1, Station 2 in Droop control option 2, and Station 3 in Constant active power control.

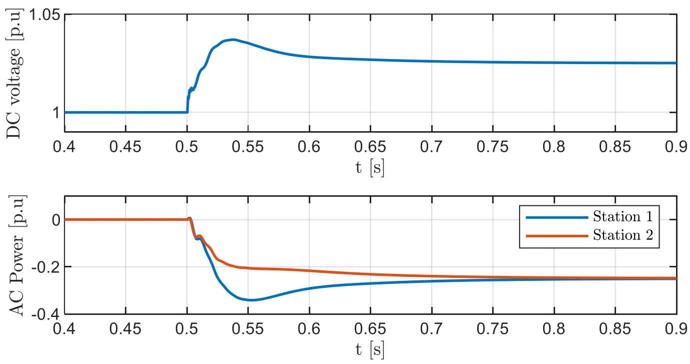


FIGURE 99: DC voltage (top) and AC power (bottom) response to a disturbance of a DC system comprising two droop implementation options.

In different scenarios, including additional analyses not detailed here, both options have demonstrated comparative performance. Despite the necessity for more in-depth exploration, particularly concerning different converter control schemes such as GFL and GFM, the evidence gathered thus far provided **no clear rational for excluding either and rather support retention of both options until and unless further analysis potentially reveals decisive factors.**

9.4.2 Determinant factors for system dynamics

Droop gain

From the above section, it was shown that the implication of the droop gain from a dynamic perspective is dependent on the respective controller implementation. This raises the question of the minimum and maximum feasible droop gain. In fact, referring to the control block diagrams in **FIGURE 96** and **FIGURE 97**, an extremely low value of droop gain for option 1 could lead to high gain instability as the active power reference becomes more sensitive to variations in the DC voltage. Similarly, a risk of high-gain instability for option 2 comes when a high droop gain is employed, since the DC voltage reference signal becomes more sensitive to variations in the active power, rendering the controller incompatible. An example of high gain instability for option 1 is shown in **FIGURE 101**, where a four terminal DC grid (shown in **FIGURE 100**) is simulated. In the MTDC grid, two stations operate in DC voltage droop mode and the other two stations operate in constant active power control. A disturbance from station 4 is introduced to the system at $t = 2s$. A droop gain of 0.002 pu is used in the station operating with droop control option 1 which renders the system unstable.

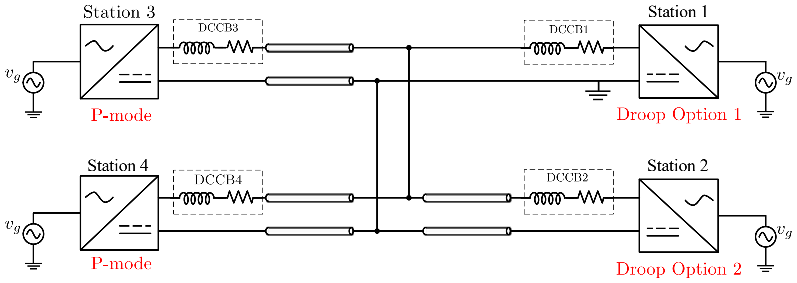


FIGURE 100: An example four terminal DC grid under study.

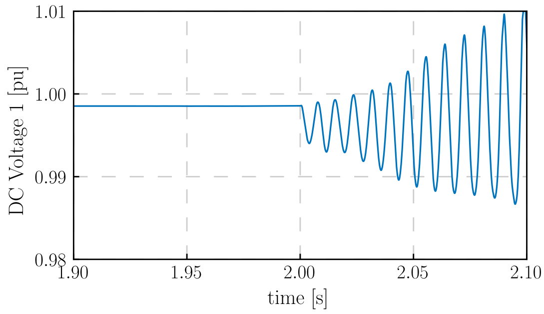


FIGURE 101: DC voltage response of a station operation with Droop option 1 at k_d = 0.002 pu.

DC reactor size

The sizing of DC reactors (DCRs) in a DC grid is commonly based on fault currents limiting considerations. However, the effect of DCRs on continuous control operation and the system response to disturbances needs to be further analysed. In **FIGURE 102** a comparison between the DC voltage response in the same DC grid depicted in **FIGURE 100** with respect to different DCR sizes is highlighted. It is clear that the DCR has a negative effect on the damping of the DC voltage. This impact should be considered in the design requirements of the DCR and the dynamic performance requirement for the primary DC voltage control.

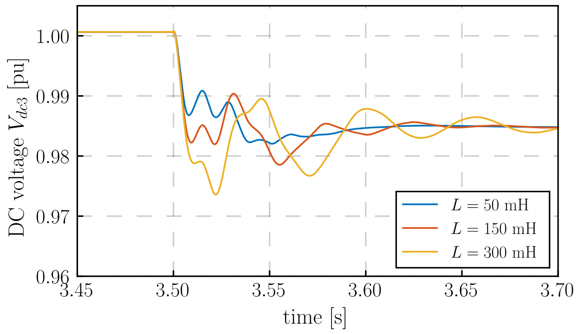


FIGURE 102: DC voltage response for different DCR values.

The negative effect of the DCR on the DC voltage damping is different for different power flow conditions. This is demonstrated in **FIGURE 103**, where two different initial power flow scenarios are compared with the same disturbance and the same system parameters. The difference between PF1 and PF2 lies in the direction of the power flow. In PF1, Fixed P control mode (P-mode) stations supply power to the DC grid, while DC voltage droop mode stations evacuate the injected power. This is inverted in PF2, where P-mode stations evacuate power from the DC grid.

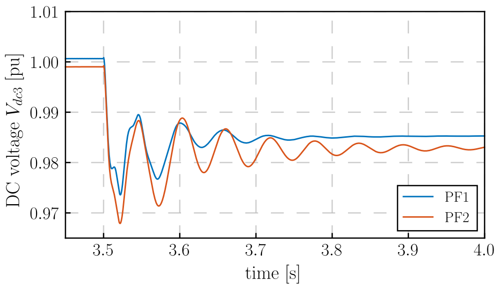


FIGURE 103: Effect of the initial power flow on the system response to disturbances. PF1: P-mode stations inject power to the DC system. PF2: P-mode stations evacuate power from the DC system.

From the above result, the negative effect of the DCR size on the damping of the DC voltage is augmented when P-mode stations operate in inverter mode. The so-called negative impedance instability of constant power loads is clearly visible. Different power flow scenarios should be included in the interaction studies of the system as well as in the compliance testing process to determine the worst case at which an MTDC could operate. If necessary, dedicated active damping controllers should be implemented.

Other determinant factors

As has been mentioned in this section, the dynamic response of the DC network is a function of both the physical elements of the grid and the active control provided by converter stations. The above two subsections demonstrated by simulation the implications of the droop gain and the DCR size on the grid's dynamic performance. However, other system constraints participate in shaping the dynamic response. These constraints include the AC grid strength alongside the internal controls of the respective converter stations.

9.4.3 Design space of droop

The previous section can be seen as an initial step in identifying the determinant factors that affect the system dynamic performance. A second step is to obtain a range of feasible control parameters that would satisfy both the static and dynamic requirements of the DC grid. **FIGURE 104** illustrates that, depending on how droop control is implemented, there is either a minimum or a maximum droop gain that ensures stability[52]. By considering conservative upper and lower limits for droop gains, both implementation options can coexist in the same DC grid, ensuring a satisfactory dynamic response.

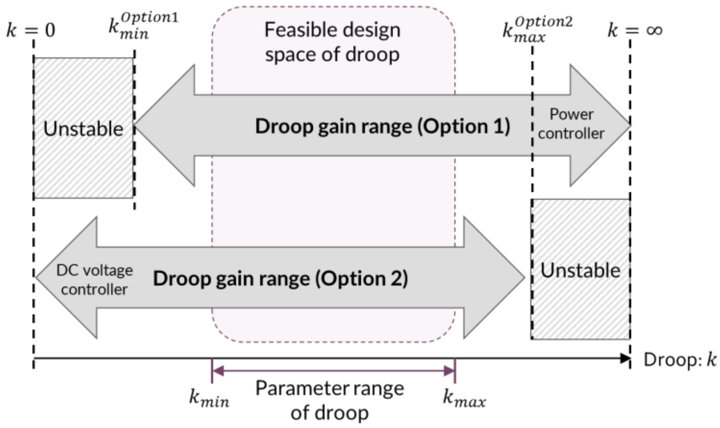


FIGURE 104: Example design space for droop gain based on the two droop implementation options.

9.5 Example for application and verification of dynamic performance requirements

This section outlines key considerations for the dynamic performance requirements specifications, with a particular focus on DC grid equivalent modelling. The effectiveness of the dynamic performance requirements specifications and the evaluation methodology described in Section 6.6.4 is verified through simulations conducted using the InterOPERA demonstrator grid model.

[52] In Option 1, an infinite droop gain means the system operates in a constant active power mode, while a droop gain of zero leads to high-gain instability, making Vdc-mode control unfeasible regardless of the droop gain value. Option 2, on the other hand, allows for Vdc-mode control with a zero-droop gain. A high droop gain in this case makes the system unstable, rendering the P-mode unfeasible.

9.5.1 DC grid stiffness at DC-PoC

The dominant DC voltage dynamics are typically observed in a relatively low frequency range (e.g. below 10 Hz[53]). This suggests that these dynamics are largely characterized by the interaction between the AC/DC converter stations and the grid in this frequency spectrum. The behavior of both the grid and the AC/DC converter stations in this range can be fully represented by their respective impedances. Therefore, to accurately evaluate the dynamic performance of a converter, it is crucial to first adequately model the grid to capture impedance within this frequency range.

FIGURE 105 depicts the sensitivity analysis results of the impedance scan of the InterOPERA demonstrator grid observed at the DC-PoC of CNVS2. For details on the InterOPERA demonstrator grid topology, please refer to D3.1 [17]. The design parameters include the uncertainty in the size of DCR located at each DCCB, with the range $[100, 150, 200]$ mH, and MMC inertia constant H_{mmc} in the range $[30, 40, 50]$ ms. While the DCR size is a design parameter dependent on vendor specific FSD characteristic, its range has been chosen to reflect the typical values outlined in Section 7.3.7. Similarly, the range of H_{MMC} has been selected based on a typical value of 40ms, accounting for variations around this value. The grid configurations vary from 3 to 5 terminals, where "a" represents a meshed grid configuration and "b" represents a radial grid configuration by removing line L1. The global behavior of the grid can be influenced by the control modes of other stations and their combinations. As an initial attempt, the worst-case operational scenario from a DC voltage regulation standpoint is assumed for this analysis, where no other stations operate in DC voltage droop mode; therefore, all other stations, both onshore and offshore stations, are set to fixed power mode. Justifications for this assumption is provided through an analysis of the frequency domain characteristics presented in **FIGURE 111**, as well as in the subsequent section, further supported by time domain simulations.

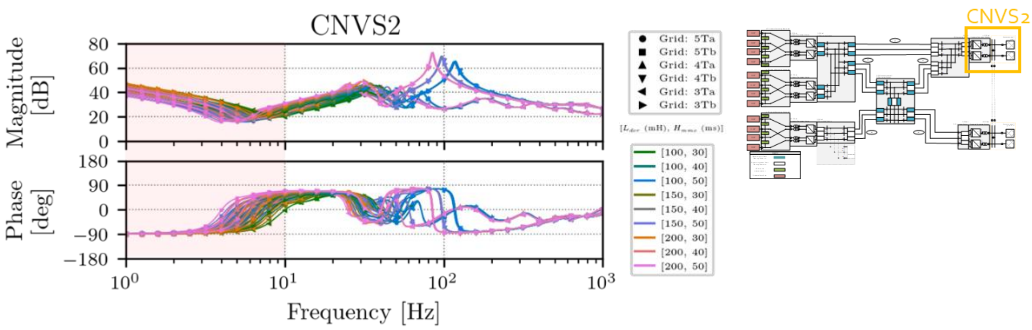


FIGURE 105 Sensitivity analysis results of the impedance scan of the InterOPERA demonstrator grid observed at the DC-PoC of CNVS2.

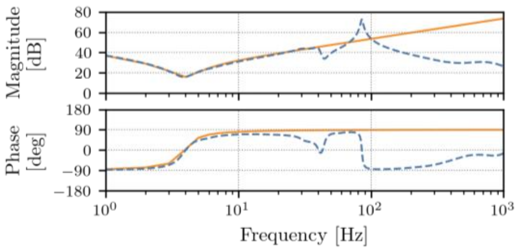
As observed, the impedance profile varies significantly depending on the grid configuration and the sensitivity parameters, making their generalization challenging. However, it can be noticed that in the low-frequency range (i.e. 1 to 10 Hz), the impedance profiles exhibit similar trends, with the primary difference being the location of the first resonance peak. This allows these characteristics to approximate into a simplified model, such as a simple RLC circuit.

[53] For a second-order approximate system with a damping ration of 0.7, the natural frequency can be approximated from the 95% control settling time T_{cs95} using the relation $\omega_n \approx 3/T_{cs95}$. For instance, in case of DC voltage control tuned to a 100ms settling time, the corresponding natural frequency f_n is approximately 4.8 Hz. For a more detailed description, please refer to .

Using a curve fitting technique [34] , the fitting results up to 10 Hz, for the two extreme cases, which exhibit the lowest and highest first resonance frequencies ($\left[f_{res1}^{Min}, f_{res1}^{Max}\right] = [3.96,\ 9.02]$ Hz), are summarized in **FIGURE 106**.

	Grid config.	Sensitivity params. L_{DCR} [mH]	Sensitivity params. H_{mmc} [ms]
Value	5Tb	200	50

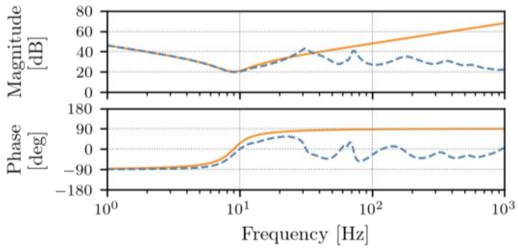
	R [Ω]	L [mH]	C [μF]
Value	6.3	755	2137



a) The case with the lowest first resonance frequency ($f_{res1}^{Min} = 3.96$ Hz)

	Grid config.	Sensitivity params. L_{DCR} [mH]	Sensitivity params. H_{mmc} [ms]
Value	3Ta	100	30

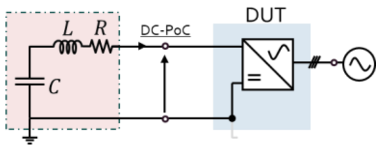
	R [Ω]	L [mH]	C [μF]
Value	10.1	401	777



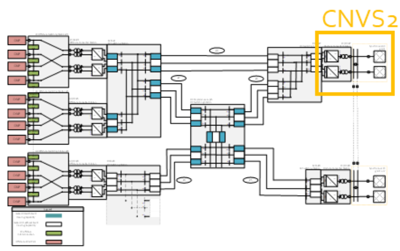
b) The case with the highest first resonance frequency ($f_{res1}^{Max} = 9.02$ Hz)

FIGURE 106 Curve fitting results to an RLC circuit, up to 10 Hz, for the two extreme cases exhibiting the lowest and highest first resonance frequencies.

Based on the derived fitting results, the step DC voltage reference responses of a simple set-up where the DUT interfaces with the RLC circuit, as shown in **FIGURE 107**.a are compared to those obtained from the detailed demonstrator grid simulations as shown in **FIGURE 107**.b. The subject station, CNVS2, is in DC voltage droop mode (implementation Option 2 as described in Section 9.4.1) with DCVSM droop of 0.05 p.u.. In alignment with the previous presumption of the worst-case operational scenario, the other stations are assumed to operate in fixed power mode. For the parameters of the demonstrator grid simulation, see Section 9.5.2.



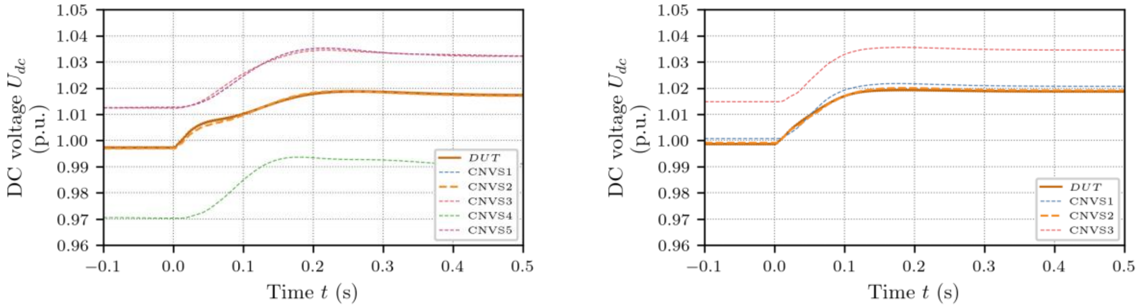
a) DUT interfacing with the RLC circuit



b) Detailed demonstrator grid

FIGURE 107 Simulation setups for the step DC voltage reference response comparison.

The comparison of the resulting DC voltages at the DC-PoCs are shown in **FIGURE 108**. For both extreme cases, the step response of the DC voltage at DC-PoC obtained with the detailed demonstrator grid is accurately replicated by the simple RLC circuit. It is also observed that the case fitted to f_{res1}^{Max} exhibits significantly slower dominant dynamics compared to the case with f_{res1}^{Min}. Therefore, these two extremes are referred to as representing "**the highest DC grid stiffness**" and "**the lowest DC grid stiffness**" from the perspective of the DC-PoC. It is important to note that this does not directly imply the inherent strengths of the DC system. The highest DC grid strength can be achieved when all converters participate in DC voltage control. Instead, the notion of grid stiffness should be understood as a characterization of the control effort required to maintain the system voltage.



a) The lowest first resonance frequency: "the highest DC grid stiffness"

b) The highest first resonance frequency: "the lowest DC grid stiffness"

FIGURE 108 Comparison of DC Voltages at DC-PoCs obtained with the DUT interfacing with the for both extreme cases.

To explore whether such a generalization is feasible, the RLC fitting results for all sensitivity parameter combinations across different grid configurations are summarized in **FIGURE 109**.

As shown, the two extreme cases representing the highest and lowest DC grid stiffness effectively encompass the range of parameter variations. Specifically, some configurations exhibit a higher inductance value, but have a lower capacitance value, resulting in an overall higher resonance frequency. Conversely, some feature lower inductance but higher capacitance. These combinations of inductance and capacitance contribute to the overall dynamic characteristic of the DC grid. Consequently, the selected extreme cases effectively encapsulate the full spectrum of possible DC grid characteristics within the frequency range under consideration.

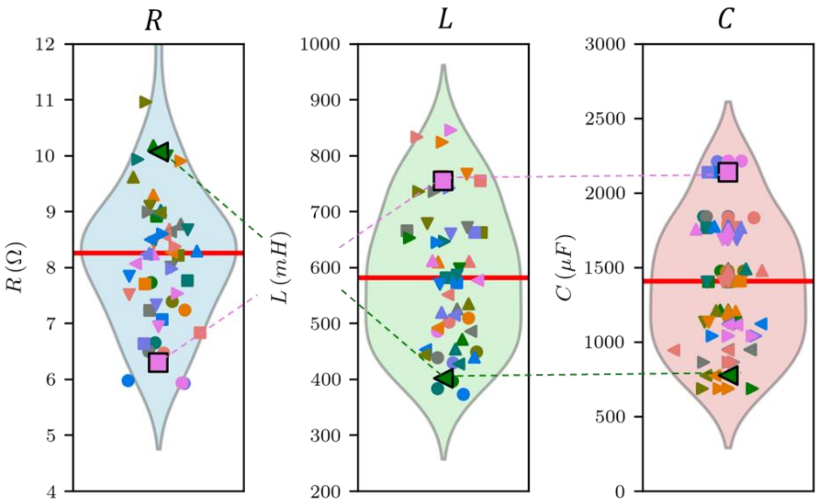


FIGURE 109 RLC fitting range; (pink: highest DC grid stiffness, green: lowest DC grid stiffness, red: median).

To generalize the proposed concept of DC grid stiffness, **FIGURE 110** shows the sensitivity analysis results of the impedance for the demonstrator grid seen at the DC-PoC of another onshore station, CNVS4. Although the impedance profiles differ noticeably from those observed at CNVS2, similar general trends are confirmed in the low-frequency range. This suggests the applicability of the proposed concept across different DC-PoCs. However, it also highlights the importance of considering the grid characteristic at each DC PoC, as a DC grid characteristic may considerably change depending on the topology of the grid as seen from the specific DC-PoC.

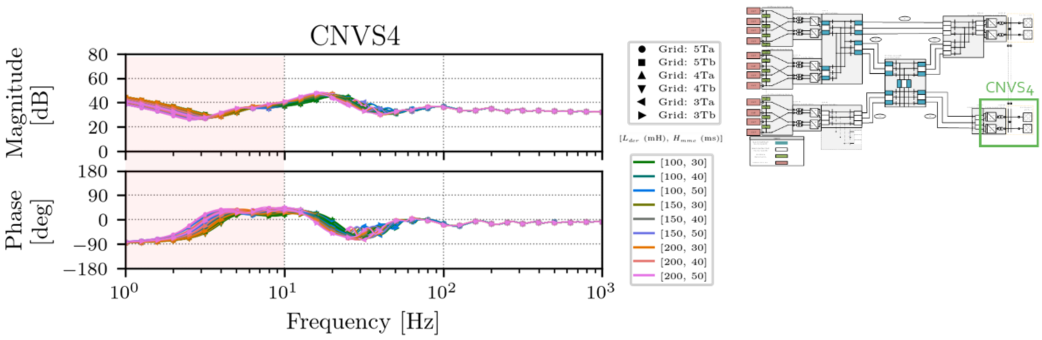


FIGURE 110 Sensitivity analysis results of the impedance scan of the InterOPERA demonstrator grid observed at the DC-PoC of CNVS4.

One important aspect that shall impact the grid impedance seen at the DC-PoC is the control mode of the adjacent converters. The following impedance scan demonstrates the impact of changing the control mode of CNVS4 in the InterOPERA demonstrator grid from fixed power mode to DC voltage droop mode. Z_{grid1} represents the grid impedance while CNVS4 is in fixed power mode. Z_{grid2} represents the grid impedance as CNVS4 is operating in DC voltage droop mode.

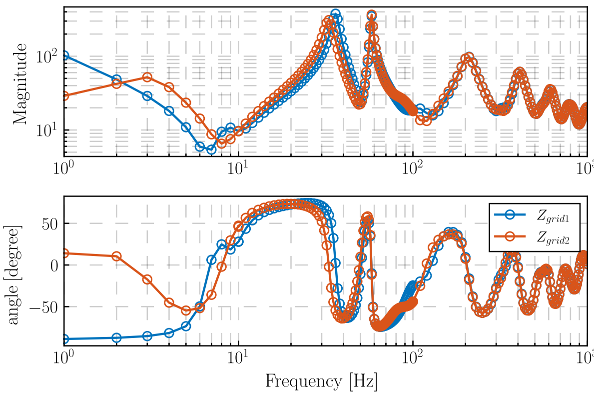


FIGURE 111: Impedance of InterOPERA five terminal grid seen at DC-PoC of CNVS2 for different control modes of CNVS4

As can be observed from **FIGURE 111**, CNVS4 operating in DC voltage droop mode, has a positive impact on the damping at low frequency range. While mid and high frequency ranges are not impacted by this change of control mode. This can be understood intuitively as the inclusion of droop controlling stations in the networks provides positive damping to the DC voltage compared to a grid consisting of only power controlling stations.

To summarize, the comparison of impedance profiles, considering parameters sensitivity and various grid configurations, has revealed that the DC grid exhibits a consistent trend in the low-frequency range. It predominantly characterizes the dominant DC voltage dynamics through the interaction between the converter and grid in this frequency range. It has been confirmed that, under the aforementioned assumptions, these trends can be effectively modelled using a simple RLC circuit.

The finding is particularly significant for the preliminary design of C&P system, as the dominant DC voltage dynamics can be replicated by such a simplified setup, which has been confirmed through the comparison with the detailed demonstrator grid simulations. Moreover, in the presence of high uncertainty in the design parameters of other sub-systems in the grid, the two extreme cases, representing the highest and lowest first resonance frequencies, have been shown to effectively encapsulate the full spectrum of possible DC grid characteristics. However, it is important to note that any simplification entails a loss of information. Therefore, to ensure the overall system stability, holistic stability assessment using accurate impedance profiles of all subsystems will be needed, as discussed in Section 9.6. It should be understood that the simplified DC equivalent should serve as input to the preliminary C&P design process.

While a complete analogy is not feasible due to their inherent differences, certain parallels with AC systems can still be drawn. In AC systems, the grid characteristics seen from an AC-PoC are typically quantified by parameters such as the maximum and minimum SCR or X/R ratios, which provides a quantitative measure of the grid strength at the AC-PoC. Similarly, in the context of DC grids, the two chosen RLC combinations can be regarded as effective quantitative measures of the DC grid characteristic at the DC-PoC. These measures offer a useful metric for evaluating dynamic performance requirements during preliminary C&P system design while accounting for the system uncertainties.

9.5.2 Validation of the standalone dynamic performance evaluations through system level simulations

This section provides a comprehensive evaluation and validation of the effectiveness, applicability, and necessary considerations of the dynamic performance requirement specifications and evaluation methodology described in Section 6.6.4. The simulations are conducted utilizing the InterOPERA demonstrator grid model, as detailed in D3.1 [17]. Emphasis is placed on assessing the effectiveness of evaluating standalone converter dynamic performance, based on the metrics defined in Section 6.6.4, in the context of grid operation where different converter stations operate simultaneously. In particular, the disturbance rejection capability, as assessed through the step power disturbance response test, is identified as a critical aspect and is therefore compared with results obtained from detailed simulations.

Simulation assumptions

The simulation assumptions are summarized in **TABLE 38**. All MMCs are modelled using Type 3 AAM model. Among various MMC control scheme available in the literature, the so-called Non-Energy-Based control scheme is adopted. Onshore converter stations operate in either DC voltage droop control mode or fixed active power mode. In the case of DC voltage droop control, a single droop section with a DCVSM droop of 0.05 p.u. is employed.

The considered event scenario is the blocking of the positive pole unit at the offshore station CNVS3 at $t = 1\ s$, leading to a sudden loss of 1GW of power injection to the DC grid.

TABLE 38: Summary of simulation assumptions.

MMC parameters	Values
MMC model	Type 3 AAM model
Rated power	1080 MVA
AC primary voltage	400 kV
AC secondary voltage	280 kV
Nominal DC voltage	500 kV
Control parameters	**Values**
MMC energy control	Non-Energy-Based control scheme
Current control response time	10 ms
DCVSM Droop constant	0.05 p.u

The same sensitivity parameters in Section 9.5.1 are considered. These include the size of DCR within the range of $[100, 150, 200]$ mH, and the MMC inertia constant H_{mmc} in the range $[30, 40, 50]$ ms. The grid configurations are varied from 3 to 5 terminals, considering both meshed ("a") and radial ("b") configurations.

KPIs

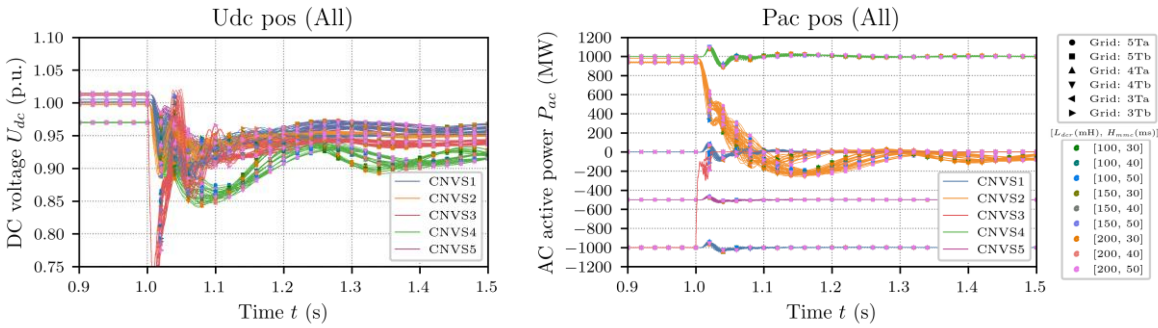
The simulations results are evaluated based on the following specific KPIs:

- Control settling time
- Power settling time
- Healthy stations' power deviation
- TOV at unhealthy station

Simulation results

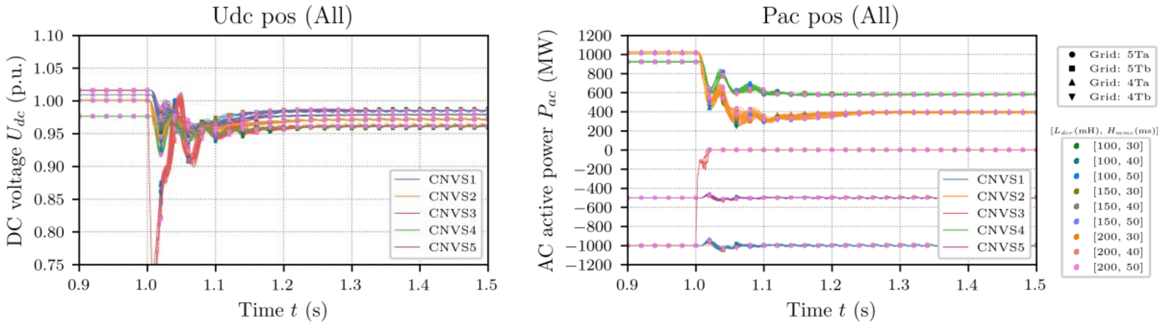
FIGURE 112 and **FIGURE 113** present the obtained results, showing the DC voltage at each DC-PoC and the active power at AC-PoC of positive pole in response to the blocking of the positive pole unit at offshore station CNVS3. **FIGURE 112** shows the results with a single droop station (CNVS2), while **FIGURE 113** shows the results when both onshore stations, CNVS2 and CNVS4, are in DC voltage droop modes.

It is observed that two cases exhibit noticeably different behavior. It is well known that the number of droop stations directly impacts the static characteristics of the DC system. In addition, it also affects the dynamic characteristic of the whole system. Typically, in the low-frequency range, an increase in the number of droop stations enhances damping characteristic, resulting in shorter settling times and reduced overshoot, in general. In order to assess the worst-case scenario from the operational standpoint, the following analysis focuses on the case where only one station is in DC voltage droop mode operation.



a) DC voltages (positive) at DC-PoCs b) AC power (positive) at AC-PoCs

FIGURE 112 Simulation results showing the DC voltages at DC-PoCs (positive pole) and AC power at AC-PoCs (positive unit) in response to the blocking of the positive pole unit at offshore station CNVS3. Only CNVS2 in DC voltage droop mode.



a) DC voltages (positive) at DC-PoCs b) AC power (positive) at AC-PoCs

FIGURE 113 Simulation results showing the DC voltages at DC-PoCs (positive pole) and AC power at AC-PoCs (positive unit) in response to the blocking of the positive pole unit at offshore station CNVS3. CNVS2 and CNVS4 in DC voltage droop mode.

In **FIGURE 114**, the voltages at DC-PoC of the subject station CNVS2 for all combinations of sensitivity parameters and grid configurations are shown. Additionally, the voltage responses obtained from the step power disturbance response test for the highest and lowest DC grid stiffness cases, detailed in Section 6.6.4.3, are also shown for comparison.

As observed, the standalone test behaviors effectively capture the low-frequency range dynamics observed in the detailed demonstrator grid simulations. However, in certain specific scenarios, oscillations in the 30-40 Hz range appear. These oscillations are understandably outside of the frequency range that the simple RLC circuit can capture and, therefore, are not fully represented. The high undershoots observed immediately after the event are caused by non-linear converter blocking and shall be disregarded.

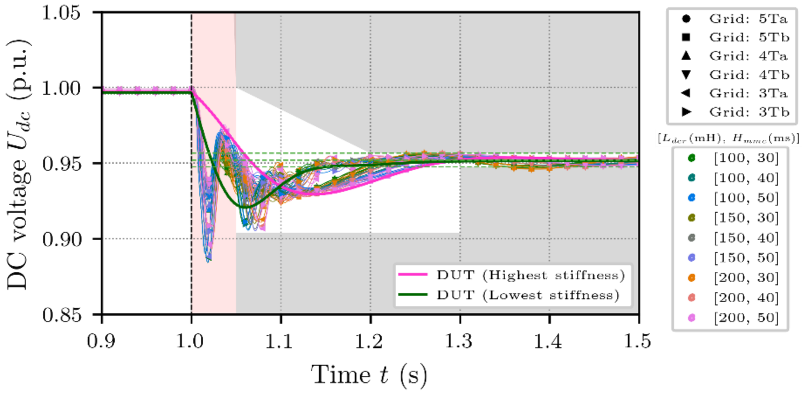
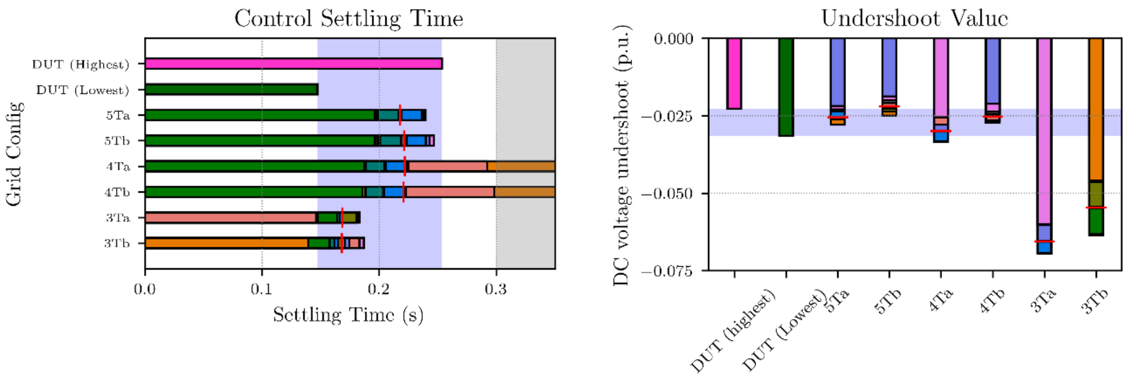


FIGURE 114 Simulation results showing the DC voltages at DC-PoC of CNVS2, compared with the step power disturbance response test results of the DUT for both the highest and lowest DC grid stiffness.

FIGURE 115 presents a summary of the KPI evaluation for DC voltages at DC-PoC of CNVS2 based on the results shown in **FIGURE 114**. **FIGURE 115.a** provides an overview of the control settling time. There is excellent agreement with the estimated control settling time, which nearly all cases falling within the predicted range by the highest and lowest DC grid stiffness cases (shadowed by blue). Minor deviations in a few specific cases are observed, but these are attributed to the local mode of remote station (CNVS4). The participation factor of the subject station in this mode is considered small, and therefore, the validity and effectiveness of the proposed methodology remains unaffected. **FIGURE 115**.b presents a summary of the undershoot values, calculated from 0.5 s after the event to exclude the immediate post-event transient from consideration. While the results for the 5T and 4T cases generally fall within the range estimated by the step power disturbance response tests, there are noticeable discrepancies in the 3T cases due to the previously described medium frequency oscillations, which are beyond the capturing capability of the simple RLC circuit models. It is important to note that the voltage undershoot observed remains well above the DC-FRT profile for the corresponding range and the voltage threshold below which temporary converter blocking may be permitted. Please refer Section 7.3 for more details.



a) Control settling time b) Undershoot value

FIGURE 115 Summary of the KPI evaluation based on the DC voltages at DC-PoC of CNVS2 shown in **FIGURE 114**, compared with the step power disturbance response test results of the DUT for both the highest and lowest DC grid stiffness.

FIGURE 116 shows the AC power at AC-PoC of CNVS2 for all parameter and grid combinations. It is observed that the power settling time can also be effectively captured by the appropriate standalone test using a simplified test environment. This observation is further supported by **FIGURE 117**, where **FIGURE 117.a** and **FIGURE 117.b** provide overviews of the power settling time and power undershoot, respectively, for all combinations and compared to the standalone compliance test of the DUT under both the highest and lowest grid stiffness cases.

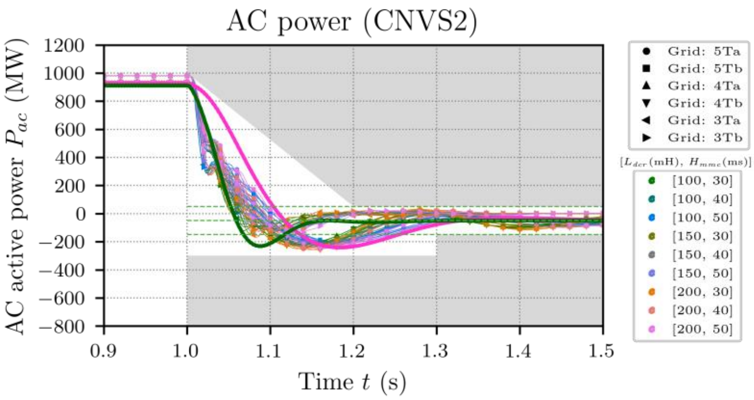
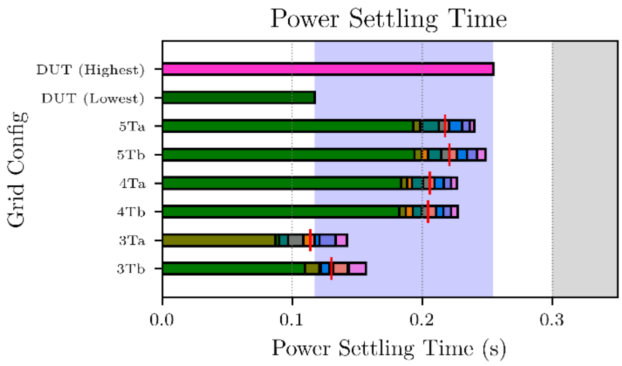
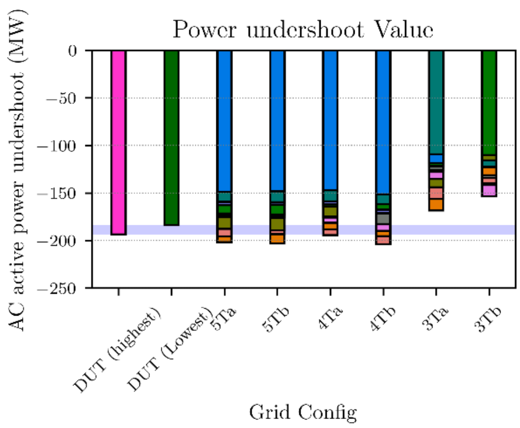


FIGURE 116 Simulation results showing the AC power at AC-PoC of CNVS2, compared with the step power disturbance response test results of the DUT for both the highest and lowest DC grid stiffness.



a) Power settling time

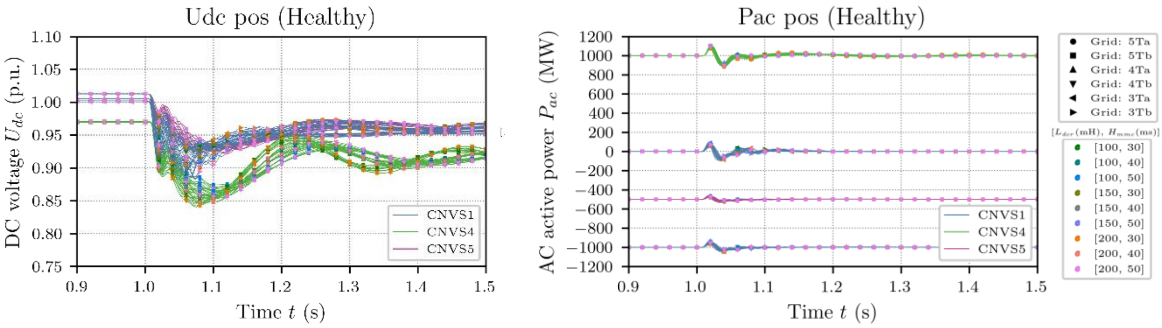


b) Power undershoot

FIGURE 117 Summary of the KPI evaluation based on the AC power at AC-PoC of CNVS2 shown in **FIGURE 116**, compared with the step power disturbance response test results of the DUT for both the highest and lowest DC grid stiffness.

In **FIGURE 118**, the DC voltages at DC-PoC voltage and AC power at AC-PoC of healthy stations are summarized. In **FIGURE 118.a**, noticeable local oscillations are observed at the distant station, CNVS4. Those typical local mode are associated with the fixed power mode converter in inverting operation. Such negative impedance characteristics may contribute to potential stability issues within the system. To mitigate these issues, if feasible, a damping control similar to a DC-PSS should be implemented.

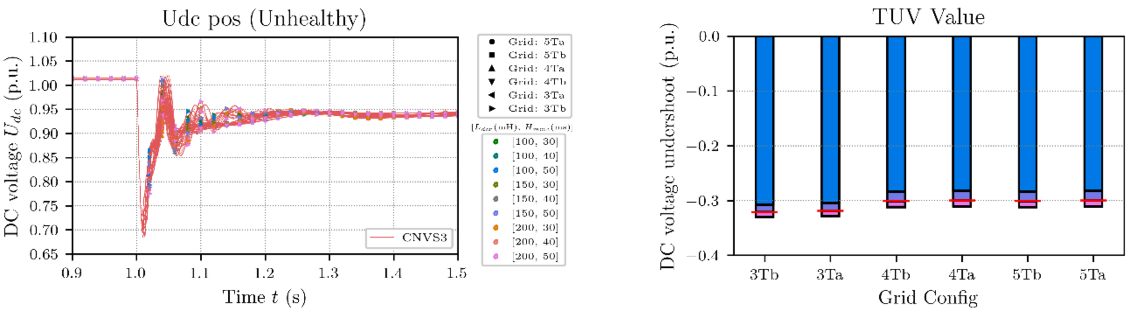
In **FIGURE 118.b**, the power at AC-PoC of healthy stations are shown. Other than a brief fluctuation immediately after the event, no significant impact is observed. This indirectly indicates the adequacy of DC voltage regulation that CNVS2 provides in all cases.



a) DC voltages (positive) at DC-PoCs b) AC power (positive) at AC-PoCs

FIGURE 118 Simulation results showing the AC power at AC-PoCs of healthy stations.

Finally, **FIGURE 119** shows the transient undervoltage observed at the blocked station (CNVS3). An immediate undershoot occurs after the blocking, lasting for approximately 50 ms, which aligns with the transient and semi-transient time range that any equipment must withstand. The control of the remote stations has a marginal effect on this behavior.



a) DC voltage b) TUV

FIGURE 119 Simulation results showing the DC voltage at DC-PoC of the unhealthy station.

9.5.3 Key conclusions and recommendations

To conclude, while the dynamic performance requirements should be specified as an intrinsic capability to an AC/DC converter, its behavior observed in a system depends on the actual grid impedance seen from its DC-PoC. The sensitivity analysis on the impedance profiles of the DC grid has demonstrated that these profiles exhibit consistent trends in the low-frequency range. As this range primarily governs the dominant DC voltage dynamics through the interaction between the DC-side control functions and the grid, it is crucial in evaluating the dynamic performance requirements. These trends can be effectively modelled using a simple RLC circuit, where RLC combinations can reflect the highest and weakest grid stiffness seen from the DC-PoC.

The comparison between detailed demonstrator grid simulations and standalone test results confirms the effectiveness of the standalone dynamic performance studies in assessing the converter's dynamic response capabilities. These can adequately capture critical dynamics, such as settling time of DC voltage and active power, which closely align with the behavior observed in detailed grid simulations. However, some notable discrepancies have also been observed, particularly in the undershoot and oscillations in the

DC voltages. The undershoot appears to be dependent on location of the disturbance and non-linearity of the induced disturbance. In contrast, the observed oscillations are likely a consequence of the simplification inherent in the DC grid equivalent model. The simple RLC circuit was tailored to represent dynamics within a specific range of frequency. Consequently, oscillatory behavior outside of this specific range cannot be captured by such a simplified model. These limitations underscore the necessity of carefully evaluating the frequency range required for accurate representation in the DC grid equivalent for the dynamic performance requirement specification.

The sensitivity parameter considered in this investigation included:

- MMC energy (inertia constant)
- DCSS DCR size
- Grid topology (number of converter stations in the system as well as grid topology (mesh vs radial)
- DC PoC (different onshore stations)

It should be noted that careful attention should be given to the energy control concept of the MMC. Different MMC control schemes in terms of the energy management are available in the literature, e.g. [35], [36], [37], [38], [39] etc.). According to them, it is anticipated that a similar trend in grid impedance within the low-frequency range may generally be expected for many of them. However, in some cases, a significant discrepancy could arise between the assigned value of H_{mmc} and its effective value, depending on the tuning parameters of the energy controller. In such cases, this added complexity must be managed appropriately to ensure accurate modelling. Furthermore, the mere implementation of the DC voltage droop controller, along with other potential AC side related controls (e.g. GFM control) might alter the grid impedance observed at the DC-PoC. In addition, the operating points of power can also affect to the grid impedance. These aspects should also be considered if such variations are relevant for DC-side dynamic performance specifications and their testing procedures.

Overall, the dynamic performance compliance studies using simplified RLC circuits offer a practical and efficient method for assessing the converter's dynamic performance, ensuring it meets the grid expectation, and maintaining the large-disturbance stability of the under varying operational conditions. However, the factors mentioned above can introduce additional dynamics and dependencies, warranting further investigation as a potential research area to enhance the understanding their possible effects on system behavior.

9.6 Example for application and verification of harmonic stability performance requirements

This section outlines the essential considerations for assessing stability performance and identified key factors that influence the system's small-disturbance stability. The prerequisites for the general framework for conducting the stability performance studies, as described in Section 6.6.5, are discussed. It follows with a demonstration using system-level simulations, and the section concludes with recommendations based on the findings.

9.6.1 Expectations for stability performance studies

If DC-side small-signal stability is of concern, the classical impedance-based analysis in frequency-domain can be applied. Consider the DUT interfaces with the grid at the DC-PoC, as illustrated in **FIGURE 120**. Each sub-system can be represented by its small-signal admittance, $Y_{mmc}(s)$ and the Grid impedance $Z_{grid}(s)$, respectively. Together, they form a closed-loop system, as shown in **FIGURE 121**. The stability of the system is determined by the impedance ratio between the converter and the DC grid. The return ratio $L(s)$, which represents the open-loop transfer function of the system, is defined as $L(s) = Y_{mmc}Z_{grid}$. The closed-loop system stability can then be assessed based on the Nyquist stability criterion.

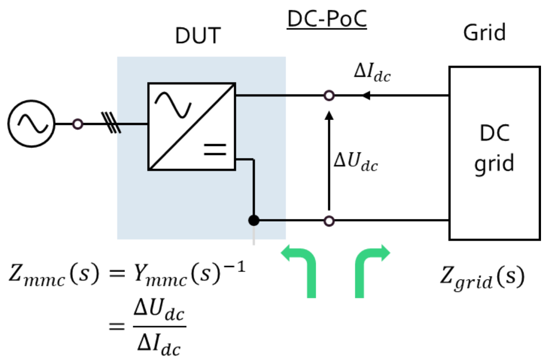


FIGURE 120 Interconnection of DUT and DC grid at DC-PoC.

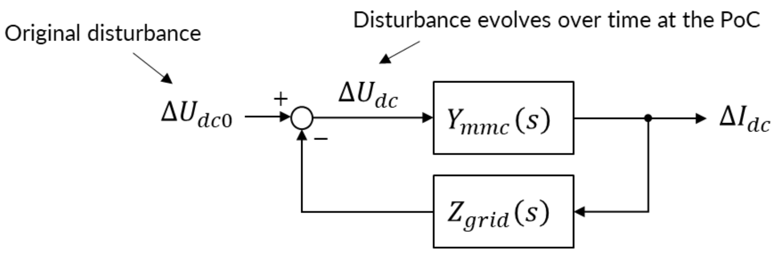


FIGURE 121 Block diagram of a SISO closed-loop negative feedback system formed by the small-signal impedance and admittance of the DUT and grid.

Focusing on the DC-side, this analysis can be readily extended to an *N*-terminal DC grid. Let the impedance matrix, which represents the impedance between each node in the grid, be $\boldsymbol{Z}_{\boldsymbol{edge}}(s)$. Additionally, denote the node admittance matrix as $\boldsymbol{Y}_{\boldsymbol{node}}(s)$, which contains the small-signal admittance of the individual converters. In this case, the system forms a MIMO closed-loop system, as illustrated in **FIGURE 122**. The return ratio matrix of the system is given by $\boldsymbol{L}(s) = \boldsymbol{Z}_{\boldsymbol{edge}}(s)\boldsymbol{Y}_{\boldsymbol{node}}(s)$. The small-signal stability can be assessed by the Generalized Nyquist Criteria (GNC).

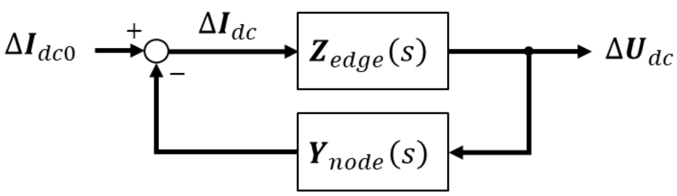


FIGURE 122 Block matrix diagram of a MIMO closed-loop negative feedback system formed by the edge impedance matrix and node admittance matrix.

It is now important to consider how this stability assessment criteria for a MIMO system can be translated into performance requirements for individual DUTs. At the design stage, the scope of functional requirements should be confined to individual sub-systems, and the evaluation of each DUT should therefore be conducted independently. Preferably, performance evaluation metrics should rely solely on the information provided for each manufacturer as inputs.

Consider a DUT to be connected to node k. First, by rearranging the above-mentioned MIMO system to isolate the node admittance $Y_{node,k}(s)$ from the node admittance matrix, $\boldsymbol{Y}_{node}(s)$, we obtain:

$$\boldsymbol{Y}_{node}^{(k)}(s) = \mathrm{diag}(Y_1(s), \dots, Y_{k-1}(s), 0, Y_{k+1}(s), \dots, Y_n(s)\,) = \boldsymbol{Y}_{node}(s) - Y_k(s)\boldsymbol{E}_k$$

where $\boldsymbol{E}_k$ is defined as $\mathrm{diag}(0, \dots, 0,1,0, \dots 0\,)$. The green-shadowed area in **FIGURE 123** corresponds to the grid impedance at the DC-PoC of node k, denoted by $Z_{grid,k}(s)$.

If $Z_{grid,k}(s)$ is stable, the stability assessment of the whole system simplifies to be the same SISO system stability assessment at node k as previously discussed. Therefore, the only required information for the stability performance assessment of the DUT is the aggregated, stable impedance profile, which represents the impedance seen at the connection point.

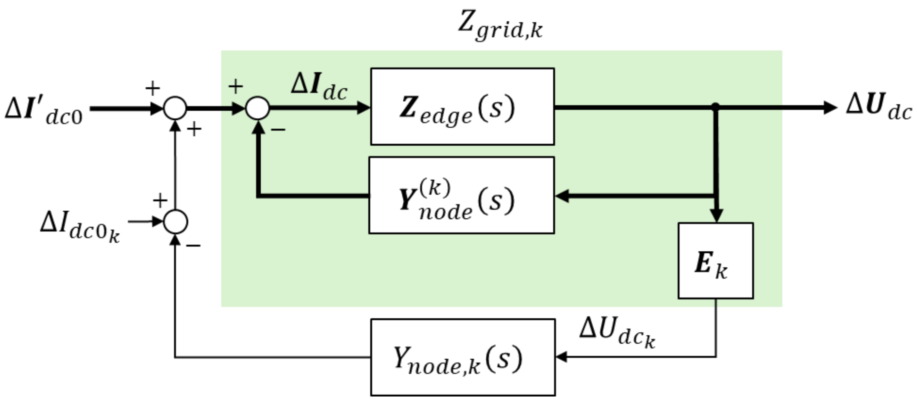


FIGURE 123 Isolated SISO system for stability assessment at DC-PoC of node k.

Thus, to conduct the SISO small-signal stability assessment, each vendor would require appropriate impedance as seen from its respective connection point. This information can only be provided by the entity in possession of the grid mutual impedance $Z_{edge}(s)$ and the admittance profile of the respective converter.

9.6.2 Confirmation by system-level studies

In this section, an application of the evaluation methodology to assess the stability performance requirements, as described in Section 6.6.5, is conducted.

For the demonstration setup, the InterOPERA demonstrator grid, shown in **FIGURE 124** , is considered. CNVS2 is considered the DUT, operating in an initial control configuration denoted **Control A.** The considered grid configuration is a radial 5T grid. According to the test method, the system operator is required to provide the grid impedance $Z_{grid}(s)$ at the relevant DC-PoC. The converter impedance $Z_{mmc}(s)$ can either be analytically obtained or measured by the vendor. To ensure consistency in assessment, conditions for the measurement (including range, resolution, methods, ect.) should adhere to the criteria specified by the system operator. Small-signal stability analysis in the frequency domain can be initiated once $Z_{mmc}(s)$ and $Z_{grid}(s)$ are obtained for a given operating point.

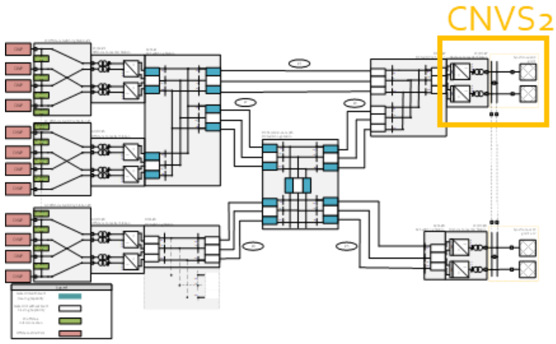
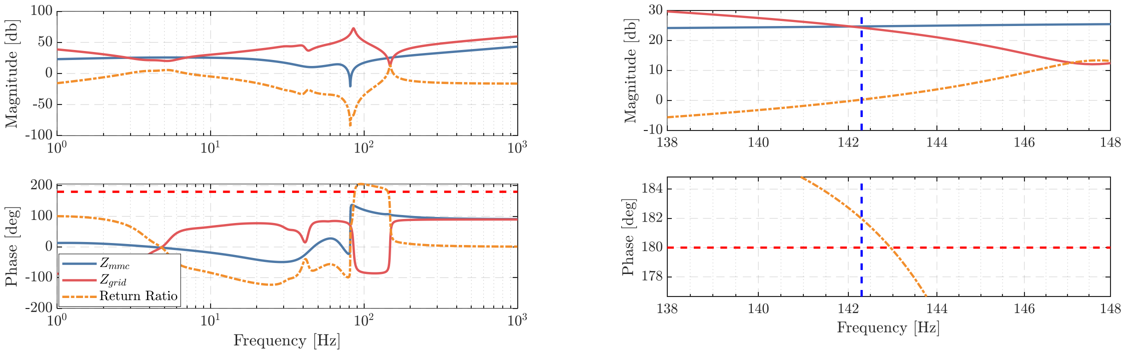


FIGURE 124: InterOPERA demonstrator grid, the Considered DUT is CNVS2

FIGURE 125 shows the Bode plots of the converter impedance $Z_{mmc}(s)$ of CNVS2 operating in **Control A**, the grid impedance $Z_{grid}(s)$ and the return ratio $L(s)$. It is worth mentioning that only the positive pole converter impedance is considered for analysis. According to the Bode stability condition, the system is stable if the phase difference between the converter and the grid impedances is less than 180° degrees at the frequency of intersection of the respective magnitude plots, which is equal to the frequency at which the magnitude $\|L(s)\| = 0dB$. From **FIGURE 125**, at $f_c = 142$ Hz, the phase angle $\angle L(s) > 180°$ indicating a negative phase margin, hence an unstable system.

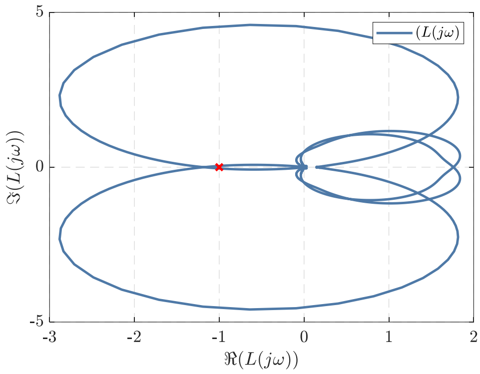


a) Full view

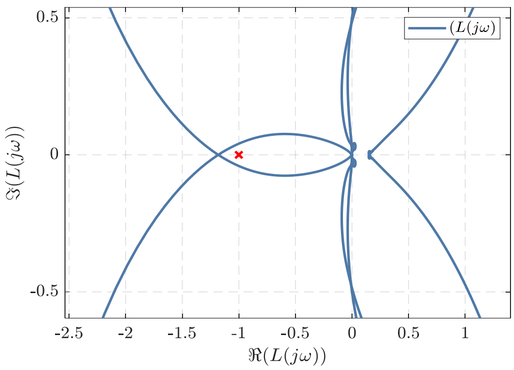
b) Zoomed

FIGURE 125: Bode Plots of $Z_{grid}(s)$, $Z_{mmc}(s)$ and the return ratio $L(s)$ for the case of **Control A**

The results are supported by the Nyquist plot shown in **FIGURE 126**, where an encirclement around the critical point (-1,0) indicates the existence of a RHP pole in the closed-loop system according to the Nyquist stability criterion.



a) Nyquist plot of $L(s)$



b) Zoomed

FIGURE 126: Nyquist plot of the return ratio $L(s)$ for the case of **Control A**

A time domain simulation is conducted to check the validity of the small-signal analysis results. Initially, CNVS2 with **Control A,** is connected to a meshed 5T grid configuration. At t=1.5, Line 1 is tripped and a radial grid configuration is obtained, which corresponds to the grid impedance utilized in the small-signal analysis, represented by $Z_{grid}(s)$.The result, shown in **FIGURE 127**, reveals a slowly growing oscillation of the DC voltage at DC-PoC2 with the exact frequency expected by the small-signal analysis results, confirming the existence negatively damped mode at $f\ = 142$ Hz.

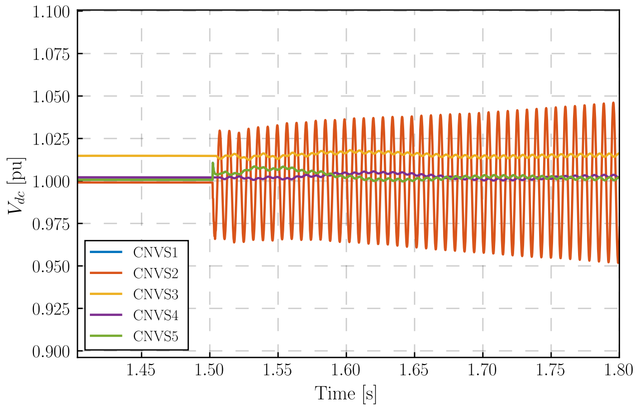
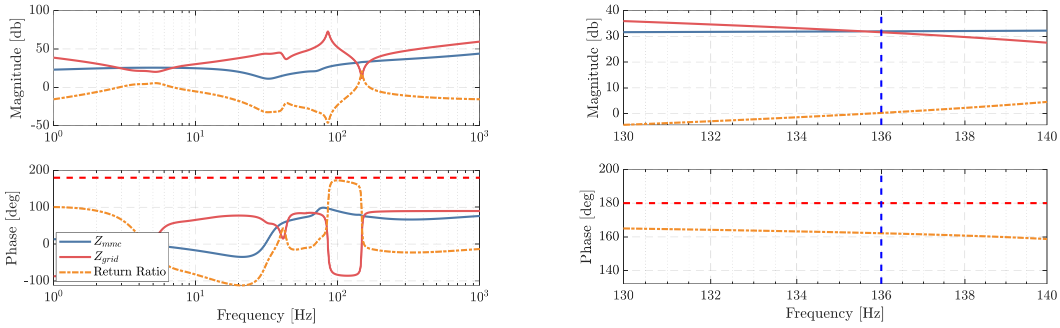


FIGURE 127: Simulation results showing instability at f =142 Hz.

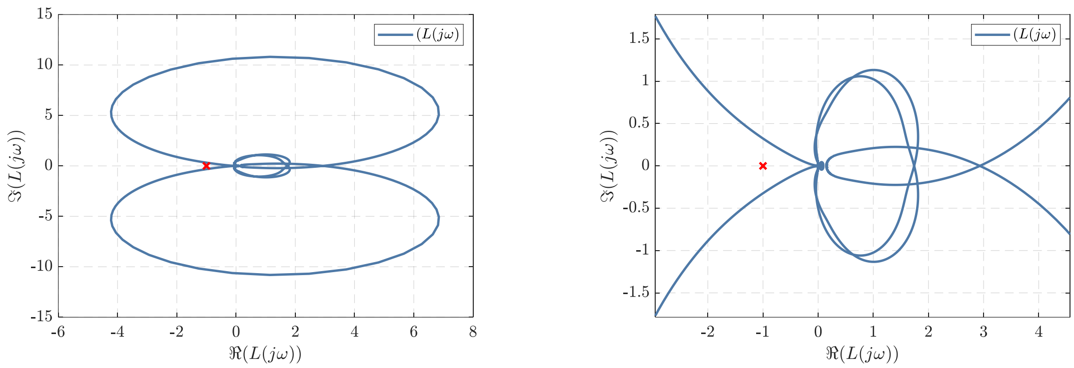
A modified controller**, Control B**, is adapted for CNVS2, to provide positive damping at the frequency range of interest. Although shown as an example, the modification of the controller can either be implemented by adding a dedicated higher-level controller or by modifying the internal control of the DUT. As can be observed in **FIGURE 128**, at $\|L(s)\| = 0dB$, the phase angle $\angle L(s) < 180°$, indicating a stable close-loop system. The phase margin (i.e. the phase angle of $L(s)$ at the gain crossover frequency) is $18°$.



a) Nyquist plot of $L(s)$ b) Zoomed

FIGURE 128: Bode Plots of $Z_{grid}(s)$, $Z_{mmc}(s)$ and the return ratio $L(s)$ for the case of **Control B**

The Nyquist plot considering the modified control, **Control B**, is shown in **FIGURE 129**, which confirms that $L(s)$ makes no encirclements around the critical point, indicating system stability.



a) Nyquist plot of $L(s)$ b) Zoomed

FIGURE 129: Nyquist plot of the return ratio $L(s)$ for the case of **Control B**

Finally, the simulation result shown in **FIGURE 130**, indicates that **Control B** can effectively damp the mode at $f = 136$ Hz, which confirms the small-signal analysis results.

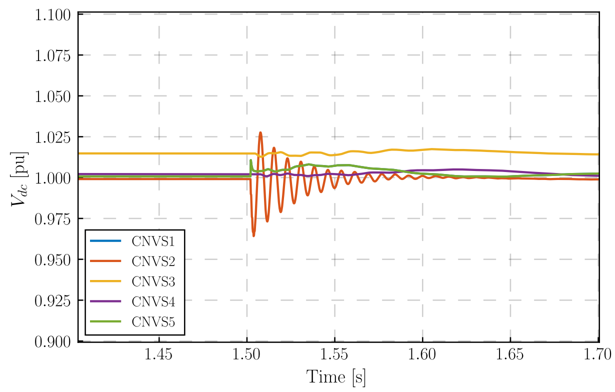


FIGURE 130: Simulation results showing the converter with Control B providing positive damping at f =136 Hz

9.6.3 Conclusions

The converter interaction with the grid has been demonstrated through small-signal analysis in the frequency domain. A use case of the InterOPERA 5T demonstrator grid has been analysed. The results show that small-signal stability can partially be addressed in the standalone compliance testing stage through the converter and the grid impedance at DC-PoC. The findings of small-signal analysis were validated by system level time domain simulations.

In this analysis, only SISO stability considerations are addressed. Specifically, the closed-loop relationship between the DUT and the grid impedance, observed from a given DC-PoC, is evaluated. For a more comprehensive approach to small-signal stability, a MIMO stability analysis should be employed. However, for standalone testing, MIMO stability analysis is impractical, as it requires additional information about the grid configuration and the various DC-PoCs, which introduces higher complexity to the standalone testing procedure. This type of detailed MIMO analysis is more applicable to system integration studies, where sufficient grid information (including the final impedance characteristic of each converter station) is available to identify the root causes of any instabilities, if present.

9.7 Alternative DC-FRT profiles and evaluation

Different approaches of defining DC-FRT capabilities have been discussed within the DC grid protection workstream. This section shall be seen as a complement to section 7.3 with the objective to provide background information on the evaluation process highlighting the main differences and outlining advantages and drawbacks of each of the solutions. It should be noted that a final assessment of the presented options must be based on technical and economical evaluations which cannot be fully concluded in the scope of InterOPERA.

TABLE 39 summarizes the different approaches of how a DC-FRT could be described. They differ mainly in terms of genericity and the quantity they are expressed in.

TABLE 39 Different categories for DC-FRT definitions

Option	Description	Quantity
1	Design / topology dependent	DC Current based
2	Design / topology dependent	DC Voltage based
3	Generic	DC Current based
4 (see section 7.3)	Generic	DC Voltage based

Evaluation criteria

- **Technological agnostic:** Are the functional requirements permitting different technological solutions or are they restricting, excluding certain technologies?
- **Functional split:** Are functional description and design of subsystems independent? How to split functional responsibilities?
- **Oversizing :** Does the decoupling of subsystem requirements and the genericity / system independence generate an oversizing?
- **Standardization:** Is the DC-FRT description subsystem-dependent or generic? Do several DC-FRT profiles co-exist?
- **Verifiability :** Can the DC-FRT profile be specified at the DC-PoC based on local measurements?

9.7.1 Generic vs design / topology dependent approach

Considering a design / topology dependent DC-FRT description, the following questions arise and reveal potential drawbacks. For each of the identified drawbacks, the advantages of a generic DC-FRT description as defined in section 7.3 are expressed.

Functional split: Are functional description and design of subsystems independent? How to split functional responsibilities?

Standardization: Is the DC-FRT description subsystem-dependent or generic? Do several DC-FRT profiles co-exist?

- For a design / topology dependent approach as proposed in the IEC TS 63291, a DC-FRT curve would need to be defined for each operational concept and each protection sequence with a dependability between converter FRT and fault clearing. The current response and overcurrent limits depend on the specific sub-system design.

- The DC-FRT voltage profile as described in section 7.3 defines an outer envelope which is valid for all fault transients at the DC-PoC of the converter independently from the converter type. This approach has been evaluated in EMT simulations based on a reference system. Functional requirements and subsystem compliance standalone tests are generic and non-project, non-station specific.

Technological agnostic: Are the functional requirements permitting different technological solutions or are they restricting, excluding certain technologies?

- The DC-FRT requirements as defined in section 7.3 do not distinguish between CO and TB. The overall objective is to ensure stable operation after fault separation. It is well understood that converter IGBT components are highly sensitive to overcurrents and dedicated limits must be respected to avoid any damage. However, it must be acknowledged that several different technical solutions exist to limit the increase of converter fault current during DC faults and that the functional description shall not impose one of them. For instance, some sub-module topologies (e.g. full-bridge) allow to control fault currents. In case of half-bridge topology, the actual converter overcurrent capability may vary depending on the IGBT design. The limitation of current increase by means of fault current limiting devices such as DC reactors.
- For half-bridge topology innovative control solutions such as temporary blocking can further avoid damage of IGBTs by taking them out of the circuit during transients while ensuring stable operation after DC voltage recovery. From a technical perspective on the DC side, the performance of a temporary blocking converter is not by default worse than a converter in continued operation.

Continued operation comes with costs, especially due to increased requirements on converter overcurrent capabilities and increased size of DC reactor. Those can be significantly reduced with a temporary blocking function and the impact need to be thoroughly assessed. The deblocking can be done quasi-instantaneous once DC voltage and current recovered to operational range leading to a temporary blocking time range of several ms to few tens of ms.

The DC-LVRT profile is therefore described independently from the actual converter fault current contribution without distinguishing between continued operation and temporary blocking.

Functional split: Are functional description and design of subsystems independent? How to split functional responsibilities?

- The protection zone matrix approach from the IEC TS 63291 defines converter FRT requirements for each protection zone creating an interdependence between protection zoning and converter FRT requirements.
  A protection zone shall not be confounded with converter FRT requirements. A converter outside a protection zone shall by definition avoid permanent stop and ensure operation after fault separation. The DC-FRT requirement as defined in section 7.3 defines an outer envelope ensuring that converter units have enough withstand capability to allow DC grid protection actions for fault separation. The fault separation requirements are specified separately in section 7.2.4 and section 7.4.

Verifiability : Can the DC-FRT profile be specified at the DC-PoC based on local measurements?

- The design / topology dependent approach from the IEC TS 63291 defines operational requirements to the converter for each FSZ independently. It remains unclear how such superposed requirements

can be verified at the DC-PoC of the converter.
The DC-FRT requirements as defined in section 7.3 provide a clear split between converter unit and switching unit functional requirements.

9.7.2 Alternative DC-FRT profiles

The DC-FRT requirements can be expressed either in DC voltage or DC current quantities, they can be either generic or design-based leading to four options as listed in **TABLE 40**. Considering that the generic voltage-based approach (option 4) has been described in section 7.3 as the preferred option, two current based options (design based (1) and generic (3)) and one design-based voltage option (2) are described and evaluated in the following.

TABLE 40 Comparison of functional requirement definition for different DC-FRT descriptions

Functional requirement	Option 1 DC Current quantities (design based-CO)	Option 2 DC voltage quantities (design based-CO)	Option 3 DC current quantities (generic)	Option 4 DC Voltage quantities (generic)
1 Converter-Connection requirement	converter station must withstand a predetermined converter-specific short-circuit current profile and remain connected	converter station must withstand a predetermined voltage profile (conservative outer envelope) and remain connected	converter station must withstand a predetermined short-circuit current profile (conservative outer envelope) and remain connected	converter station must withstand a predetermined voltage profile (conservative outer envelope) and remain connected
2 Converter-Operational requirement)	converter station must remain in continued operation	converter station must remain in continued operation	converter station must deblock after a certain time if blocked after voltage recovery	converter station must deblock after a certain time if blocked after voltage recovery

All DC-FRT curves need to be defined in a way that enough withstand capability of the converter is ensured to ride through the fault according to the same fault transients. A minimum circuit can be derived under the assumption that adjacent lines are disconnected leading to the highest current contribution of the converter (no voltage support from adjacent lines leading to the most severe voltage drop at the converter DC-PoC). The simplified circuit is depicted in **FIGURE 131**. It consists of the following elements:

- L_{DCSS}: DC inductance of the DC switching station
- L_{dcMMC}: Equivalent DC inductance of converter unit
- U_{dc}: Rated converter DC voltage represented by an ideal voltage source

- U_{TW}: Controlled voltage source emulating DC fault transients including traveling wave phenomena
- $L_{sum}=L_{DCSS}+L_{dcMMC}$

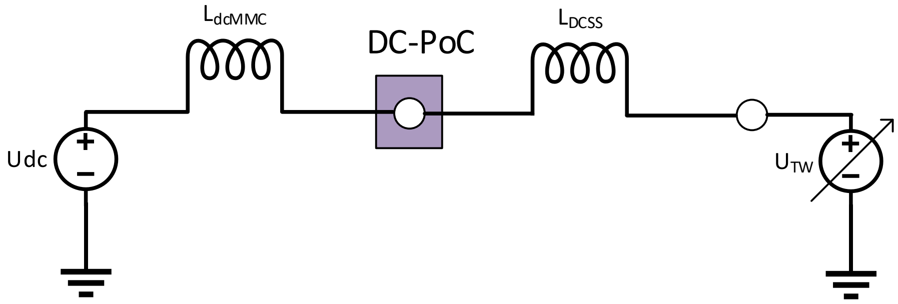


FIGURE 131 Simplified circuit to determine equivalent DC inductance to ensure DC-FRT requirements

FIGURE 132 shows an example of DC voltage evolutions for different fault distances emulated by the controlled voltage source U_{TW} from fault arrival (T=0s) to fault neutralization (T_N=5ms). The controlled voltage source considers cable losses by a simplified damping factor and ideal reflection coefficient equal to two. This is a worst-case approximation considering an inductive cable termination. This profile represents an outer envelope for DC fault transients independently from the converter type. The converter type, rating or control may or may not have an influence on the actual voltage at the DC-PoC but this does not change the outer envelope related to DC fault transients.

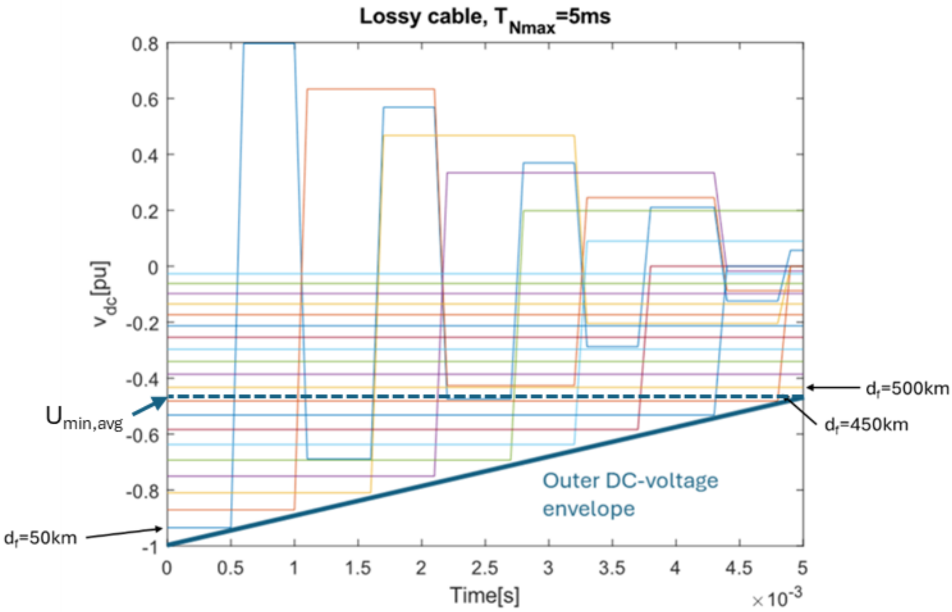


FIGURE 132 Possible DC voltage transients at cable termination depending on fault distance (d_f=50...1000km) for a fault neutralization time of 5ms (for illustration purpose); $U_{min,avg}$: Minimum average undervoltage during fault neutralization

For both design-based solutions an illustrative calculation example DC inductor sizes will be provided in the dedicated section considering hypothetical boundary conditions (design constraints, see **TABLE 41**) for converter station and switching station according to the simplified circuit shown in **FIGURE 132**.

TABLE 41 Example parameters for equivalent DC inductance determination

Subsystem	Design parameter description	Parameter	Value
DC system	Rated DC voltage	U_{dc}	525kV
	Maximum fault neutralization time	$T_{N,max}$	5ms
Converter station	DC overcurrent limit for CO	$Idc_{Max,CO}$	4kA (2pu)
DC switching station	Maximum DC current breaking capability	I_{cbc}	20kA

9.7.2.1 Option 1: Design based solution based on current for continued operation

The current based approach defines the DC-FRT based on overcurrent capabilities that the converter station needs to withstand during fault neutralization while remaining in continued operation. It should be noted that the approach focusses on primary protection and continued operation. Different DC-FRT profiles are expected to be defined for backup protection and temporary stop (temporary blocking).

FIGURE 133 shows two concepts of DC-FRT profiles based on DC overcurrent. For both concepts it is assumed that the TSO defines the following key parameters for an MTDC grid or a zone thereof:

> $Idc_{Max,CO}$: DC overcurrent capability requirements of converter stations

> $E_{max,CO}$ / $\Delta Q_{max,CO}$: Energy rating or charge of the converter station to remain in CO

> $T_{N,max}$: Maximum fault neutralization time (indirectly defined by $Idc_{Max,CO}$ and max di/dt in concept (a), explicitly specified in concept (b))

Concept (a) additionally defines maximum and minimum di/dt values:

> Max di/dt: Maximum increase of DC fault current

> Min di/dt: Minimum decrease of DC current during fault current suppression

For concept (b) the following design based approach has been proposed:

> Specify converter parameters: $\Delta Q_{max,CO}$ and $Idc_{Max,CO}$

> Specify fault separation related switching unit parameters: $T_{N,max}$, ICBC (current breaking capability)

> Specify inductances L_{DCSS} and L_{dcMMC}

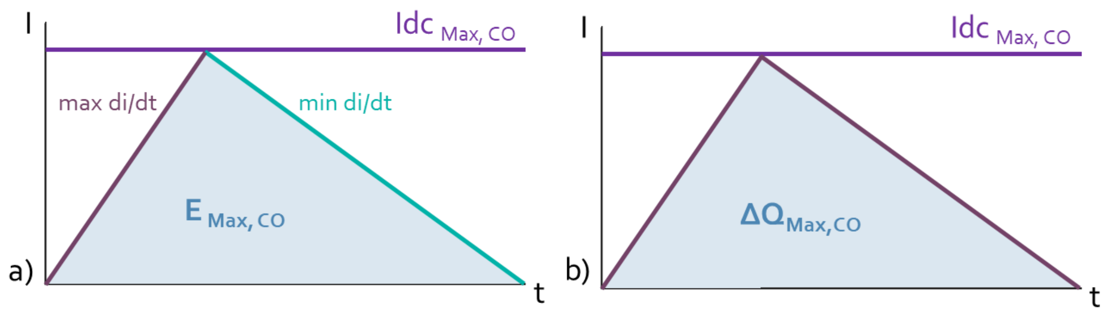


FIGURE 133 Design based DC-FRT profile based on DC overcurrent; With and without specification of maximum and minimum di/dt respectively represented by concept (a) and concept (b)

In concept (a), to ensure that min di/dt ≤ di/dt ≤ max di/dt the grid operator needs to choose the equivalent DC inductance accordingly. This involves coordinating the DC inductance between the converter station and the DCSS as the increase of the fault current is directly dependent on the design of both subsystems as shown by the simplified circuit in **FIGURE 131**. The equivalent DC inductance is the sum of L_{DCSS} inside the DCSS and L_{dcMMC} inside the converter station assuming an ideal voltage source as a worst case. The maximum di/dt represents an average current increase from fault arrival to fault neutralization ($T_{N,max}$). It should be noted that it can be temporarily higher (e.g. for close faults during voltage reversal). This should be considered for the final definition of the design-based DC-FRT curve based on current as a temporarily higher increase of current while remaining below the absolute current threshold shall not lead to a disconnection of the converter. Simplified equations to determine minimum inductances to keep the converter in continued operation are provided in the following, where $U_{min,avg}$=-0.46 U_{dc} and Idc_r=2kA correspond respectively to the minimum average undervoltage as indicated in **FIGURE 132** and the rated converter DC current in this example.

$$L_{sum} = L_{dcMMC} = \frac{U_{dc} - U_{min,avg}}{Idc_{Max,CO} - Idc_r} T_{N,max}$$

$$L_{DCSS} = \frac{U_{dc} - U_{min,avg}}{I_{cbc} - Idc_r} T_N$$

Applying the example based on parameters listed in **TABLE 41**, a minimum total inductance of 1916mH would be needed to ensure continued operation. The minimum inductance design for the DCSS would be of 212mH. After coordination between DCSS vendor and converter station vendor, an optimized design of 212mH for the switching station and 1704mH for the converter station is possible.

Technological solutions: The current-based approach is a pragmatic solution limiting the design space due to pre-defined technical choices which directly defines converter functional requirements with overcurrent capabilities which is understood to be the most critical design constraint. On the other hand, overcurrent limits risk to exclude some converters with low overcurrent capabilities. Different from the DC voltage FRT definition, where the transient part corresponds to an outer envelope of DC fault undervoltages, the overcurrent is a response to undervoltage which depends on the technical solution. Advanced technical solutions such as temporary blocking or fault current control (ex: full-bridge) are penalized if the short-circuit level is chosen to make all vendors able to comply. In fact, for those advanced solutions, similar performance could be achieved with significantly lower requirements on both the equivalent DC inductance and the converter requirements.

Interoperability-by-design: If the current response and overcurrent limit is tailor made, the response according to faults is predictable. Further investigation is required to verify to which extend different design concepts may coexist in an MTDC grid.

Standardization: Functional requirements and subsystem compliance standalone tests depend on the specific project and/or station inside a project, they are project and/or station specific. By now it is not clear how several DC-FRT curves may co-exist in this design-based approach (e.g. DC-FRT curve for CO, TB, primary, backup). Application of several DC-FRT curves may add complexity.

Oversizing: The DC inductance design is tailor made with low overdesign for a pre-defined overcurrent limit. However, the overcurrent limit could be seen as arbitrary since the primary purpose is to ride through DC fault transients represented by a voltage drop. Imposing an overcurrent might lead to oversizing restricting advanced technical solutions for converters (e.g. temporary blocking, energy-based control, fault current control).

9.7.2.2 Option 2: Design based solution based on voltage for continued operation

The voltage-based approach defines the DC-FRT based on a voltage profile that the converter station needs to withstand during fault neutralization while remaining in continued operation considering the DC switching station design between DC fault location and converter station resulting in the simplified circuit as shown in **FIGURE 131**. It should be noted that the approach focusses on primary protection and continued operation. Different DC-FRT profiles are expected to be defined for backup protection and temporary stop (temporary blocking).

The functional requirements and design constraints are formulated in the following:

Functional requirement

A worst-case retained voltage profile **UV1** (see outer envelope, **FIGURE 132**) at the DC-PoC of the DCSS, for which the DCSS must be able to interrupt the consequential current.

A minimum equivalent converter inductance $\mathbf{L_{dcMMC,min}}$ that the converter must provide. This, for example, can be obtained by consensus amongst vendors.

A minimum equivalent DCSS inductance $\mathbf{L_{DCSS,min}}$ that the DCSS must provide and a maximum neutralisation time $\mathbf{T_{N,max}}$.

DCSS vendor design

The DCSS vendor chooses a $\mathbf{L_{DCSS}}$, which must be no less than $L_{DCSS,min}$, based on UV1, $L_{dcMMC,min}$, their FSD's T_N and $I_{FSD,max}$, assuming maximum DC system voltage behind the $L_{dcMMC,min}$ inductance.

Converter vendor design

The converter vendor chooses a $\mathbf{L_{dcMMC}}$, which must be no less than $L_{dcMMC,min}$, based on UV1, the $L_{DCSS,min}$, $T_{N,max}$ and their converter's overcurrent capability $Idc_{Max,CO}$.

Applying the example based on parameters listed in **TABLE 41**, a minimum total inductance of 1916mH would be needed to ensure continued operation. The minimum inductance design for the DCSS would be of 212mH. No co-ordination between the converter station vendor and the DCSS vendor is needed because the two are decoupled by the $L_{dcMMC,min}$ and $L_{DCSS,min}$, at the cost of potential oversizing of inductors.

Technological solutions: The voltage-based approach is a pragmatic solution which does not impose an overcurrent capability which is understood to be the most critical design constraint. The converter vendor can adjust the design in a way that continued operation is ensured, for example by adjusting the DC inductance. This DC-FRT is limited to continued operation but can be extended to cover temporary blocking functionalities and backup protection.

Interoperability-by-design: Further investigation is required to verify to which extend different design concepts may coexist in an MTDC grid.

Standardization: The DC-FRT specifications in terms of DC voltage are specified at the DC-PoC of the DC switching station with a certain dependence on the DC switching station design. By now it is not clear how several DC-FRT curves may co-exist in this design-based approach (e.g. DC-FRT curve for CO, TB, primary, backup). Application of several DC-FRT curves may add complexity.

Oversizing: The DC inductance design is tailor made with low overdesign for a pre-defined undervoltage profile.

9.7.2.3 Option 3: Generic DC-FRT profile based on current

A generic description should result in a single DC-FRT curve based on DC current independent from specific converter designs and DC grid topologies. Considering this, the DC-current envelope should be valid for both continued operation and temporary stop (including advanced solutions such as temporary blocking). Generic outer envelope for operational current limit and total overcurrent limit needs to be specified. The operational limit needs to correspond to overcurrent in unblocked state, total overcurrent limit needs to be specified for blocked state. It seems challenging to determine a generic envelope for the rate of rise of fault current for both converter states. To cover all cases in a generic manner, the outer envelope may lead very high short circuit currents (e.g. diode-rectifier fault current with strong AC grid).

9.7.2.4 Option 4: Generic DC-FRT profile based on voltage

See DC-FRT requirements of converters, section 7.3.

9.8 Example for application and verification of protection requirements

To test and verify that the protection requirements proposed in this document are valid and include all main characteristics, a verification methodology is considered and illustrated in **FIGURE 134**. The methodology starts with the definition of the protection-related functional requirements as presented in this chapter and in particular in section 7.3 and 7.4 for DC-FRT and fault separation respectively. Based on these requirements, the standalone tests are proposed to design the subsystems (i.e., converter and switching stations). Then, the standalone tests are applied to the subsystems to have a design compliant with the requirements. The last step is to include all subsystems in a common network to evaluate their behaviour during the system-level verification. This last step uses EMT simulation and a set of KPIs to corroborate that the results obtained are compliant with the system requirements. After the system level verification, the results can be used to adjust the protection requirements including the learnings of the network application.

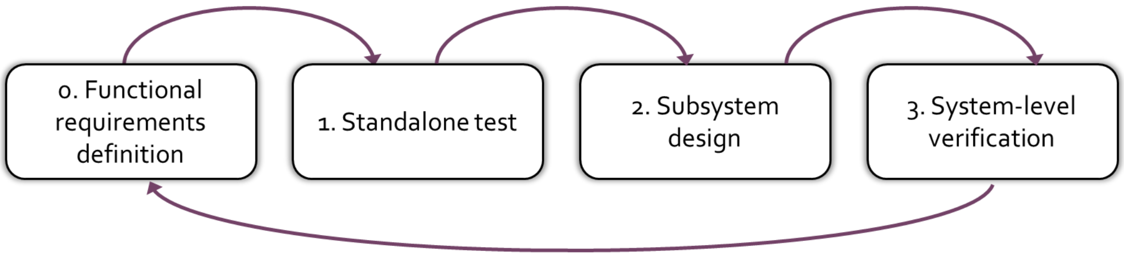


FIGURE 134 Main stages of the methodology proposed to test the functional requirements in a system.

Disclaimer: The values and hypotheses considered in this appendix are used as example. The main goal of this section is to provide an example for the application and verification of the protection functional requirements.

9.8.1 Functional requirements definition

The grid protection functional requirements have been presented in this chapter. Starting from the definitions in Section 7.1, defining the system requirements in Section 7.2, to the DC-FRT and fault separation requirements in sections 7.3 and 7.4 respectively.

As presented in Section 7.3.6, the converter station must respect the FRT requirements at the DC-PoC. According to **FIGURE 54** the FRT profile can set with the parameters presented in **TABLE 30**. The **TABLE 42** presents the proposed values for the DC-FRT parameters used in this example. Based on these values, the standalone tests can be applied, as presented the following section.

TABLE 42 Proposed parameters to test the DC-FRT

Parameters	Value	Hypotheses/ Reasoning
U_{UV1}	-1 [p.u.]	Worst instantaneous transient found for a fault near the PoC, see **FIGURE 56**
U_{UV2}	-0.25 [p.u.]	Average undervoltage based on **FIGURE 61** (depending on T_{rec1})
U_{UV3}	0.6 [p.u.]	Estimated voltage recovery level

U_{UV4-1}	0.75 [p.u.]	Worst estimated undervoltage to keep an MMC operational during T_{rec1}, related to U_{UV4-2}
U_{UV4-2}	0.8 [p.u.]	Based on dynamic operating bands defined in Section 6.2.2
U_{UV5}	0.9 [p.u.]	Based on static operating band defined in Section 6.2.1
T_{rec1}	7 [ms]	Assuming $T_{N\,max} = 5$ [ms] and $T_{buffer} = 2$ [ms]
T_{rec2}	50 [ms]	Estimated time to recover dynamic bands
T_{st}	200 [ms]	Estimated time to recover static bands
ΔT_{dblk}	0 [ms]*	Assuming immediate converter deblock once the operating conditions are recovered

* 10 [ms] were initially proposed, for this study no delay is considered.

9.8.2 Standalone tests and subsystems design

9.8.2.1 Test network definition and modelling

As an example, a five terminals system based on the system proposed in [17], is used in this study to test the protection functional requirements. The simplified model is presented in **FIGURE 135**, where the locations and connections between converter (CS) and switching stations (DCSS) are presented.

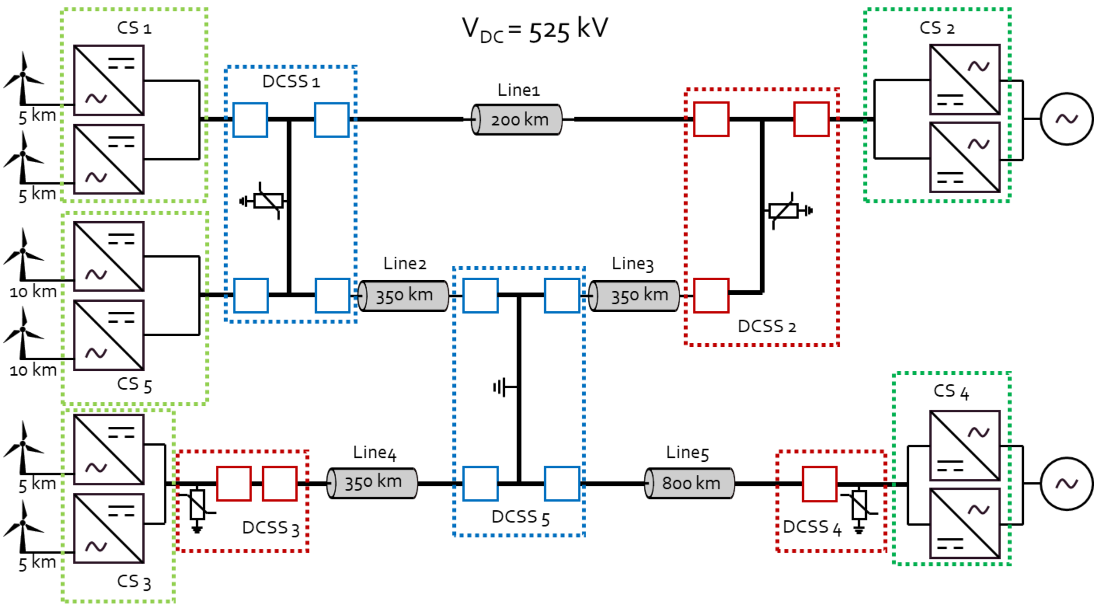


FIGURE 135 Simplified schematic for the five terminal test system[54]. The offshore AC-DC converters on the left are connected to windfarms and set in V/f control. The onshore converter stations on the right are set in DC droop control. The blue DCSSs contain FSD, the red DCSSs contain only disconnectors.

Note that no energy absorbers have been considered. To ensure that after the considered contingencies a load-flow within converter ratings is obtained, the initial load flow has been set as follows: CS1,3,5 injecting 320 [MVA] into the DC network. The CS2,4 are in droop control with P_{ref}=450 [MW] and

[54] The length of lines 1 and 3 are not the same lengths used for the 5 terminals demonstrator.

V_{ref}=525 [kV]. With this initial power flow, in case of loss of one of the onshore stations (e.g., faults in line 1, 3 or 5), the second one will take over without exceeding its rated power. The reactive power exchange has been set to 0 [MVA].

DCSUs

The model focusses on protection related aspects of a DCSU. Two types of DCSU have been considered, the first DCSU without current breaking capability and the second with FSD. Both models are presented in **FIGURE 136**. The DCSU with CBC uses a FSD representation with a surge arrester in the energy dissipation branch (providing the TIV during the current breaking) in parallel to an ideal switch in the main branch. The surge arrester V-I characteristics is presented in **TABLE 43**. The DCR (L) is sized using the standalone procedure presented in Section 7.4.3.

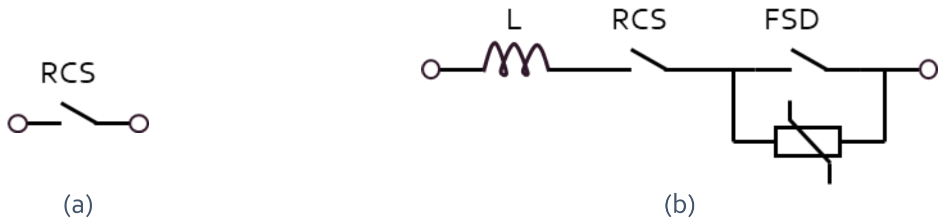


FIGURE 136 Simplified DCSU models. (a) without current breaking capability, (b) including an FSD.

TABLE 43 V-I table for the surge arrester in the DCSU with CBC.

Current [kA]	Voltage [p.u.]
0.0000001	0.451807229
0.0000002	0.518072289
0.0000005	0.572289157
0.000001	0.602409639
0.000005	0.63253012
0.00001	0.638554217
0.00005	0.644578313
0.0001	0.65060241
0.0005	0.656626506
0.001	0.662650602
0.005	0.674698795
0.01	0.680722892
0.05	0.722891566
0.1	0.771084337
0.5	0.837349398
1	0.861445783
2.5	0.903614458
5	0.945783133
10	1
20	1.072289157
40	1.168674699
100	1.445783133

For the considered system presented in **FIGURE 135**, DCSS1 and 5 consider DCSU with FSD, while DCSS2,3,4 do not have current braking capability.

AC equivalents

The onshore AC grid has been modelled as a strong grid with a short circuit power around 43 GVA, 50 [Hz] and 400 [kV]. Both, onshore and offshore converter stations, consider a transformer leakage of 15 [p.u.] with onload losses of 1%, and magnetizing current of 1%.

The offshore AC side is modelled as an aggregated windfarm per DC pole operating at 66 [kV_{ac}]. The simplified windfarm model is presented in **FIGURE 137**. The model is composed of a generator model, that changes the generated power based on the wind speed. The model also considers an internal DC bus interfaced by AC-DC converters, a DC chopper to avoid overvoltage, and AC filters at each AC terminal. In case of an AC fault the windfarm is not tripped, it has a continuous, degraded, operation. The windfarm model does not consider any disconnection strategy nor islanded mode operation. The frequency and voltage amplitude on the offshore AC side are controlled by the AC-DC converters.

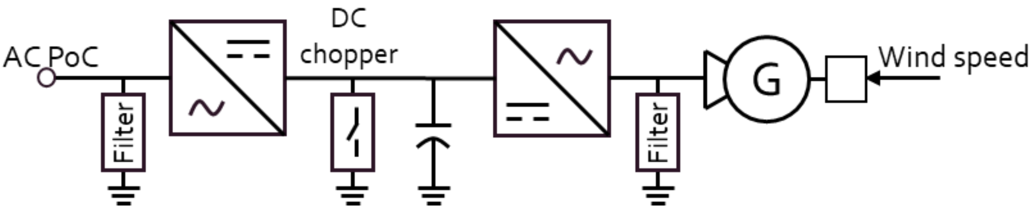


FIGURE 137 Simplified, aggregated, windfarm model.

Cable

The geometry of cable considered for the simulations is presented in **FIGURE 138**, while the main parameters are presented in **TABLE 44**.

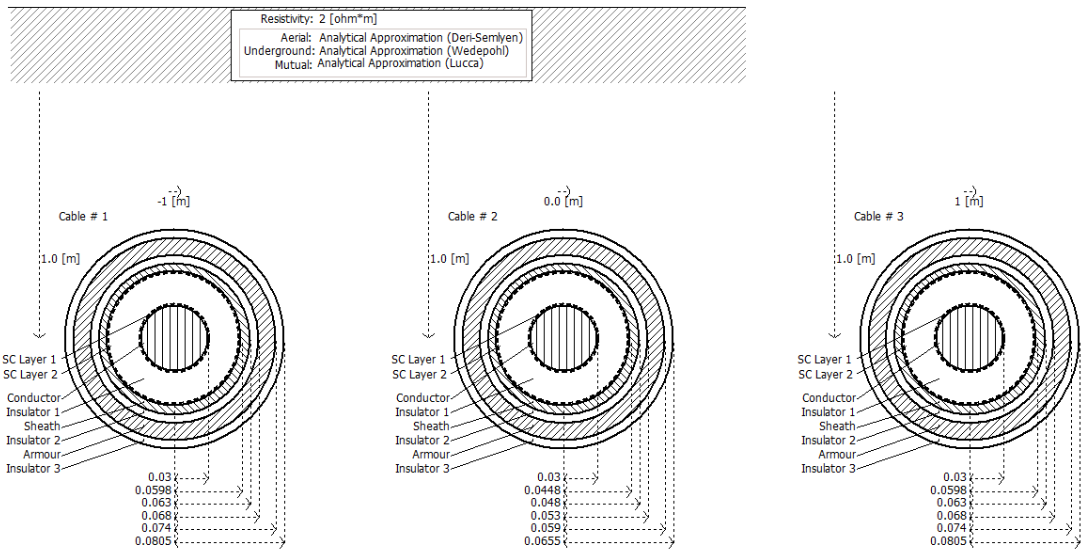


FIGURE 138 Geometry and spatial distribution of the cable model used.

Changing the electrical parameters of the cable can change the system behaviour. For instance, increasing the resistivity of the second conducting layer (sheath), can increase the damping factor for transient events. The cable considered for this analysis assume a low resistance (low damping) corresponding to an aluminium sheath as a worst-case scenario.

TABLE 44 Electrical parameters used for the HVDC cable model.

Location	Parameter	Value
Core	Resistivity	2.4357 e^{-8} [Ω·m]
	Relative permeability	1
First insulating layer	Semi-conducting layers	Present
	Relative permittivity	2.4
	Relative permeability	1
First conducting layer	Resistivity	2.8 e^{-8} [Ω·m]*
	Relative permeability	1
Second insulating layer	Relative permittivity	2.4
	Relative permeability	1
Second conducting layer	Resistivity	1.8 e^{-7} [Ω·m]
	Relative permeability	10
Third insulating layer	Relative permittivity	1
	Relative permeability	1

* If a lead sheath is considered, a resistivity of 2.14e^{-7} [Ω·m] should be used.

Converters

The converter stations consider a non-energy based, average half-bridge MMC model, based on the models developed by the CIGRE and available in [40]. The average model is equivalent to a type 4 defined in [41].

The model was modified to block depending on the arm current and the DC voltage measured at the DC PoC (external measurement as presented in **FIGURE 139**). The converter can be permanent blocked, for converters designed for CO, or temporary blocked allowing the TB functionality. This blocking logic is only implemented to test the DC-FRT and the TB functionality allowing the blocking by voltage.

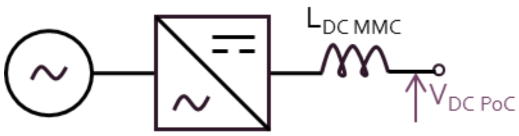


FIGURE 139 Measurement of DC voltage at PoC.

The blocking logic is presented in **FIGURE 140**. The absolute value of arm currents is compared to the arm current blocking limit (in this case 4 [kA]) to trigger the blocking signal (**FIGURE 140**a). When the current is below the threshold the blocking signal (by overcurrent) is deactivated instantaneously. **FIGURE 140**b presents the blocking signal by voltage. In this case a hysteresis is used. The converter blocks if the voltage is below 0.75 [p.u.] and deblocks if the voltage is above 0.8 [p.u.]. The converter is blocked in one of the two signals is true. Consequently, the converter is only deblocked if the current and DC voltage have recovered acceptable levels.

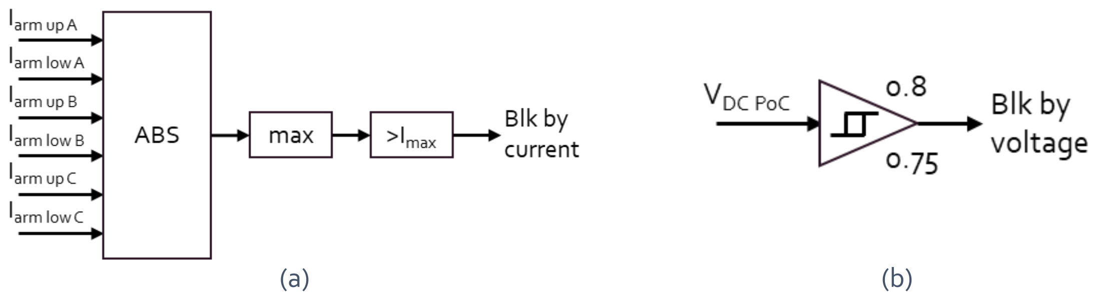


FIGURE 140 Converter blocking implemented. (a) based on current and (b) based on voltage.

When the converter is blocked all PI correctors are reset and the control is restarted slowly. This is achieved with rate limiter that restarts the control in 0.1 [s]. This can be evidenced in **FIGURE 158** where the TB converter restart the AC reference in 0.1 [s]. This behavior increases the startup time after a TB. Different control strategies during the TB can be adopted to reduce this time (e.g., freezing the PLL or synchronizing with the AC voltage kept by the WFs).

The main MMC parameters, used in this study, are presented in **TABLE 45**. The blocking strategy based on external voltage measurement has been implemented to reflect and test the proposed FRT. Converter stations provided in the market might use different measurements to protect the equipment. Furthermore, the TB capability is not widely provided for HVDC converters available in the market. This functionality is considered in this example to explore its capabilities.

TABLE 45 Main MMC parameters.

Parameters	Value
Energy	40 [MJ]
Number of cells	278
Arm current blocking limit	4 [kA]
Arm inductance	43 [mH]
DC inductance	Depending on the FRT strategy and standalone test
Rated power	1 [GVA]
Blocking delay	150 [µs]

9.8.2.2 Converter design from standalone test

To evaluate the standalone test; two converter designs are proposed. A converter with TB functionality and another without TB (reminding that the TB functionality is considered in this example to check its impact on the grid stability). The test and results are presented below.

The proposed standalone test presented in **FIGURE 60**, where the voltage profile depends on the DC-FRT parameter T_{rec1} (see **FIGURE 61**), has been proposed to respect the aforementioned DC-FRT requirements.

One solution for the converter station to be compliant with the requirements is to change the DCR size such that the converter does not reach internal overcurrent capability limits during the DC-FRT. However, if the converter can provide the temporary block functionality, the DCR sizing depends, mainly, on the conditions during the blocked state. A minimum inductance size can be calculated depending on each manufacturer designs. For instance, but not limited to this, the DCR can be size to respect the semiconductor devices thermal capability.

Using an MMC generic model; considering the parameters presented in **TABLE 45**, the maximum arm current has been measured depending on the DCR and are presented in **FIGURE 141**. It is worth noting that additional requirements could be necessary to correctly size the DCR but; it depends on the sizing criteria of each vendor. For this study, a DCR of 200 [mH] is considered for a converter design with TB.

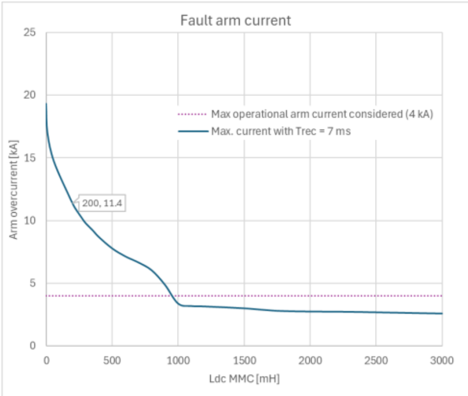
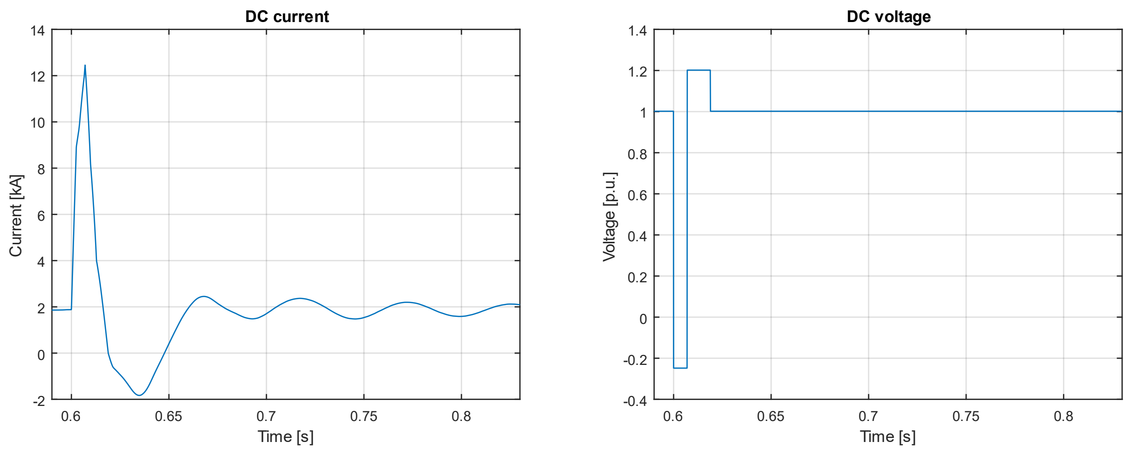


FIGURE 141 Maximum fault arm current measured, depending on the DCR. An MMC generic model has been used considering the parameters presented in **TABLE 45**.

Following the **FIGURE 61**, the undervoltage for a $T_{rec1} = 7$ [ms] is ~-0.25 [p.u.]. Then, the converter standalone test is simulated applying this voltage drop. A recovery overvoltage of 1.2 p.u. is applied to stop the fault current, simulating the fault isolation. Once the current is stopped, the overvoltage is removed and only the nominal voltage is applied as presented in **FIGURE 142**b. The DC current measured at the converter terminals is presented in **FIGURE 142**a. It can be seen that the current can reach over 12 [kA]. The converter recovers to normal operating conditions after the simulated fault neutralization.



(a) (b)

FIGURE 142 DC current in (a) and voltage in (b) measured at the terminals of the converter during the standalone test for a converter with TB and DCR of 200 [mH].

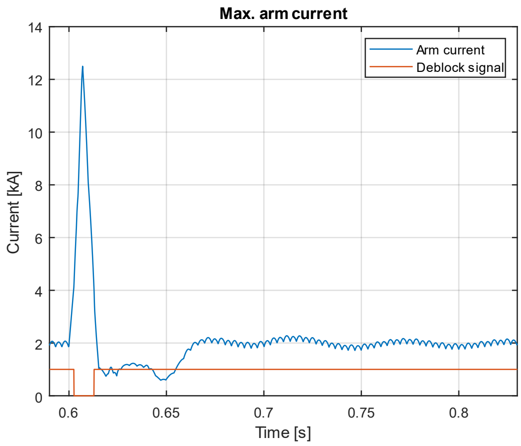
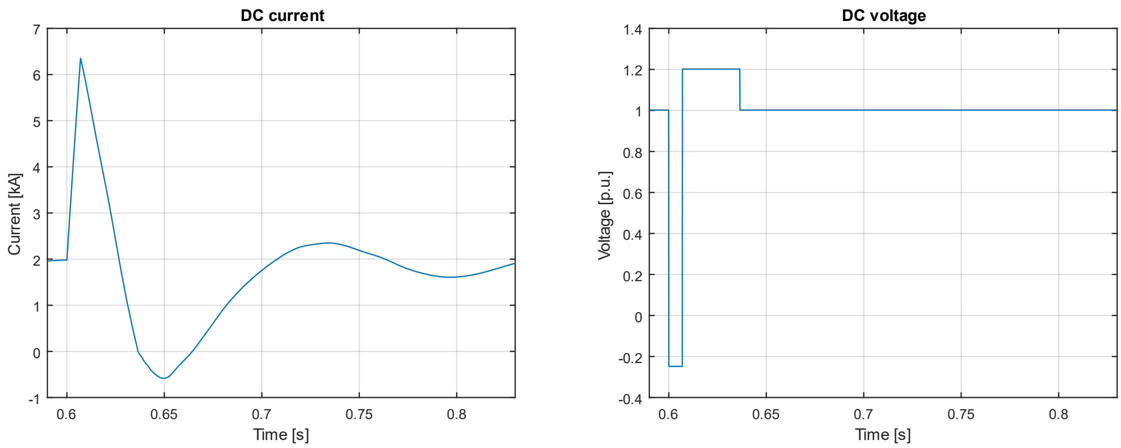


FIGURE 143 Maximum arm current, and deblocking signal, in the converter with TB during the standalone test.

The maximum arm current and the deblocking signal are presented in **FIGURE 143**. It can be noted that the converter blocks when the arm current reaches 4 [kA] and it deblocks again once the current is below this threshold. It is also noted that the arm current can reach over 12 [kA] which is deemed acceptable in the chosen example but cannot be generally assumed for converter solutions available today. This evidenced that the DCR sizing for a converter with TB functionality is linked to the capacity to withstand the fault current during T_{rec1}.

On the other hand, if the converter should provide continuous operation during a fault event, the converter supplier can increase the DCR size to withstand the overcurrent avoiding the converter blocking or disconnection.

Applying the same -0.25 [p.u.] voltage drop in the standalone test setup, now for a converter without TB, has led to the results presented in **FIGURE 144** and **FIGURE 145**. The results were obtained with a DCR of 980 [mH]. The DC side measurements are presented in **FIGURE 144**, while the internal arm current is presented in **FIGURE 145**. It can be noted that the arm current does not reach the protection threshold of 4 [kA], thus, it does not block.



(a) (b)

FIGURE 144 DC current in (a) and voltage in (b) measured at the terminals of the converter (without TB) during the standalone test. The converter station is considered with a DCR of 980 [mH].

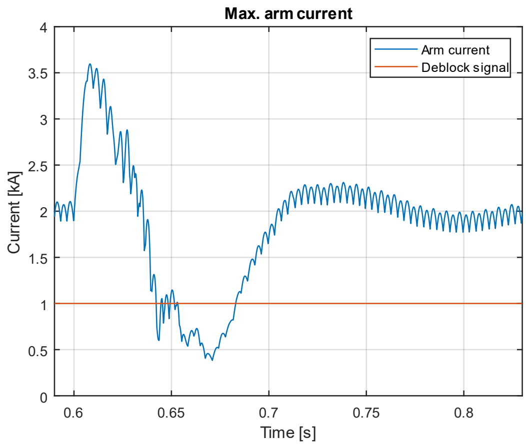


FIGURE 145 Maximum arm current in the converter (without TB) during the standalone test.

9.8.2.3 Switching unit/station design from standalone test

Similar to the converter design two DCSS designs with different neutralization times and the current breaking capabilities are considered.

Disclaimer: The values are used to illustrate how FSDs with different performances are compliant with the functional requirements, they do not intend to represent any vendor specific products.

- $T_N = 2$ [ms] and $I_{CBC} = 15$ [kA]
- $T_N = 5$ [ms] and $I_{CBC} = 30\ [kA]$

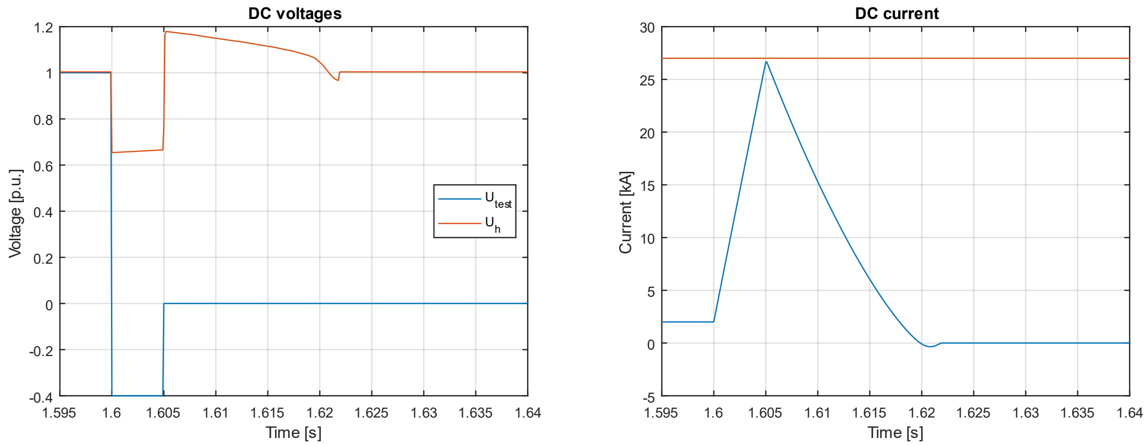
The switching stations must be compliant with the standalone test. For these sub-systems, the standalone test is presented in Section 7.4.3.

The test is used to size the DCR, of each SU, in order to respect the CBC. In this study, it is assumed that the complete switching station is provided by the same vendor (design of DCSS as presented in Section 7.4.3.2). Both DCSSs 1 and 5 are composed of four DCSUs therefore, the equivalent DCR for the healthy grid side is $L_{DC\ SU}/3$ (assuming that all inductances in the DCSS are equal).

Based on the proposed standalone test, the undervoltage for $T_N = 5$ [ms] is $U_{test} = -0.4$ [p.u.] (**FIGURE 67**), and the analytically calculated DCR is 110 [mH] (see **FIGURE 70**).The standalone test has been simulated and the results are presented in **FIGURE 146**.

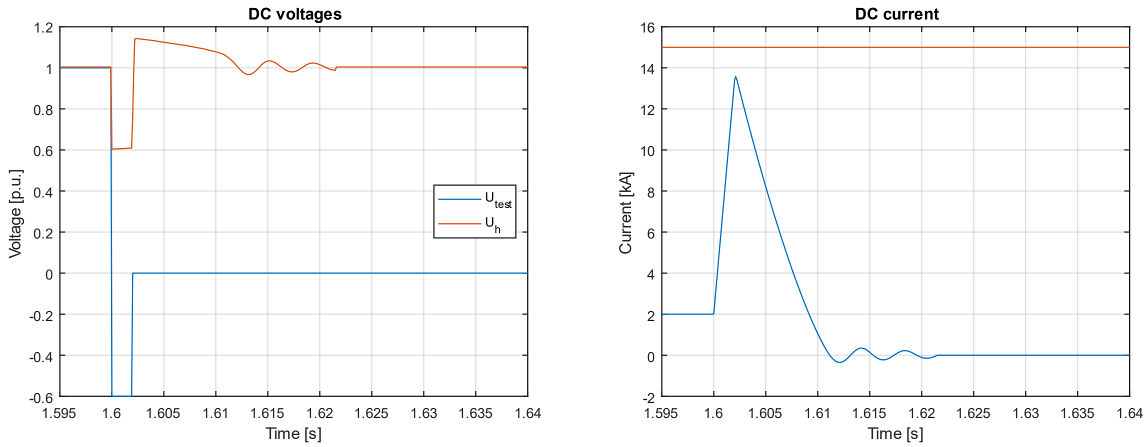
For the DCSS standalone test, the recovery overvoltage is applied by the DUT. It can be noted that U_{test} remains at 0 [p.u.] after T_N. The maximum fault current does not reach the CBC of the DCSU of 30 [kA].

Similar results are presented in **FIGURE 147** for the design with $T_N = 2$ [ms], with U_{test} dropping down to -0.6 [p.u.], validating the analytical sizing presented in **FIGURE 70**.



(a) (b)

FIGURE 146 Simulation cresults of the DCSS standalone test for a DCSU with a DCR of 110 [mH], $T_N = 5$ [ms] and $CBC = 30\ [kA]$. (a) DC voltages, (b) DC fault current.



(a) (b)

FIGURE 147 Simulation results of the DCSS standalone test for a DCSU with a DCR of 100 [mH], $T_N = 2$ [ms] and $CBC = 15$ [kA]. (a) DC voltages, (b) DC fault current.

In summary, the proposed designs are:

- $T_N = 2$ [ms] and $I_{CBC} = 15$ [kA] → $L_{DC\ SS} \approx 100$ [mH]
- $T_N = 5$ [ms] and $I_{CBC} = 30\ [kA]$ → $L_{DC\ SS} \approx 110$ [mH]

The surge arrester energy sizing is out of scope for this compliance test. This could be tested in a different test. This sizing should be done in a more detailed study.

9.8.3 Key performance indicators

The key performance indicators (KPIs) can be defined for each sub-system and the integrated grid to evaluate their behaviour in case of protection event e.g., DC faults.

- **AC side:** The impact of a DC fault on the AC grid (off- or onshore) can be evaluated based on existing AC FRT requirements such as the undervoltage limits and duration. The impact on the frequency and power can be also measured. Further AC grid requirements can be found in Appendix 9.1.

- **Switching station:** The switching station compliance can be verified by measuring the effective fault neutralization time, if the DC fault current is respecting the maximum current breaking capability and measuring the fault current suppression time.
- **Converter station:** On the converter station the verification is based on the capability of the converter to ride through the DC faults, but also measuring the maximal arm current and information about the blocking events.
- **System level:** In general, if the subsystems have respected the functional requirements, the system should be compliant with the protection design. However, additional verification can be done. The verification of the DC-FRT at each PoC in all ranges (transient, semi-transient, dynamic and static) can be used to obtain detail information about the system.

9.8.4 System level verification and simulation results

In this stage the subsystems are implemented in a simulation model to test their interactions. The results are evaluated based on the predefined KPIs (see Section 9.8.3).

- **Simulation cases:** to test the interactions between the proposed sub-system designs, 4 main cases are proposed.
- **Case 1:** all converter stations in temporary stop
- **Case 2:** all converter stations in continuous operation
- **Case 3:** offshore converter stations in continuous operation and onshore converter stations in temporary stop
- **Case 4:** offshore converter stations in temporary stop and onshore converter stations in continuous operation

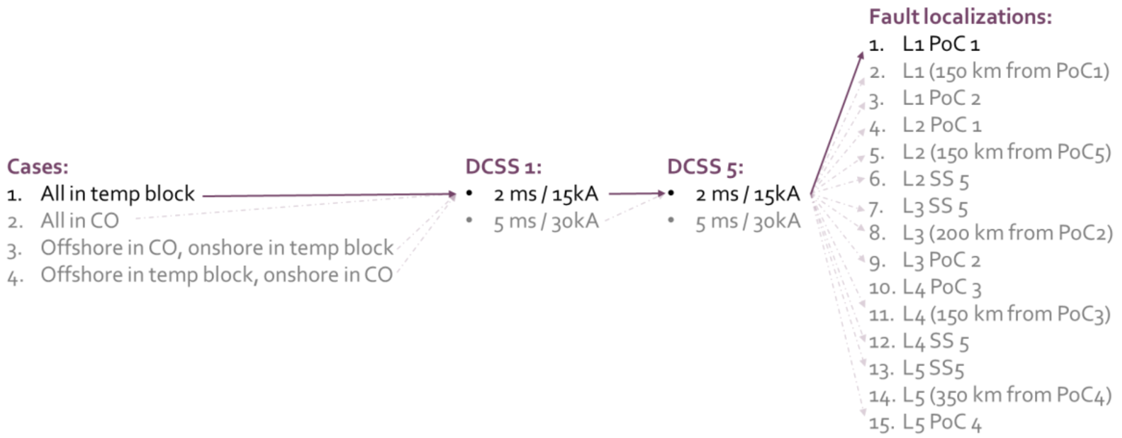


FIGURE 148 .Four levels of design variations: converters (cases), two DCSSs, and fault location. A total of 240 simulations cases have been run.

For each of the cases the design of the switching stations 1 and 5 (DCSSs with CBC, see **FIGURE 148**) are changed along with the fault localization.

The simulations consider pole (positive)-to-ground faults as they are defined as one of the ordinary contingencies in [17].The faults are located at the extremities of the cables (each PoC – 10 locations) and along the cable (not exactly in the middle – 5 locations). A solid fault is considered.

The following subsections present the aggregated simulation results, to check the tendencies. To simplify the representations, the results related to converters permanently blocked are ignored. For instance, the results on converter 2 (pole positive) are not presented when a fault is inside its protection zone (e.g., fault on line 1 or 3).

The detailed results of a simulation example are presented in Appendix 9.8.5.

9.8.4.1 Offshore AC system verification

The first KPI to check is the system compliance with AC grid requirements, especially the offshore AC-FRT. The simulation results were compared to the German AC-FRT [42, 43] and presented in **FIGURE 149**. It can be noticed that even when the converters block temporally, the AC voltage drop can be recovered under 150 [ms] to regain stability. As previously mentioned, the windfarm models are simplified and do not consider the islanded mode operation functions (see Section 9.8.2.1), nor protection actions. However, the obtained transients do not reach, or approach, the AC-FRT limits maintaining the PPMs in normal operating mode. It can be also highlighted that even without advanced control strategies (either on the windfarms nor the converter stations) the AC systems can recover steady-state conditions. Further analysis, with a more detailed windfarm model, can be found in Section 9.9.

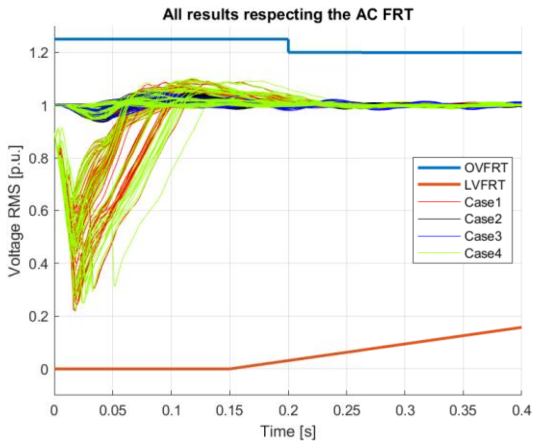


FIGURE 149 AC voltage at the offshore stations for all simulations performed. None of the events have violated the AC-FRT.

The active power of all offshore converter stations is presented in **FIGURE 150**. The power tends to recover steady state conditions after the fault event, similar to previous results.

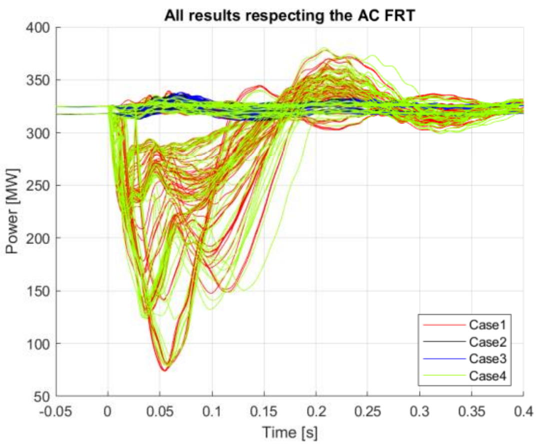


FIGURE 150 Active power of all offshore converter stations, for all simulations performed.

9.8.4.2 Switching station verification

To validate the DCSUs designs, the maximum fault current is measured and presented in **FIGURE 151**. It can be noticed that the maximum fault current does not exceed the 30 [kA] (for the 5 [ms] design), nor the most restrictive design of 15 [kA] (for the 2 [ms] design). Additionally, changing the converter FRT strategy from CO to TB does not change the maximum overcurrent to break (e.g., comparing results from case 1 and 2). Reminding that these two cases have DCR on the converter station with a difference over 700 [mH], suggests that the converter station DCR size have a low impact on maximum DC fault current to break (for a given T_N). The results validate the choice of DCR in the DCSSs.

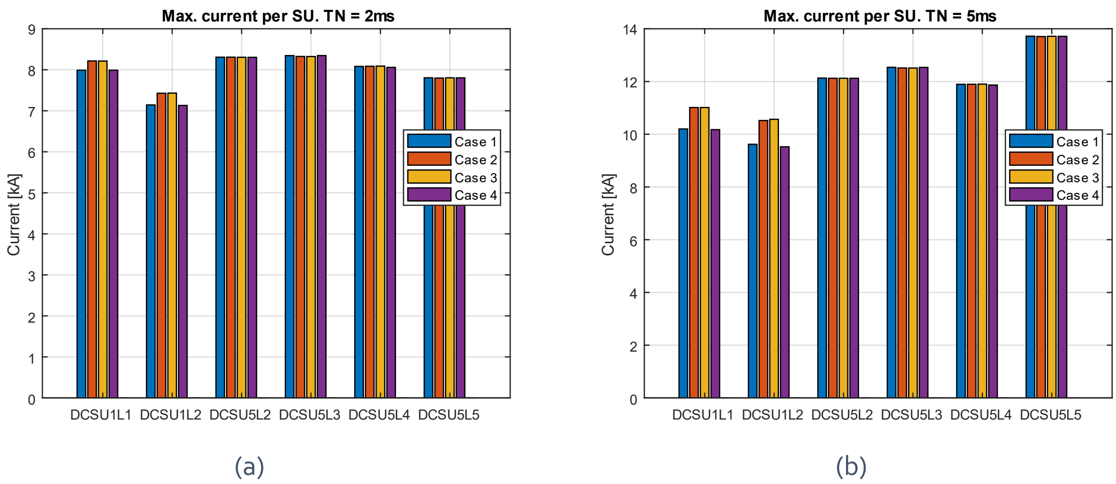
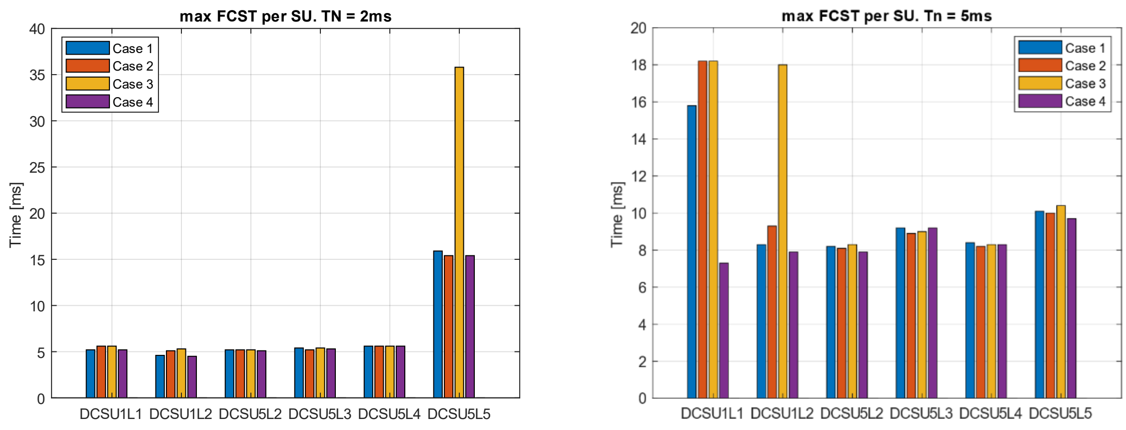


FIGURE 151 Maximum DC fault current measured for the DCSSs (a) with $T_N = 2$ [ms], (b) with $T_N = 5$ [ms], for all simulations performed.

The relatively low DC fault current could be interpreted as a possible oversize of DCRs, however, the DCSUs must be also sized for internal bus faults (not addressed in this study) that could be more restrictive. Further studies should be addressing the optimal selection of DCR for DCSSs.

The operation of the DCSS in a system, can be also evaluated by measuring the fault current suppression time (FCST - see definition in **FIGURE 48**). The FCST measured at each of the DCSU used in the study is presented in **FIGURE 152**. The maximum time registered do not exceed 37 [ms]. This FCST depends on the grid topology, the inductances considered and the selected TIV of the involved FCDs.



(a) (b)

FIGURE 152 Maximal fault current suppression time per DCSU and all cases.

9.8.4.3 Converter station verification

The DC voltages measured at the PoC are compared to the proposed DC-FRT and presented in **FIGURE 153**. The FRT is applied depending on the travelling wave arrival to each PoC. In general, the FRT requirement starts when the DC voltage at the PoC is below the static threshold U_{UV5}. From the results, it can be noted that most of the simulations respect the FRT. To better understand the cases violating the proposed FRT, the FRT is divided into 4 ranges: transient (between the travelling wave arrival and T_{rec1}), semi-transient (between T_{rec1} and T_{rec2}), dynamic (between T_{rec2} and T_{st}), and static (after T_{st}). The different ranges are presented in **FIGURE 154**.

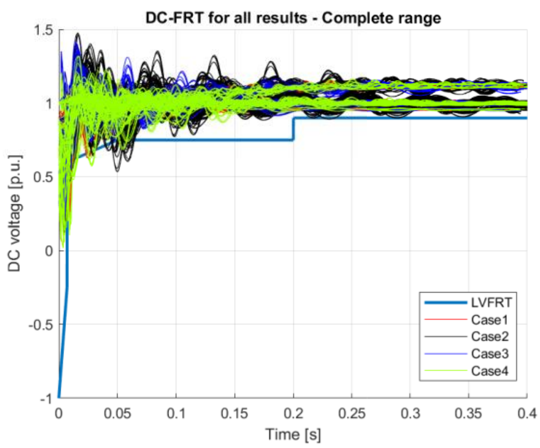


FIGURE 153 DC voltage at all PoCs of the system, compared to the proposed DC-FRT.

FIGURE 154a presents the transient region of the DC-FRT. During this range, the DC voltage is affected, mainly, by the fault location and cable parameters [26]. The results obtained do not reach the maximum undervoltage (-1 [p.u.] estimated in **FIGURE 56**) as the fault locations are not close enough to the PoC. The closest simulated fault is at 150 km, while the worst undervoltage is obtained for faults located at less than 50 km (see **FIGURE 56** and **FIGURE 59**a).

The semi-transient range is presented in **FIGURE 154**b. During this time the DC voltage is mainly affected by the DC network topology and some fast control actions. For this example, some of the fault scenarios violating the DC-FRT seem to be linked to network interactions, undamped oscillations, and slow DC voltage recovery for distant converters. Some of the results from case 2 continue to oscillate and violate the proposed FRT near the limit T_{rec2}. Detailed analyses have led to evidence that the most critical fault locations are on line 2 (due to network interactions) and line 4 (due to unexpected oscillations). Furthermore, the distant converters have a relatively slow voltage recovery, due to the travelling wave across the system.

The dynamic range is presented in **FIGURE 154**c. This range is affected by the control strategy of the converters connected to the grid. The few violations in this range are due to undamped oscillations already present in the semi-transient range. These violations can be avoided by an adequate control tuning (out of the scope of this example study).

The static range is presented in **FIGURE 154**d. Most of the simulations respect the proposed DC-FRT on this region. The few violations are caused by the undamped oscillations mentioned above. The voltage levels during the static region can be improved with appropriate droop repartitions.

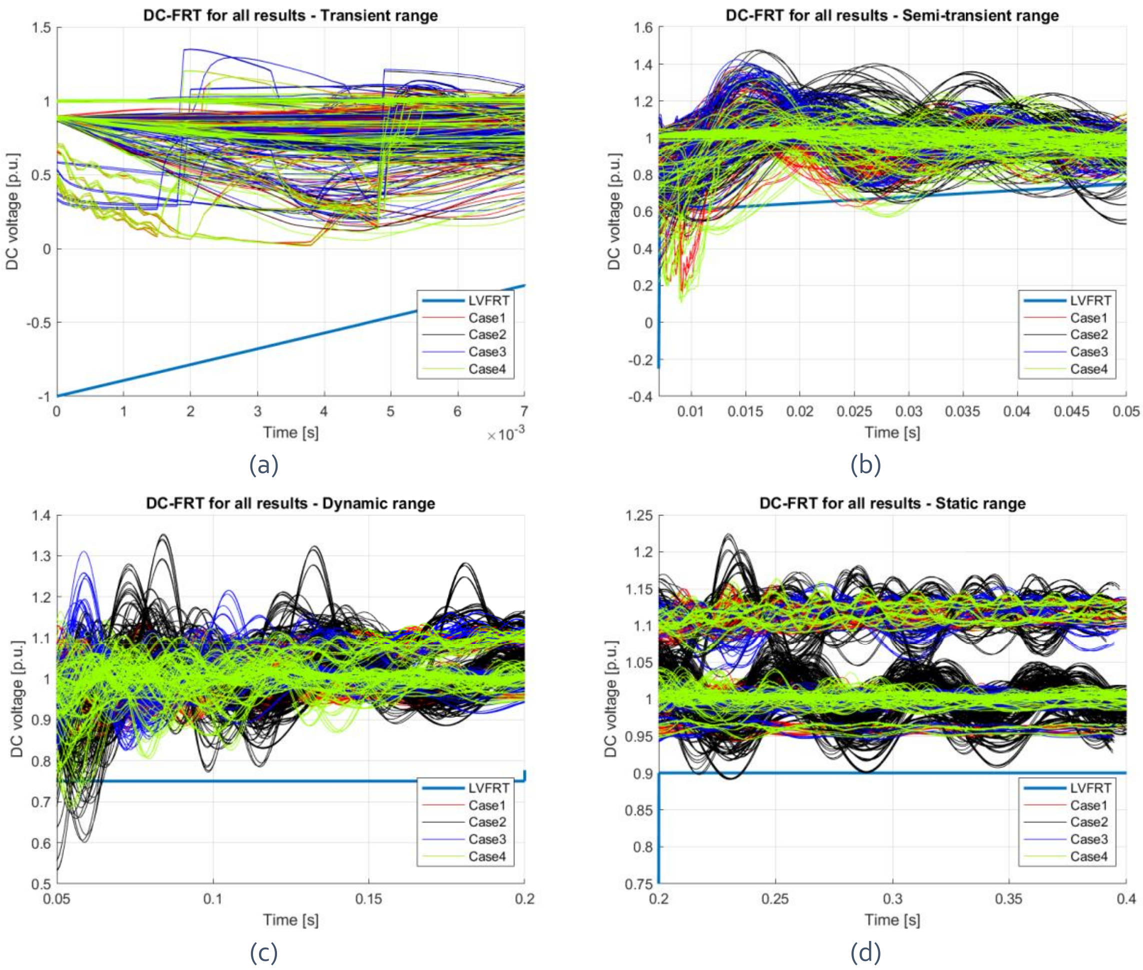


FIGURE 154 The different time ranges of the DC-FRT: (a) transient range, (b) semi-transient range, (c) dynamic range, and (d) static range.

The converter design can be evaluated checking how it behaves when operating connected to the studied system. **FIGURE 155** presents the maximum instantaneous arm current per converter station. In general, the current does not exceed the maximum threshold set at 4 [kA].

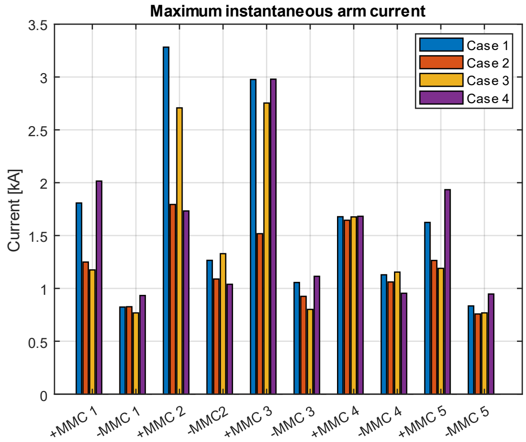
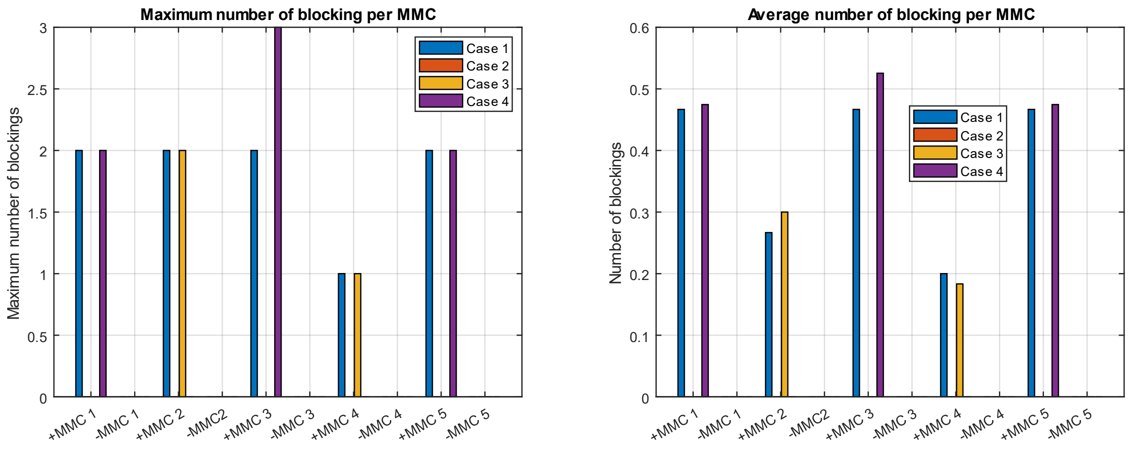


FIGURE 155 Maximal arm current in the converters for all cases and fault locations.



(a) (b)

FIGURE 156 (a) Maximal, and (b) average number blockings of each converter in a simulation, for all cases and fault locations.

The maximum number of consecutive blocking events within one simulation is presented in **FIGURE 156**a while the average number of blockings per simulation is presented in **FIGURE 156**b. It can be noticed that +MMC3 can be blocked 3 times in a single simulation but, in average, this converter does not block every simulation.

The multiple blocking capability can lead to extended requirements for the converter. Future studies can clarify the impact, adding additional criteria related to this point.

9.8.5 Detailed simulation results protection studies

Following the study presented in above, this section presents additional detailed results.

9.8.5.1 Time domain results, an example

This section presents the detailed, time domain, simulation results of one simulation case. The general simulation conditions are:

- **Converter case 1:** all converter stations with TB capability.
- **Neutralization time:** 5 [ms] for both DCSS1 and DCSS5.
- **Fault localization:** positive pole to ground fault at one of the terminals of line 2 next to the PoC 1,5. Converter stations 1 and 5 are connected to the same bus through DCSS1.

The simulation starts with an initialization of the system and at 1.1 [s] the fault event is simulated. The total simulation time is 1.5 [s]. Most of the figures show the initial time domain, only the FRT figures modify the time scale to take into account the beginning of an undervoltage event (t=0 [s]).

9.8.5.2 Offshore AC measurements

The AC RMS voltage measured at the WFs are presented in **FIGURE 157**. It can be noticed that the AC voltage does not violate the AC-FRT requirements and only the affected WFs (1, 3, 5) diverge from the nominal voltage of 66 [kV]. However, this measure alone is not conclusive. It cannot tell if the WF is disconnected or not, because the model used do not consider the protections strategies (see Section 0). Thus, additional measurements are presented.

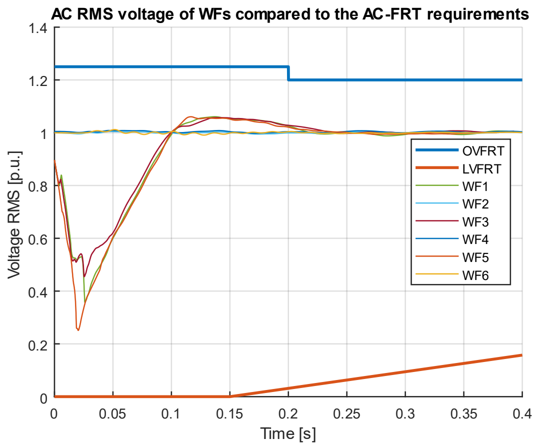


FIGURE 157 AC RMS voltage measured at the terminals of the WFs, compared to the AC-FRT requirements.

FIGURE 157 presented the AC RMS voltage, to check more in detail the impact of the DC fault on the AC networks, the instantaneous AC voltages are presented in **FIGURE 158**. It can be noted that the affected WFs (**FIGURE 158**a,c,e) have a reset of the AC voltage due to the blocking of the adjacent converters in grid forming control (see **FIGURE 135**). This behaviour increases the transient time. To reduce this transient time, different control during and after the converter blocking can be adopted (see Section 9.9).

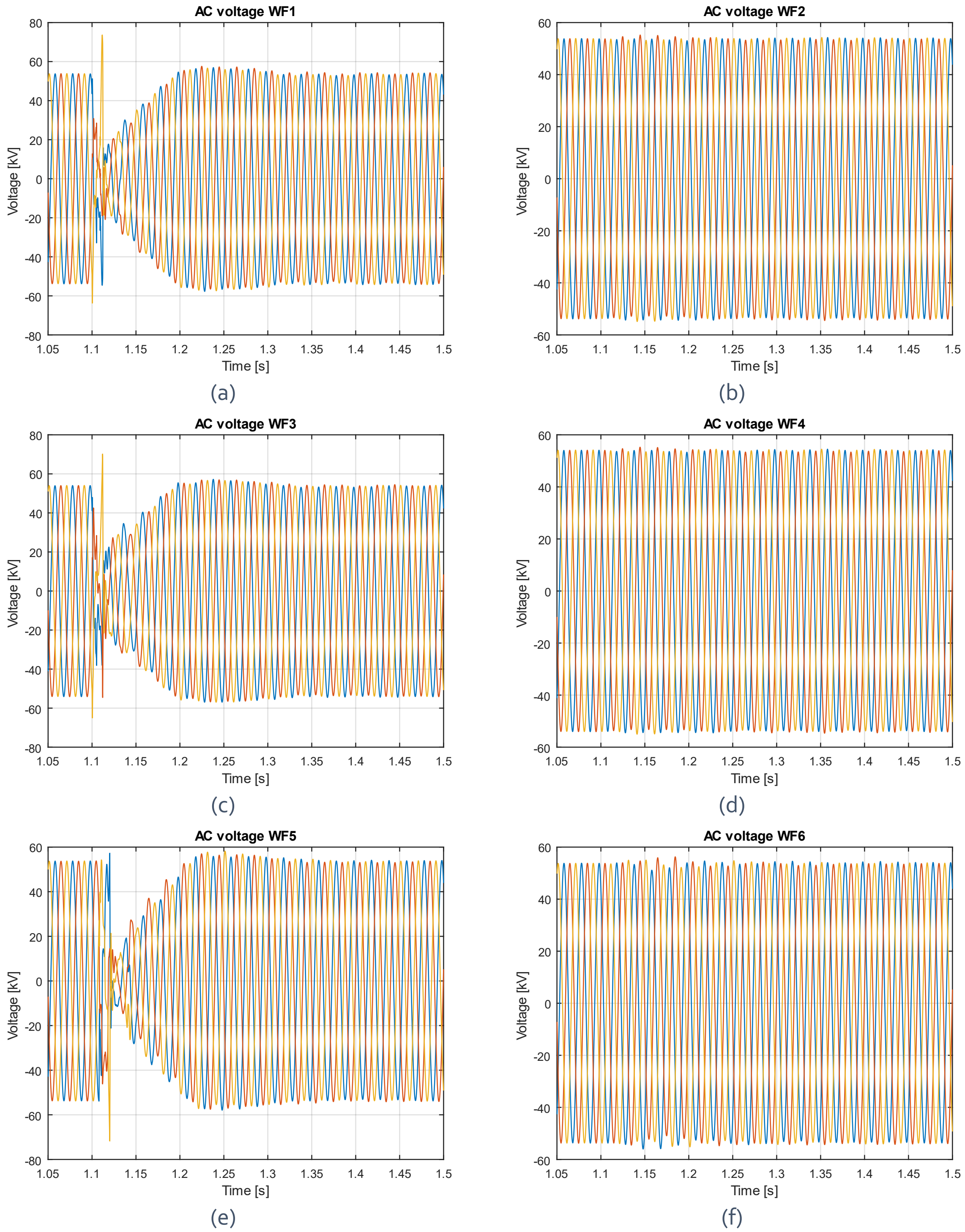
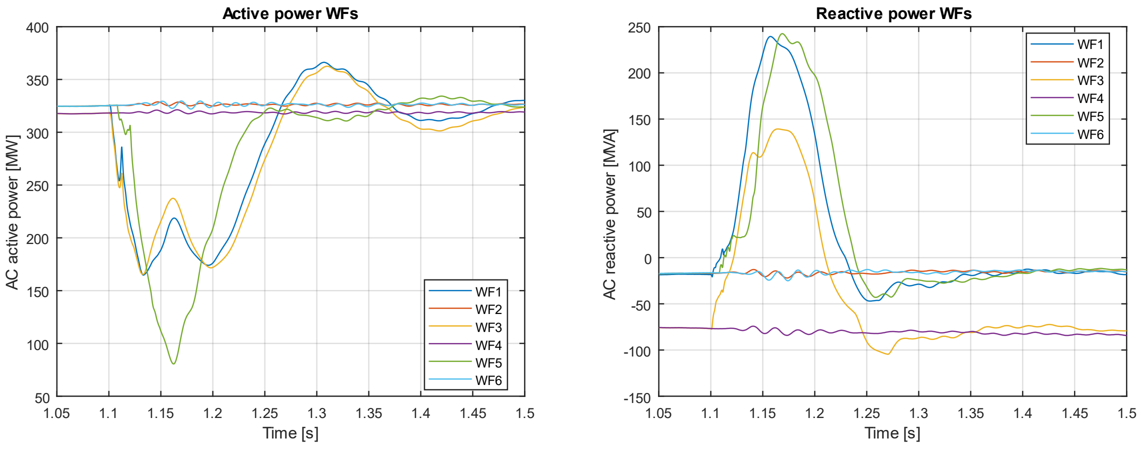


FIGURE 158 Instantaneous AC voltage per WF.

The active and reactive power exchanged by the WFs are presented in **FIGURE 159**a, and **FIGURE 159**b respectively. In general, the WFs are able to recover stability and tend to recover pre-fault conditions. WFs 3 and 4 show a difference in active, and specially for the reactive power exchanged. This is mainly due to the different length of the AC cable (10 [km] instead of 5 [km]) considered for the converter station 5 as presented in **FIGURE 135**.



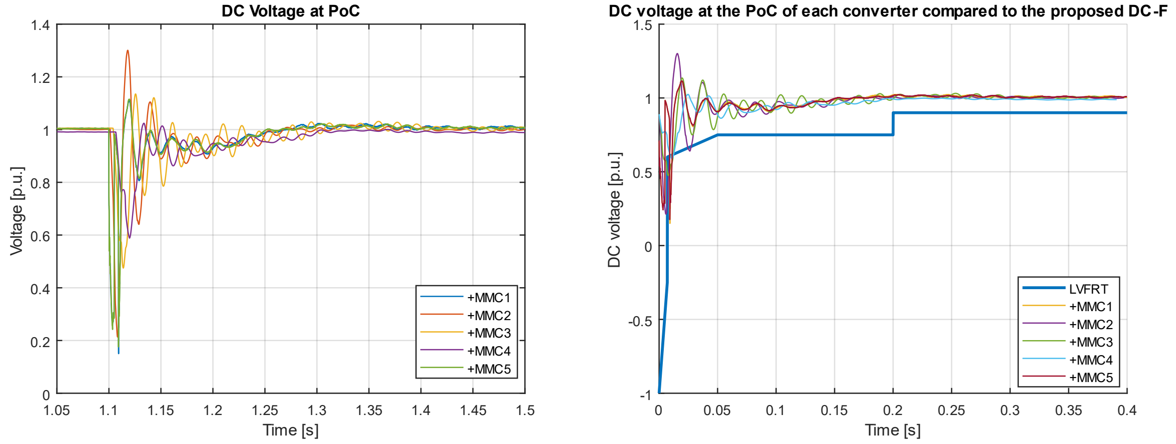
(a) (b)

FIGURE 159 (a) Active and (b) reactive power per WF.

9.8.5.3 Converter station measurements

The converter station figures are limited to the converters connected to the positive (faulted) pole. The DC voltage measured at the PoC are presented in **FIGURE 160**a, and compared to the DC-FRT in **FIGURE 160**b. It can be evidenced that the DC voltage have violated the proposed DC-FRT. A zoom into the different regions of the DC-FRT is presented in **FIGURE 161**.

FIGURE 161b shows that the voltages in the semi-transient regions take more time to recover than DC-FRT curve. The proposed DC-FRT is too restrictive for these transients. As the system recover stability after the fault, the parameters affecting the semi-transient region of the DC-FRT can be adjusted to avoid unnecessary converter disconnections.



(a) (b)

FIGURE 160 DC voltages (a) measured at the PoCs and, (b) compared to the DC-FRT proposed.

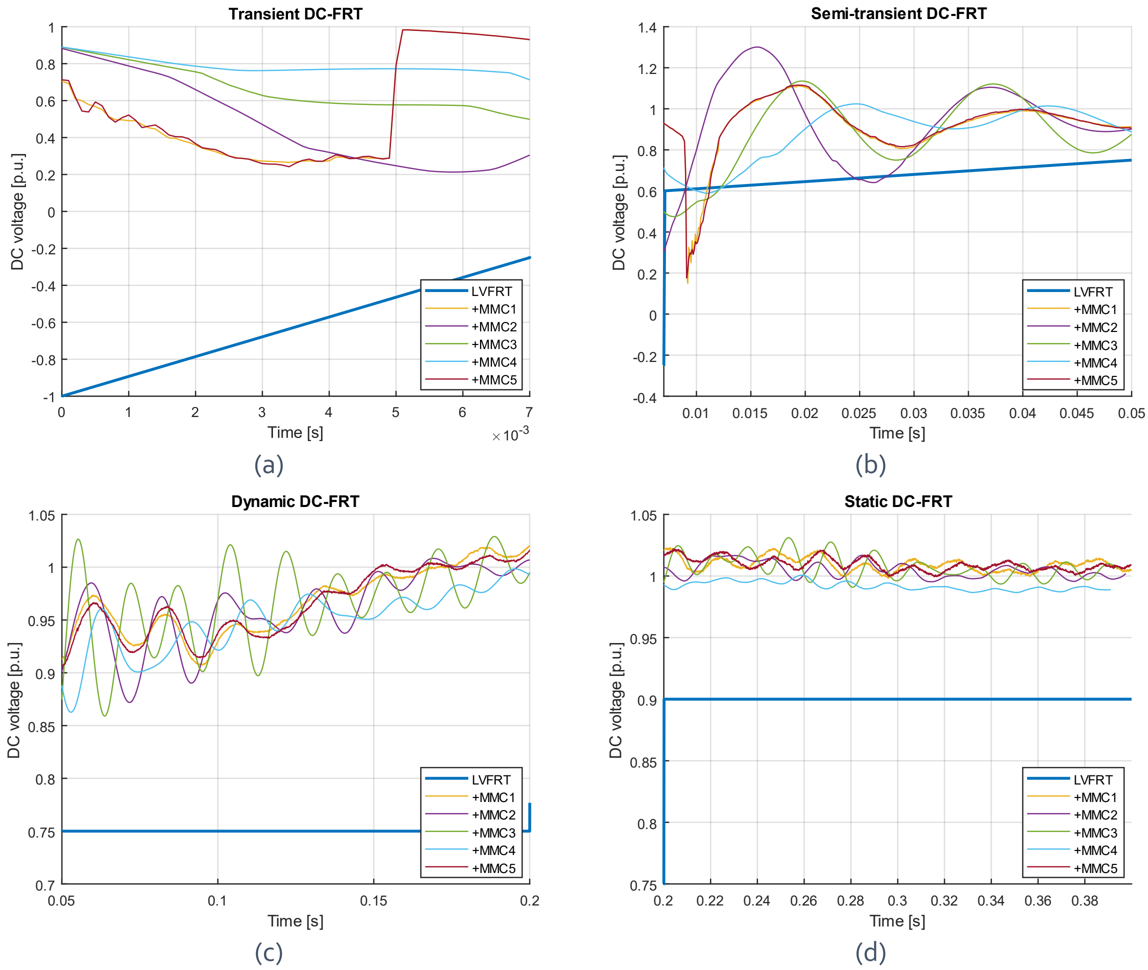


FIGURE 161 Different regions of the DC-FRT. (a) transient, (b) semi-transient, (c) dynamic, and (d) static region.

FIGURE 162 presents the DC voltages measured at the PoC of all converters compared to the adjusted DC-FRT curve, proposed in Section 9.8.6 ($U_{UV3} = 0$ [p.u.]).

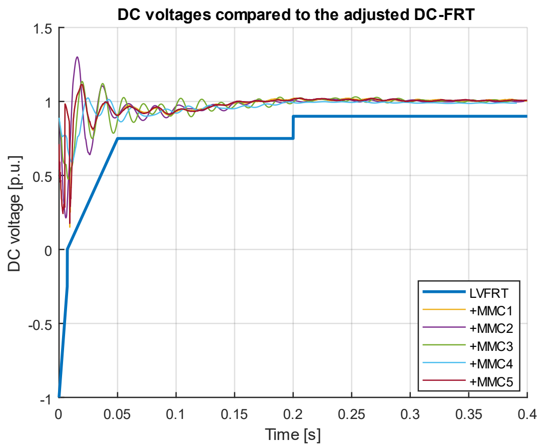
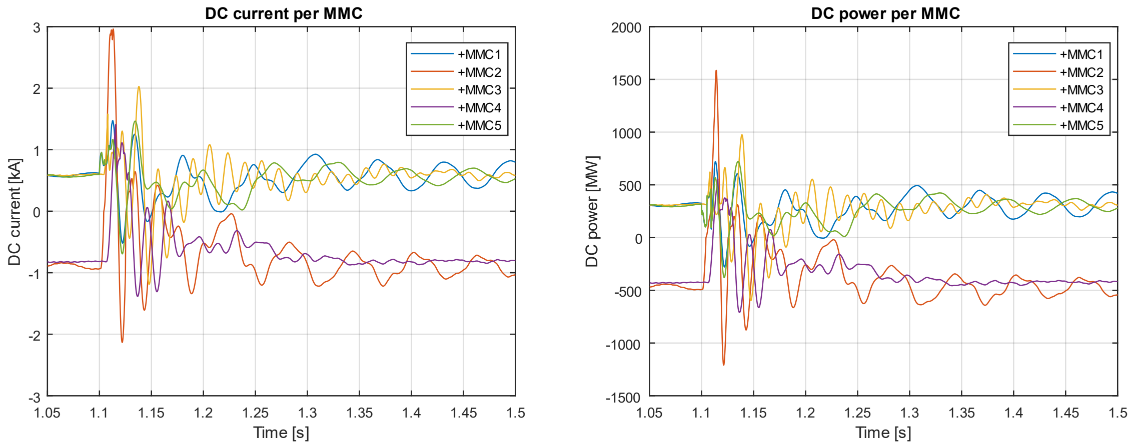


FIGURE 162 DC voltages compared to the adjusted DC-FRT curve.

The DC current and power per MMC are presented in **FIGURE 163**a, and **FIGURE 163**b respectively.



(a) (b)

FIGURE 163 Measurements at the converters connected to the positive pole. (a) DC current, (b) DC power.

The maximum arm current is presented in **FIGURE 164**. It shows that the maximum current measured is 3 [kA], which is the below the overcurrent limit of 4 [kA]. However, as presented in **FIGURE 165**, the converters have blocked multiple times. This is because the converters are also blocked by undervoltage measured at the PoC (see Section 0). This blocking condition is only used in this example to test the proposed DC-FRT definition.

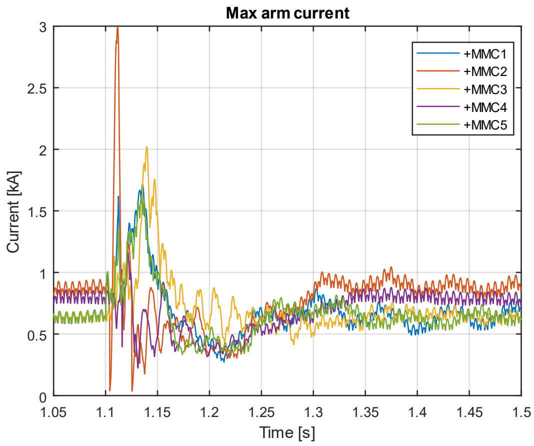


FIGURE 164 Measurements of the maximum instantaneous arm currents in the MMCs.

FIGURE 165 also shows that the converters can block multiple times during a fault event. Converters 1, 2, and 5 have blocked 2 times. Despite these multiple blocking events they all recover stability and remain deblocked until the end of the simulation. Another interesting result is that at 1.11 [s] there are 4 converters simultaneously blocked, including MMC2 in V_{DC} droop control. It suggests that fast simultaneous blocking do not lead to instabilities. However, further studies must be carried out to determine the limitations of simultaneous blocking as it depends on the converter controls, system topology, cable lengths, etc.

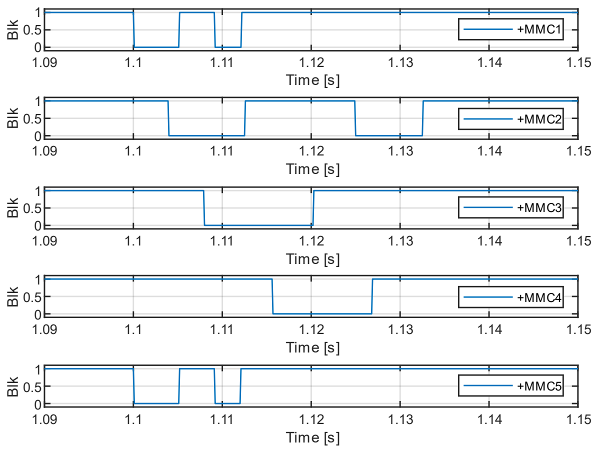


FIGURE 165 Blocking signals per converter. MMC1,3,5 are in grid forming control, and MMC2,4 in V_{DC} droop control.

9.8.5.4 DCSS measurements

To check the behaviour of the DCSSs the DC current is presented in **FIGURE 166**. It can be noticed that the maximum current measured is below the CBC of the DCSU, i.e. 30 [kA]. It can also be noticed that the TIV application is after 5 [ms] of the front arrival. For the DCSU1 L2 the fault is at its terminals so there is no delay between the fault and the travelling wave arrival. On the other hand, the DCSU5 L2 has a delay due to the distance. Both DCSUs operated correctly.

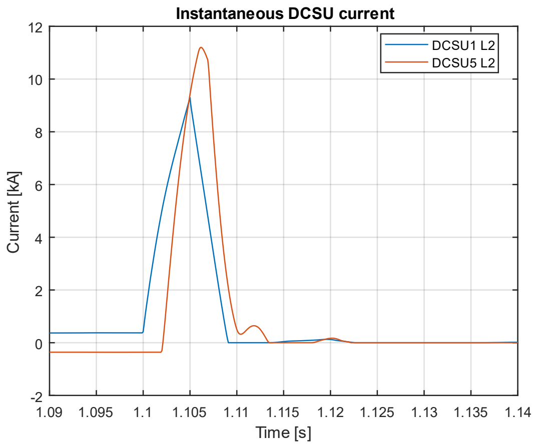


FIGURE 166 DC current at the DCSSs adjacent to the fault.

9.8.6 Conclusions

As proposed in Section 9.8.3, the system verification can validate the sub-system designs individually and their interactions. From the results analysed above it can be concluded that most of design combinations have respected the system requirements. However, a few points should be highlighted:

- **Standalone test:** The proposed methodology, including the definition of the standalone test for the subsystems have led to satisfactory results on the system level integration. The subsystems designs are compliant with the operational limitations stablished for the standalone test. For instance, the converter stations remain in CO during the fault events and the maximum DC fault current opened by the FDS are not higher than the predefined level. Furthermore, based on the different mix between converter and DCSS designs, the subsystem designs have shown interoperability.

- **Converter stations with or without temporary blocking (TB):** this preliminary study has evidenced that the TB functionality could be beneficial for the HVDC systems showing an acceptable impact on both the DC grid and the adjacent AC grids. As presented above, a converter station with TB can significatively reduce the DCR size. Further analysis show that the TB functionality can also reduce the average DC voltage and DC power recovery times as presented in **FIGURE 167**a,b, where the case 1 is all converters with TB functionality and case 2 all in CO.
- Furthermore, **FIGURE 168** presents the cumulative maximum blocking time of converters for all cases and fault locations (removing the results where the converter is disconnected e.g., disconnection of converter station 2 for a fault in line 1 or 3). It can be noticed that the blocking time of converters does not exceed 18 [ms], making TB functionality a fast action.
- From the results obtained, there is no suggestion that the TB will affect negatively the AC offshore grid. The results do not show instability issues, and all transients respect the AC-FRT requirements (voltage measurements). Further results can be observed in Section 9.9. However, further studies must be conducted to validate these conclusions (e.g., considering more realistic WF models). Moreover, the impact of TB on the converter design is not clear. Adapting the control and sizing the equipment can be subject to additional functional requirements (e.g., number of consecutive blockings that the converter should be capable to withstand).
- On the other hand, the solutions in CO have evidenced possible control-related issues. The results obtained for case 2 have presented undamped oscillations that increase the time to recover normal operating conditions (see **FIGURE 169**). The relation between the protection and control requirements should be study in future studies.

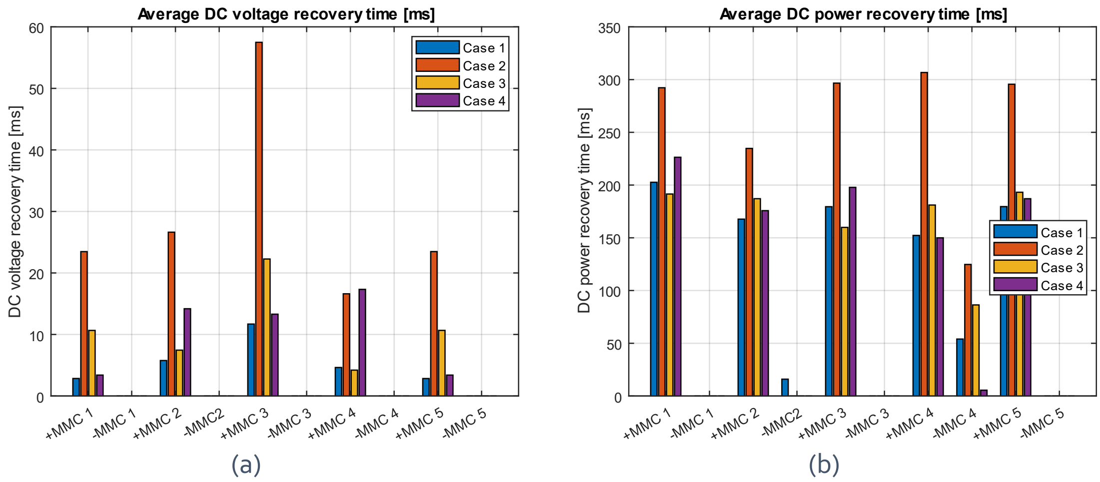


FIGURE 167 Comparison between cases of the average recovery times for (a) DC voltage and (b) DC power.

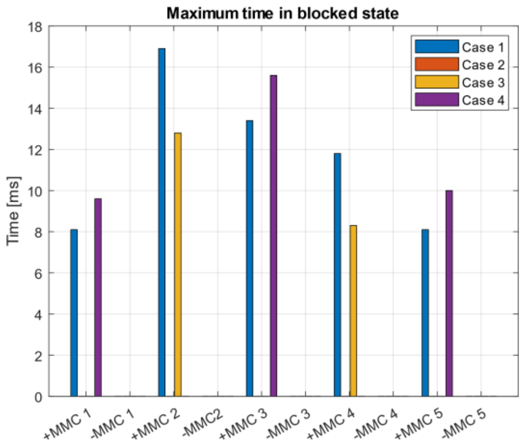
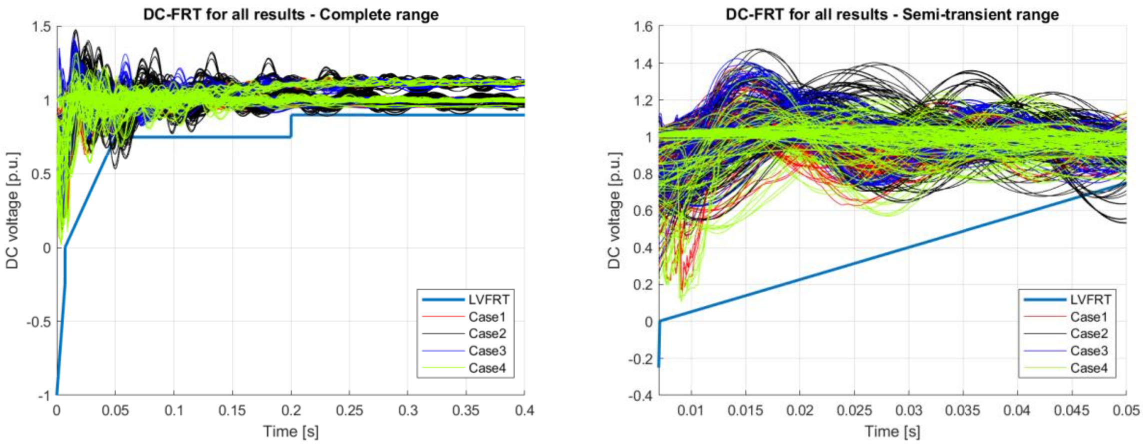


FIGURE 168 Maximum blocking time per converter, for all cases and fault locations.

- **DC-FRT profile:** The proposed FRT was tested, and it is in accordance with most of the transients obtained. The voltage measurements did not exceed any of the prescribed ranges in the transient part of the profile. However, during the semi-transient region the parameters could be changed to relax the restrictions. Additional studies can be carried out to verify the impact of the control strategies on the dynamic region of the DC-FRT.
- It is worth to note that the FRT definition should agree with the control requirements presented in Chapter 6. The dynamic and static bands should be coordinated between the protection and control standalone test (as suggested in **TABLE 42**).
- **New U_{UV3}:** based on the results the modification of the undervoltage threshold U_{UV3} to 0 [p.u.] can relax the restrictions on the semi-transient region. **FIGURE 169** presents the new DC-FRT compared to all voltage transients. It can be noted that most of the transients comply with the newly defined semi-transient region (**FIGURE 169**b). There are still violations at the interface with the dynamic region due to undamped oscillations, essentially for case 2 which might be due to the increased size of DC reactors compared to the other cases. Note that optimisation of control dynamics was not in the scope of this study and further investigations may be required. The new proposal is also presented in **FIGURE 162** for the detailed example of Appendix 9.8.5.



(a) (b)

FIGURE 169 Voltage transients of all simulations compared to the new DC-FRT curve with $U_{UV3} = 0$ [p.u.]. (a) the complete DC-FRT range, (b) semi-transient range.

- **Modelling:** the models used are generic and simplified. Further studies can confirm the results considering more detailed models including line surge arresters, different grounding strategies, more detailed DCSS model, etc.
- **Control tuning:** one of the principal inconveniences found on this work is the lack of adequate control tunning strategy leading to undamped oscillations. As this work focused on the protection strategy other control related KPIs were neglected.
- **Topology-dependent problems:** the preliminary studies done to determine the standalone test have neglected the topology-dependent problems. For this example, the results suggest that the grid is sensible to pole-to-ground faults in line 2. Note that this study did not consider reduced configurations (i.e. due to system split or maintenance of components). Such reduced configurations could lead to more severe voltage transients which could be investigated in further studies. Additional investigations should also confirm the interactions between the grid topology, the control tuning and the observed undamped oscillations.

9.9 Temporary blocking offshore

Disclaimer: This study focusses on state-of-the art control solutions: Offshore converter in V/f control and DC connected PPMs in GFL control. From there, additional control functions for islanded operation are investigated. It should be noted that other control schemes for PPMs such as GFM are other means to achieve enhanced DC-FRT during temporary blocking of the offshore converter. Some TSOs see additional beneficial services such as instantaneous reserves which could be provided by PPMs in GFM. This is already requested in current grid code specifications of several TSOs.

The DC-FRT requirements described in section 7.3 allow temporary blocking in order to ensure an inclusive design of both converters and FSDs while reducing the size of DC reactors which might improve the overall controllability (see also section 6.5). With regards to converters connected to an offshore grid consisting of DC connected PPMs, the converter is likely to be in V/f control mode. When temporary blocking of an offshore converter occurs, the voltage and frequency reference of the PPMs is temporarily lost, PPMs are temporarily in islanded operation. The objective of this section is to investigate if the DC-FRT specifications, and in particular if the temporary blocking of a converter is compliant with existing AC grid specifications for PPMs. The sequence will be decomposed and the impact of each event for the AC offshore grid will be analysed step-by-step as shown in **FIGURE 170**. The additional functions required for the DC-FRT of the PPM will also be presented in this section in **FIGURE 171**.

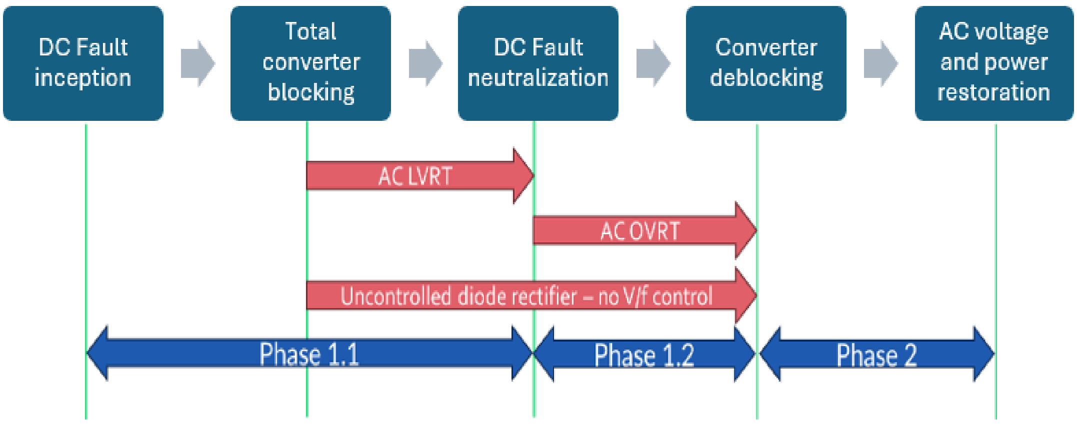


FIGURE 170 Sequence of temporary blocking on the AC offshore side

For the AC grid, the initial DC fault is not immediately observed, as the fault current is initially provided by the submodule capacitors of the converter and due to the fact that DC faults are likely to be cleared much faster than AC faults. According to the DC-FRT profile, the converter may block which leads to a drop of AC voltage. This constitutes what has been referred to as phase 1.1 in **FIGURE 170**. By respecting the LVRT profile defined in [44], the PPM are required to remain connected during DC fault clearing. This phase does not require additional functions compared to classic LVRT protection and results confirming this can be found in section 9.9.2.3.

After fault neutralization the DC voltage is restored. For the AC grid, this means that the offshore converter which behaves as a diode rectifier, becomes non passing as, the DC voltage is much higher than the AC voltage. However, the PPM keeps feeding constant power. As none of the power produced is evacuated, the control action of GFL turbines will cause the voltage and frequency to increase until either a physical modulation limit of the PPM is reached, or the voltage is high enough to make the converter passing and the produced power to be evacuated again. This is referred to as phase 1.2 in **FIGURE 170**. In order to prevent any undesired disconnection due to OVRT violation, protection functions shall ensure the ability of the PPMs to operate in islanded mode. Results obtained in 9.9.2 show how integrated functions limit the voltage magnitude, and the frequency deviation to simplify the resynchronization of the deblocked offshore converter.

Finally, the offshore converter deblocks and resynchronizes, initiating phase 2 where the offshore converter takes over the control of the AC offshore voltage and frequency. Results obtained in 9.9.2.3 show that a resynchronization function for the converter are recommended to prevent a phase jump between the converter and PPMs in islanded mode operation. The strategy for the transition from islanded mode to GFL mode might require to reset the control and the active power restoration.

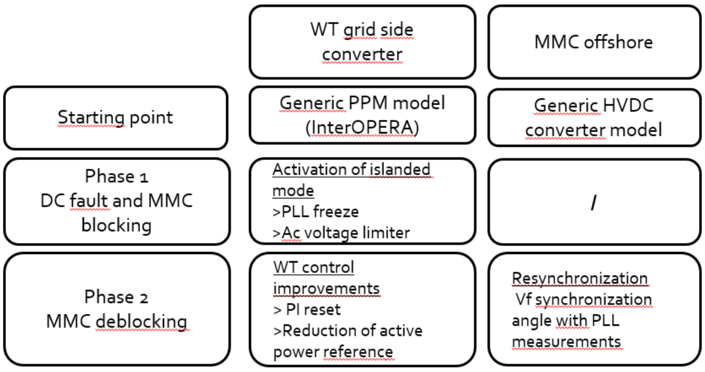


FIGURE 171 Functionality of AC grid converters with temporary blocking functionality and PPMs in islanded mode operation

First, the overall sequence from DC fault inception to full restoration will be presented. Secondly, challenges and solutions will be presented for both the islanded mode operation during converter blocking and the resynchronization after deblocking. The performance of such solutions will be evaluated based on EMT simulations. Finally, conclusions and recommendations will be drawn.

9.9.1 Model description and modelling hypothesis

9.9.1.1 Topology

The topology of this investigation considers PPMs in decoupled operation connected to a multi terminal DC grid. The focus of this paper is the ability of the PPM to stay connected to the offshore grid despite a temporary blocking of the offshore converter and the ability of the converter to reconnect to the AC grid after blocking. Therefore, the DC grid will be simplified as much as possible while maintaining realistic behavior in voltage. The topology used throughout this section is shown in **FIGURE 172**.

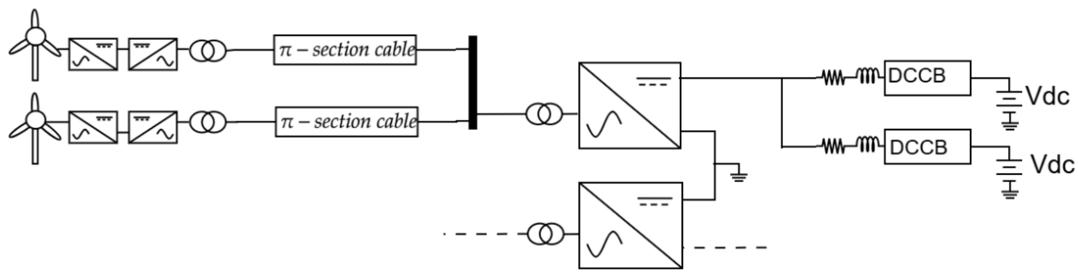


FIGURE 172 Topology of the offshore and DC grid

- The two wind turbines (WT) are aggregated models, each representing a PPM. The wind turbines are considered to be type IV -Permanent Magnet Synchronous Generator (PMSG) [45] models and as such need to be connected through back-to-back full-scale converter (FSC) to the AC grid. For simplification and due to their absence of synchronization with the offshore grid, the WT and machine side converter (MSC) are replaced by a controlled current source and constant power reference as the mechanical dynamics available directly at the WT level and MSC are way slower than the electric transients considered in this study. [46]
- Each grid side converter (GSC) is connected to the AC offshore grid where both transformers of the PPMs and the offshore converter are represented. The cable array is modelled as a π-section.
- The offshore converter is considered part of a bipole although only the positive pole will be considered in this study.
- The DC grid is composed of two parallel feeders represented by ideal DC sources via a DCCB and a DCR. One feeder will face a DC fault while the other one will provide a path for power exportation after DC voltage recovery.

9.9.1.2 Control structure

The system control strategy shown in **FIGURE 173** illustrates the topology considered for this study. The current PPMs using HVDC connection currently relies on a control strategy similar, at least in general concept, to the one presented in this section:

PPMs are in GFL and the offshore converter is in V/f mode to provide the reference of voltage and magnitude for the PPMs. The system modelled in EMT software to obtain the hereafter presented results only include converters models for the GSC and the offshore converter.

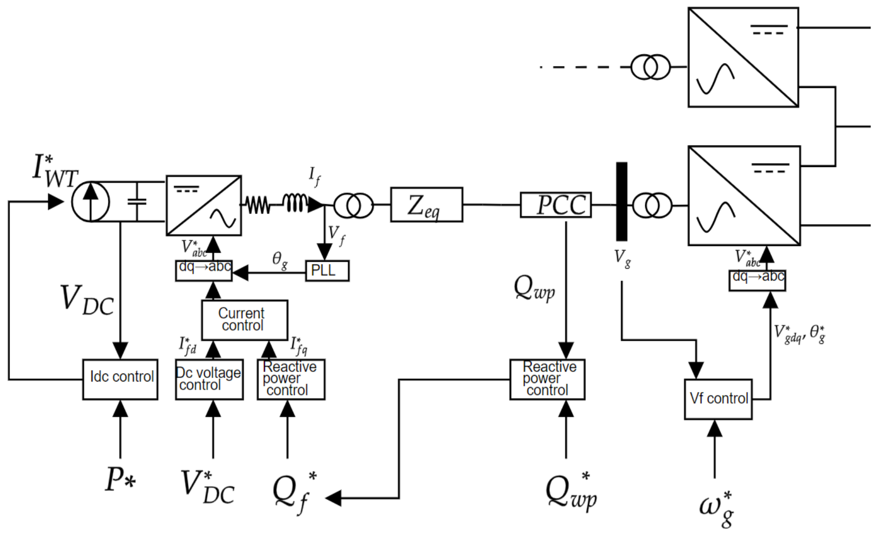
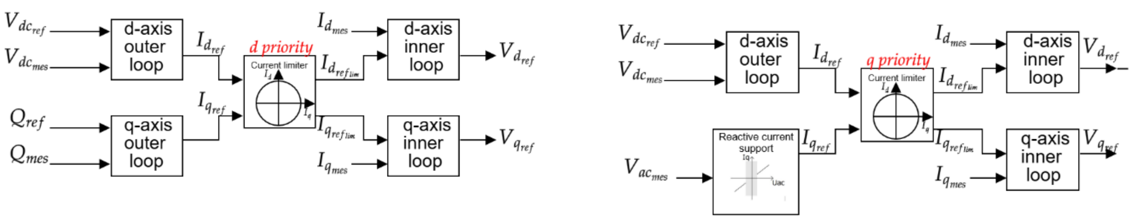


FIGURE 173 Overall offshore grid topology, references and measurements of PPMs and offshore converters

The GSC is in GFL. In normal operation priority is given to active power. The FRT-control mode is activated when the measured AC voltage exceeds a band of more than 10% compared to the nominal value. The GFL GSC regulates Vdc in regular operation and Vac in FRT mode (**FIGURE 174**), while always respecting its own limitation in current and voltage modulation. The regular and FRT control of the WT is presented in **FIGURE 174** (a) and (b) respectively.



(a) (b)

FIGURE 174 Control of the WT:(a) in regular operation, (b) in FRT mode

9.9.1.3 PPM and offshore converter protection functions

The wind turbine is equipped with four different protections:

- A DC chopper in charge of limiting the voltage of the back-to-back link under 1.07 pu.
- An overcurrent protection that trips the OWF if the current at the WT exceeds 1.1 pu despite the current limiter present in the control
- An overvoltage/undervoltage protection which compares the voltage to a predetermined voltage profile
- A rate of change of frequency (ROCOF) protection which triggers when a maximum value of 2.5 Hz/s is exceeded

Among those protections, the last two will be disabled to observe the dynamics of the system.

According to the DC-FRT profile specifications, the offshore AC/DC converter could temporary block if the voltage at its DC-PoC exceeds dynamic voltage ranges (see section 7.3). Until DC voltage recovery the converter could stop switching and operate as a diode rectifier.

9.9.1.4 Simulation scenario

To study the temporary blocking, the sequence as shown in **TABLE 46** is applied.

TABLE 46 Simulation sequence for temporary blocking investigation

Time (s)	Event
0.5 to 0.9	WT power ramp up
1.2	DC fault on feeder 1
~1.208	Offshore convert blocking
1.210	DCCB opens, neutralizing fault
1.5	Converter is deblocked

In section 9.9.2, the last event will not be considered as the focus is the islanded operation. It should be noted that the deblocking and resynchronization is artificially delayed in order to investigate islanded mode operation and resynchronization as independent events. With regards to the DC-FRT the temporary blocking is significantly shorter limited to several tens of milliseconds (see **FIGURE 168**).

9.9.1.5 Simulation parameters

TABLE 47 Parameters of the study

Parameters of the wind turbine	
Total rating	495 MW
Number of WT	33
Generation per WT	15 MW
Generator nominal voltage	0.9 kVRMSLL
Grid nominal voltage	132 kVRMSLL
DC link nominal voltage	1 800 V
Frequency	50 Hz
Xtransfo	0.1 pu
Rtransfo	0.001 pu
Lfilter	0.05 pu
Rfilter	0.0015 pu
Parameters of the AC grid	
Resistance	0.056 Ohm/km
inductance	0.000369 H/km
Capacitor	0.000000196 F/km
Default distance	5 km
Voltage level at the WT	900 V RMS LL
Voltage level on the AC grid	132 kV RMS LL
Voltage level at the offshore converter	300 kV RMS LL
Parameters of the offshore converter	

Rating	1000 MVA
Voltage HVDC	525 kV
Xtransfo	0.15 pu
Rtransfo	0.001 pu
Xarm	0.15 pu
Capacitor energy in each submodule	40 kJ
Number of submodules	278

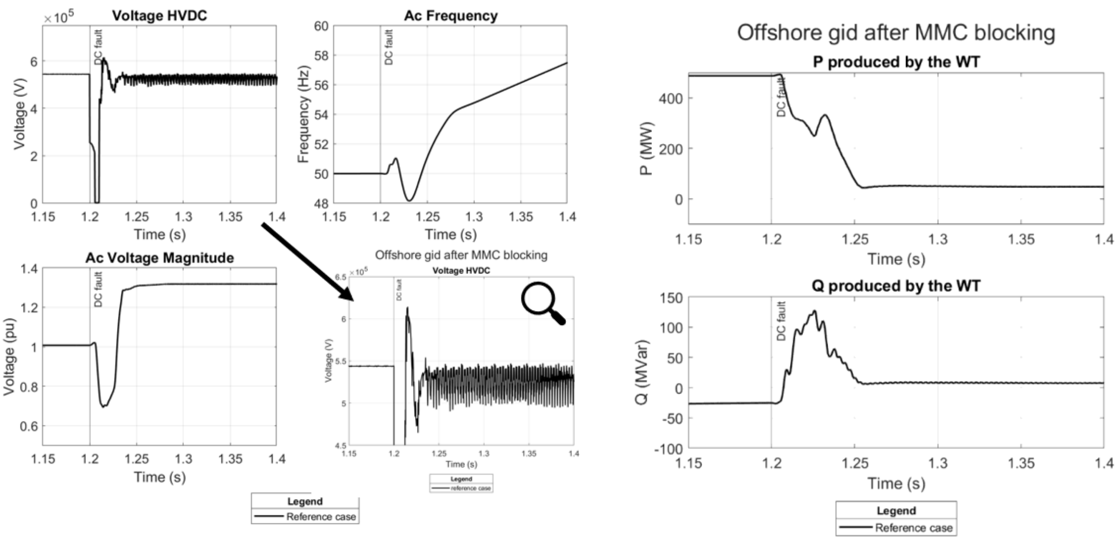
9.9.2 Islanded operation of WT

Islanding operation of WT is a subject well developed in literature as well as the problems that come with trying to operate a GFL converter in islanded operation. [47] [48] describes precisely the phenomenon observed. In the following, the phenomena in islanded mode operation are investigated in a two-step approach referring to the control functions described in **FIGURE 171.** It should be noted that other control functions for islanded mode operation may exist, more investigations on alternative control functions could be carried out. It should further be noted that other control modes such as GFM are other means to achieve enhanced DC-FRT during temporary blocking of the offshore converter. From the 4GTSO point of view additional beneficial services such as instantaneous reserves could be provided by PPMs in GFM which is already requested in current grid code specifications.

9.9.2.1 Islanded operation without PLL saturation and voltage limiter

In this stage both islanded mode operation functions are disabled. Results are shown in **FIGURE 175.** At t=1.2s, the DC fault occurs, causing the HVDC voltage to drop to a first level at around 250 kV, where the capacitors of the MMC are discharging into the fault, until the blocking of the MMC, which causes the second drop in HVDC voltage down to zero. At t=1.210 s, The DC fault is neutralized, causing the HVDC voltage to increase rapidly thanks to the TIV of the DC switching unit. Afterwards, the HVDC voltage oscillates around the diode rectifier voltage of the offshore converter. The AC grid is not impacted in the first instances of the DC fault due to the discharge of the MMC submodules. Once the MMC is blocked, the fault current is provided by the AC grid, thus the AC voltage drops and the frequency deviates due to the power unbalance. Once the DC voltage is restored, the frequency diverges, and the voltage magnitude increases compliant with observations in [47] [48]. The frequency increase is due to the Phase-locked loop (PLL): to fulfil the objectives of the control of the WT, i.e. the required P and Q transfer, The control generates an angle reference theta* slightly different from the measured angle theta of the grid to enable the power transfer. However, this relies on the fact that another converter somewhere on the grid controls the angle and frequency. While the offshore converter is blocked it is not the case, leading to a shift of angle and to an increase of frequency.

The explanation for the voltage increase observed relies on the same logic that can be explained in different ways. Another explanation is, while the AC offshore voltage is too low for the diodes of the blocked offshore converter to be passing, the offshore grid is connected to the GSC on one side and can be considered as an open circuit on the other side. The result is, the control of the GSC increases the voltage at the WT to obtain the desired power flow, but it fails as the grid is comparable to an open circuit so no current, therefore no power is flowing, so the GSC tries to increase the voltage even more to achieve its control objective until it reaches its modulation limit.



(a) (b)

FIGURE 175 (a) AC and DC grid response to offshore converter blocking; (b) Power injected by the WT on the offshore grid

Disclaimer: in **FIGURE 175**, PPM protection functions are omitted to observe the evolution of a simple GFL model without the WT tripping.

Depending on the design of the offshore grid, the AC voltage will saturate for one of the two following reasons considering no additional control functions:

- The AC voltage is limited by the modulation level of the GSC. When reaching this limit, the AC voltage becomes constant. For instance, in case of **FIGURE 175**(a) , the voltage is limited at precisely 1.31 pu.
- The AC voltage level can be lower if the offshore HVDC converter diodes become passing before the GSC reaches its modulation limit. This results in an undesired export of AC power during islanded mode operation.

For example, in **FIGURE 175** the AC voltage saturates to a constant value due to the modulation limit because the voltage is only high enough to export about 10% of the produced power.

It can be concluded that three aspects are of concerns when trying to operate an GFL PPM in islanded mode:

- The frequency divergence
- The increase in voltage magnitude
- The power injection to the HVDC grid through diodes

As mentioned before, the injection of power to the HVDC grid is a consequence of the voltage increase so those two issues are linked. The increase of frequency is also a concern for potential deblocking, an important frequency deviation may create a stronger transient when deblocking the offshore converter and may provoke difficulties when resynchronizing the converter and the offshore grid. To mitigate those issues islanded mode operation with PLL freeze and AC voltage limitation will be investigated in the next subsection.

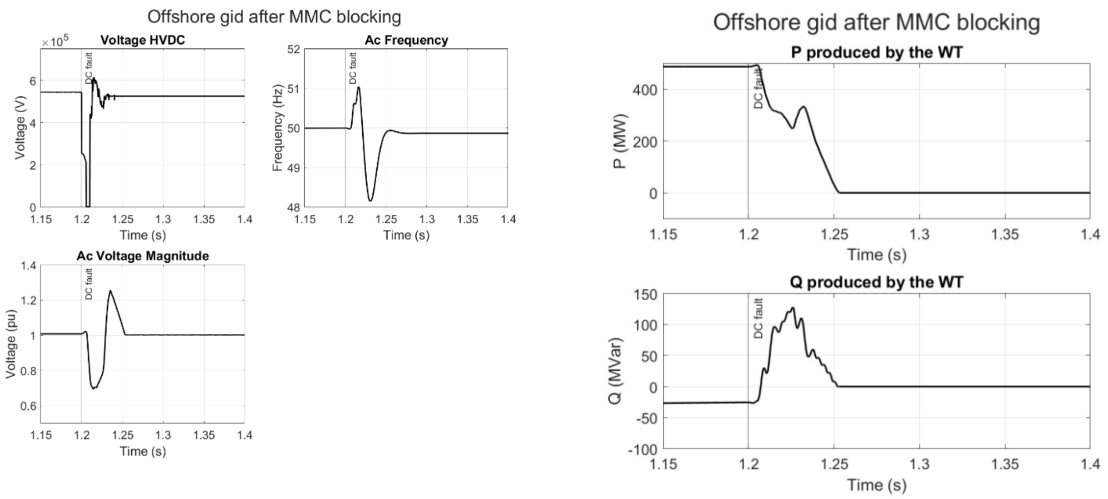
9.9.2.2 Islanded operation with PLL saturation and voltage limiter

The problem of frequency divergence of the PLL during islanded mode operation is well documented in literature and can be solved by limiting the PLL deviation, for example by saturating or freezing triggered by the measurement of an abnormal situation, here the voltage magnitude for instance. The overvoltage on the AC offshore grid must be limited so that the converter diode cannot become passing which can be realized by a voltage limiter added to the control or a combination of DC crowbar and GSC modulation limitation. Control solutions illustrating this general idea can be found in [48] [49]. Other solutions including AC chopper can also exist but will not be considered as they would require additional component not initially present in the AC grid under investigation.

The implemented islanded mode functions are solutions that do not require a change of control mode concept in normal operation. The GSC can resume GFL mode after the offshore converter is deblocked. The islanded mode triggers when the voltage measured by the WT exceeds 1.2 pu and has 2 actions:

- ➢ Freezing the PLL
- ➢ Limiting the voltage magnitude to 1 pu

By adding a PLL freeze, the frequency is maintained in an acceptable range and the WT creates a stable frequency close to 50Hz once in islanded mode. This action on frequency has no impact on the other issues observed previously and just aims to support the resynchronization when the converter deblocks. It should be noted that this study was performed with aggregated models and potentials interactions such as circulating current between WT have not been assessed.



(a) (b)

FIGURE 176 (a) AC and DC grid response with PLL freeze and voltage limiter, (b) Power response with PLL freeze and voltage limiter

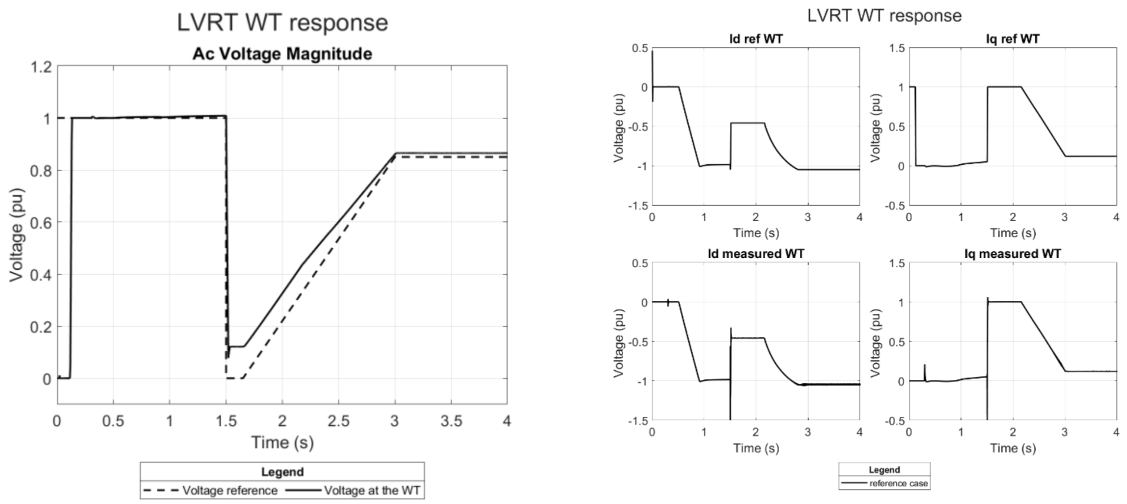
The voltage limiter efficiently reduces the voltage to the designated value of 1 pu. Note that a small transient exists where the voltage exceeds the trigger value of 1.2 pu, which must be taken into account to not interfere with other protection functions such as ACCB tripping. The limitation of the OV also prevents the converter diodes from being passing and stops the transfer of active power.

The results show that with those two additional functions the previously identified issues are mitigated. From a control perspective, no time limit for islanded mode operation has been identified but the maximum duration should comply within the energy dissipation rating of the DC chopper.

Disclaimer: It shall be noted that islanded mode might not be readily available in all current market solutions for PPMs. Beyond the simulation assumptions made in the key investigations, detailed investigations might be required for some vendors before such a functionality can be offered commercially.

9.9.2.3 LVRT ability of the WT

To demonstrate that the additional functionalities presented in **FIGURE 171** do not hinder compliance with existing requirements during the LVRT **FIGURE 177** (a) shows the PPMs response to a LV event created by replacing the offshore converter by controllable AC voltage source which emulate a LV event corresponding to the LVRT profile implemented in the WT. The WF responds to the LVRT event by providing reactive current, successfully riding through zero voltage for 150ms, proving their ability to ride though the LV event caused by a DC fault.



(a) (b)

FIGURE 177 WT response to an AC grid forced at the LVRT profile requirement: (a) Voltage (b) Current

9.9.3 Reconnection of the offshore converter to the AC offshore grid

9.9.3.1 Technical issues

In literature resynchronizing a GFL HVDC converter to a grid or the black start of PPM [50] have already been addressed but reconnecting a GFM HVDC converter over such a short time frame is a different challenge and can lead to different interactions.

Potential concerns for the offshore converter during resynchronization are the necessary conditions for deblocking, the reinitialization of the converter after the deblocking and the transient on both the AC and DC grid caused by the deblocking. After resynchronization of the offshore converter, the PPMs need to ensure the transition from islanded mode operation to GFL control including post fault active power recovery. This will be investigated in this section. Based on the previous section, the PLL freeze and AC voltage limiter function will be considered as a starting point, providing a desired voltage magnitude and frequency to resynchronize to for the offshore converter.

For the offshore converter, a deblocking function was designed in a very simple way. The converter deblocks when the DC voltage recovered to operational voltage bands as shown in **FIGURE 54**.A focus of this study will be the interactions of this deblocking and resynchronization function with the islanded mode previously defined and characterizing the different behaviour of the AC grid if the deblocking is initiated before or after the islanded mode is triggered.

The deblocking function shall ensure the recovery of the converter control to allow a smooth resynchronization to the DC and AC grid:

- **The reset of the control loop of the converter:** The errors integrated just before the blocking probably have no relation with the restored voltage that exist during the deblocking
- **Resynchronization to the offshore grid:** As an initial solution for the resynchronization, the measurement of the converter PLL is used to support the converter control. The PLL keeps measuring the grid angle despite the blocking and can therefore be used to initialize the V/f angle for the converter after deblocking as illustrated in **FIGURE 178**. This way transients or phase jumps during the synchronization process can be significantly reduced.

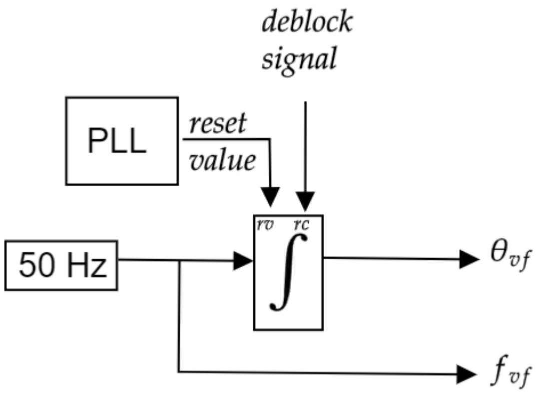
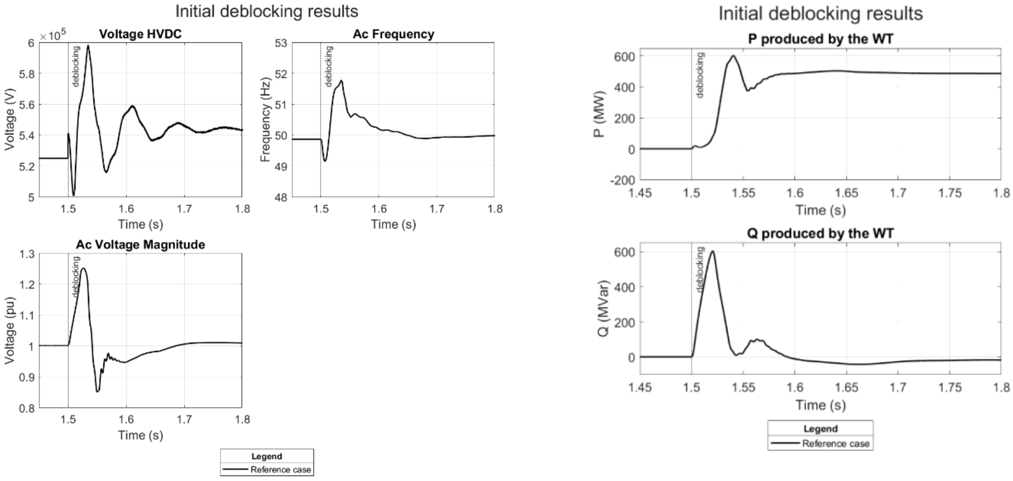


FIGURE 178 V/f angle initialization through PLL use

9.9.3.2 Resynchronization without additional functions

The deblocking was first simulated without the resynchronisation functions described above in order to observe possible transients. Initial results in **FIGURE 179** show an important transient in voltage, frequency and magnitude. The first reason for this transient is the initial angle difference compared to the offshore grid angle. The second reason is the transient increase of power at WT side after deblocking of the converter.

The observed overvoltage transients are critical as they reach 1.25 pu, which could cause a reactivation of islanded mode. The second issue is the HVDC voltage which increases almost 20% over its nominal value and will cause stress to converters in charge of the DC voltage.



(a) (b)

FIGURE 179 (a) AC and DC grid response and (b) power response to deblocking

9.9.3.3 Pre-set deactivation of islanded mode

To investigate the impact of the blocking transient on the resynchronization, in the simulation environment both islanded mode and deblocking will be deactivated at the same time t=1.5 s, 300 ms after the DC fault, to ensure that the system reached a steady state. The transition from islanded mode operation to GFL based on local measurements without communication will be addressed in section 9.9.3.4.

To solve the issues identified in the previous section, two additional modifications are considered:

- Resynchronization to the offshore grid angle before deblocking
- Reduce the power transient of the WT.
  - By resetting the PI controller of the WT
  - By reducing the power injected by the MSC and re-ramp the power after the deblocking

The results for resynchronisation considering such additional functions are presented in **FIGURE 180** while being compared to the reference case. Thanks to the synchronization method, the AC voltage increase is lowered from 1.25 pu to close to 1.1 pu. The second result “with PI reset”, includes a reset of the integral components of the PI loops of the GSC of the WT. As pre-fault and post-fault errors are not necessarily correlated, it might cause the control to have an adverse effect during the deblocking. The third results showcase the effect of a potential curtailment, the power injected into the DC back-to-back is reduced to 0 before being restored with a ramp up between 1.6 and 2s. **Disclaimer**: That specific test was performed by modifying the power injected in the back-to-back for simplicity. Although this raises the question of feasibility, similar results could be obtained by acting on the reference of the outer loops of the WT control. The fourth result combines the PI reset and the power curtailment in addition to the resynchronization through a PLL.

The most obvious effect of modifications at the PPMs level is acting on power transient and the HVDC voltage. Although, the damping of the transient is most efficient with rest of both power reference set-point and PI reset, it also slows down the response of the system considerably.

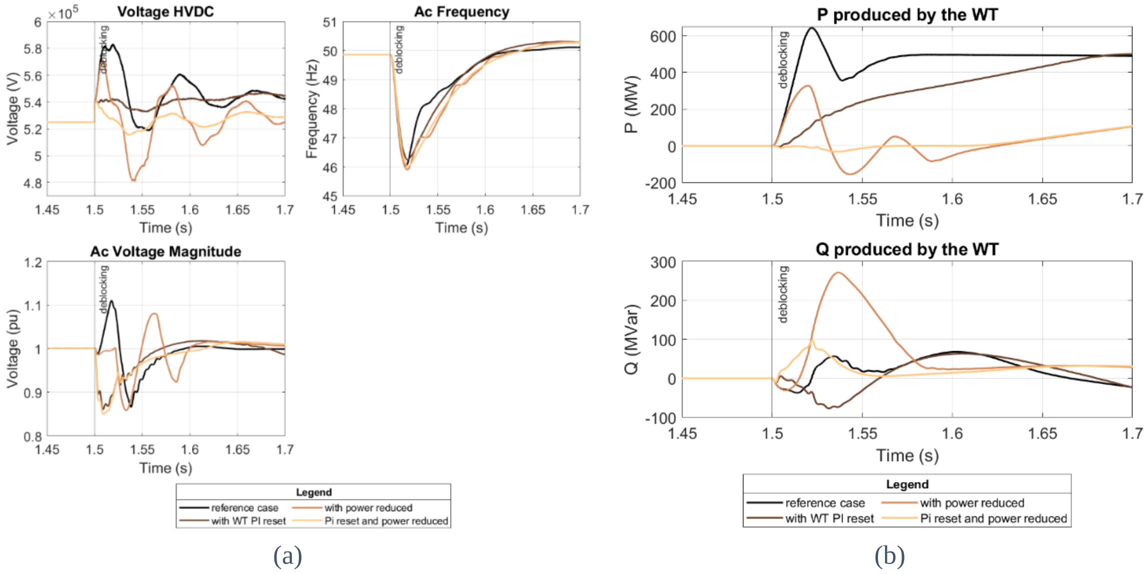
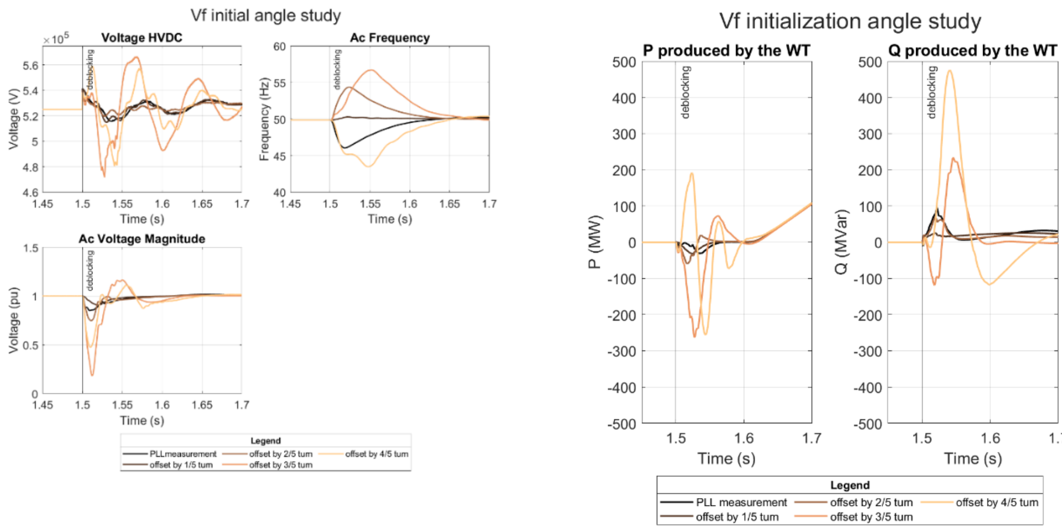


FIGURE 180 (a) AC and DC grid sensitivity and (b) power sensitivity to WT operation during deblocking

The following simulations are performed with reset of both PI and power reference. The stability in terms of frequency has been observed to be greatly affected by the change on the initialization angle performed with the initial synchronization. However, this transient might be further improved when using a different angle. For the sake of determining the optimal angle and leads to improve the synchronization to the offshore grid, a sensitivity analysis is performed to find the best angle for the resynchronization of the offshore converter. The initialization realized with an angle by the PLL was kept but offset angles were added to the measured angle by increments of 2pi/5. The results are illustrated on **FIGURE 181**.

In the best-case scenario, PLL measurement +1*2pi/5, the voltage only drops to 0.95 pu before being restored and the frequency is almost not impacted. Opposite to this, in the worst-case scenario, PLL measurement +3*2pi/5, where the frequency drops to 0.25 pu and the frequency increases above 56 Hz.



(a) (b)

FIGURE 181 (a) AC and DC grid sensitivity and (b) power sensitivity to V/f synchronization angle

As shown in the sensitivity analysis, the synchronization with a PLL guarantees an initialization angle close to the grid angle which improves the transient compared to the worst case scenario. However, a more in-depth analysis might help determine the causes for this offset and help obtain an optimal transient for the deblocking of the converter, guaranteeing its safety and minimizing the power loss.

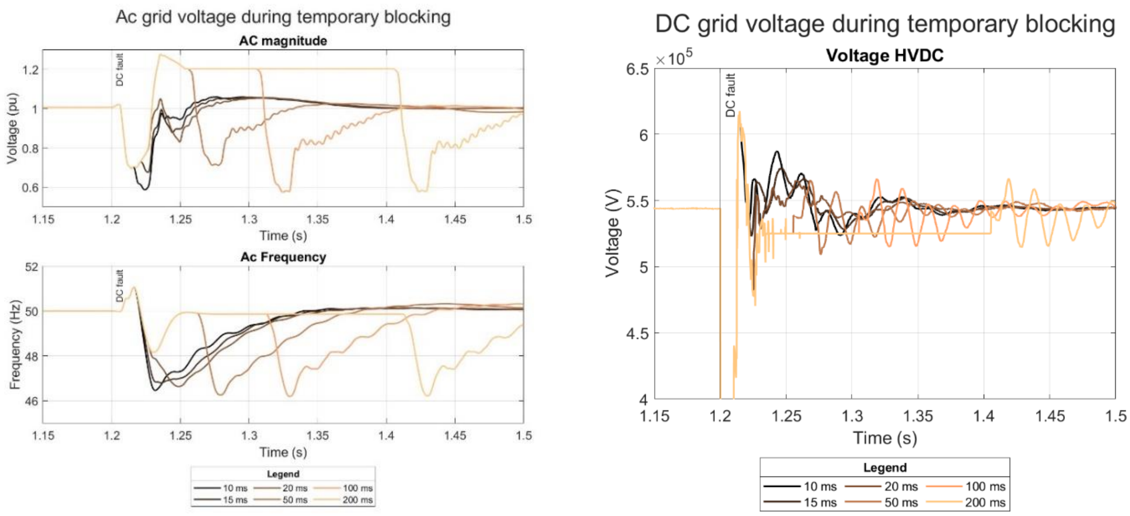
In the simulations of this section, the deactivation of the islanded mode of the WT occurred at a predetermined time set to match the deblocking of the converter. In a real system this would require some signal exchange to deactivate islanded mode which is undesirable due to the slow speed of communications compared to the considered time frame. The objective of the next section is to determine a way for the PPM to detect the deblocking and resynchronization of the offshore converter based on measurable signals.

9.9.3.4 Natural deactivation of islanded power mode

In this section a limitation of the voltage magnitude of the PPMs to a higher value than 1 pu during islanded mode operation is considered. When the offshore converter deblocks, the subsequent decrease of the AC voltage serves as a deactivation criterion based on local measurement where no communication is needed.

This voltage limit should be set high enough to ensure that the islanded mode is only deactivated when there is a significant difference between the islanded mode voltage and the reference of the offshore converter, to easily detect the change, but it also should not be too high to avoid the blocked converter becoming passing or that the OVRT limits are violated.

With the simulation parameters presented, a limit of 1.2 pu allows both conditions to be fulfilled. The deactivation threshold for the islanded mode of PPMs was set to 1.03 pu. The simulation presented here includes most of the functions from the previous scenarios (voltage limiter, PLL freeze, PI reset, V/ initialization). Due to its low impact and concerns about the time required to activate it, the power curtailment considered previously will be discarded in the following studies. The simulation results shown in **FIGURE 182** present the response of the system over a large scale of temporary blocking duration, the time in the legend represents the duration of temporary converter blocking.



(a) (b)

FIGURE 182 (a) AC grid and (b) DC grid sensitivity to temporary blocking duration; automatized resynchronization of PPMs

Two main behavioural cases can be identified:

1 Case long enough to trigger the islanded mode of the WT
2 Cases of fast deblocking before islanded mode is activated (t_blocking<20ms).

Disclaimer: The measurement of AC voltage magnitude used for the triggering of the islanding mode is the same used for the triggering of OVRT protection, meaning there is no possibility for the protection to trip before the islanding mode if the voltage exceeds the designed trigger of 1.2 pu.

Temporary blocking is shown to be theoretically possible across all the range of considered duration with a few aspects to take note of:

- For duration close to the activation of the islanded mode, the power restoration duration varies between 50 ms and 150 ms depending on whether the islanding mode of the WT was activated or not.
- For long durations close to 300 ms, EMT simulations show no limitations in temporary blocking duration. However, one currently identified limit is the thermal energy of the WT DC crowbar dissipating the power during the temporary blocking. EMT simulations have shown theoretical feasibility, but physical limitations should be discussed.

9.9.4 Recommendations for PPMs and offshore converters during DC-FRT

This section investigated the overall feasibility of temporary blocking assessing different control functions during islanded mode operation of PPMs and during resynchronization of the offshore converter. All control solutions described in **FIGURE 171** were added to the regular GFL control were tested together across simulation representing expectations during temporary blocking. The system was able to successfully ride through all critical cases under the assumptions the additional functions presented in **FIGURE 171** are added.

From a functional perspective, the DC-FRT requirements and existing AC requirements shall be aligned in order to ensure stable operation during and after DC grid contingencies. This implies that during temporary blocking of half-bridge type offshore converters, the PPMs shall operate in a safe and stable islanded mode operation without violation of the OVRT profile. Considering a non-TSO specific OVRT profile as shown in **FIGURE 183**, it would be recommended that during islanded mode (IM) operation the PPMs operate below the transient overvoltage level U_{OV1} such that unwanted disconnection during temporary blocking is avoided. The maximum time to operate in islanded mode T_{IM} shall be aligned with the DC-FRT profile and in particular with the maximum deblocking time which is defined by the following equation where T_{rec2} is the maximum DC voltage recovery time and ΔT_{dblk} is the maximum deblocking time after DC voltage recovery. An additional settling time T_{set} for the AC side shall be considered. Further, the frequency limitation during T_{IM} shall be limited in order to ensure a smooth and fast synchronization.

$$T_{IM} = T_{rec2} + \Delta T_{dblk} + T_{set}$$

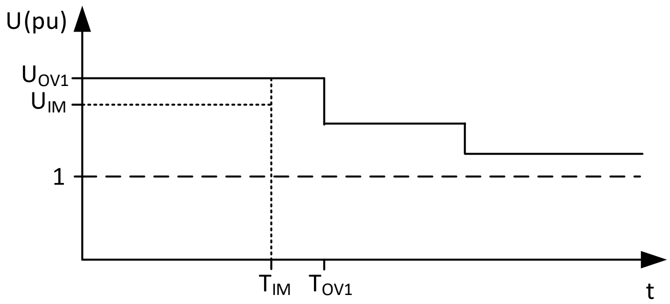


FIGURE 183 OVRT profile (non-TSO specific) for DC connected PPMs; recommendations for islanded mode operation during DC contingencies in case of temporary converter blocking in alignment with DC-FRT requirements

After deblocking the offshore converter resynchronizes to the offshore grid being in islanded operation. The resynchronization of the offshore converter shall be as smooth as possible, avoiding phase jumps. Therefore, it is expected that the offshore converter considers the measured phase angle before deblocking. Once synchronized, the offshore converter is expected to return into the initial control mode, controlling AC voltage and frequency.

After resynchronization of the offshore converter, the PPMs shall return from islanded mode operation into the pre-fault grid following control mode. The step response of active power shall be compliant with post-fault active power recovery requirements (see section 7.3.5).

9.10 DC grid control architecture in multi-TSO context

9.10.1 Introduction

The previous sections have addressed requirements for MTDC systems from a functional point of view. All the functionalities that must be included in the DC grid control were listed and discussed without detailing control architecture nor addressing multi-TSO projects. In this section, aspects related to DC grid control implementation are further discussed, such as controllers hardware redundancy, communication, and hierarchy, as well as the interface between DC grid control and TSOs. Moreover, future potential European HVDC use cases, such as those listed in the deliverable D3.1, include mostly multi-TSO projects. This stresses the importance of analysing control architecture considering relevant constraints that apply for this type of project.

This section aims to enhance understanding of the practical aspects involved in implementing functional requirements and to explore potential options for future DC grid control architectures, considering the diverse needs and appropriate solutions for multi-TSO projects. Therefore, the specific goals of this section are:

1. To clarify constraints for the DC grid control architecture in a multi-TSO context.
2. Discuss potential DC grid control topologies to implement required functionalities.

Accordingly, the remaining subsections of this section cover: most relevant constraints in multi-TSO projects from both regulatory and functional perspectives; two potential DC grid control architectures that aim at complying with these constraints; and a conclusion subsection to highlight the takeaway points of this section.

This section is based on the discussions within the workstream AC/DC Security and Dispatch.

Disclaimer: *The DC grid control architectures presented in this section are intended solely to raise awareness about practical implementation aspects in a multi-TSO context. They do not reflect a formal consensus within the InterOPERA consortium. The two-stage architecture discussed was proposed by the 4 German TSO working group on the topic and does not necessarily align with other partners perspectives. Similarly, the single-stage architecture represents another conceptual approach without implying collective agreement. Since this work is still in progress, the ideas and proposals outlined in this section are subject to further changes.*

9.10.2 Constraints for the choice of DC grid control architecture in multi-TSO context

Projects involving multiple TSOs require special attention to the implementation of control architecture. Because these stakeholders are different companies, these projects require a clear separation between different TSOs from both legal and operational point of view. The remainder of this subsection covers first security and operation principles that must be followed in this type of multi-party projects in Subsection 9.10.2.1, and how these principles translate into development constraints applicable for these projects in Subsection 9.10.2.2.

Note: This section is based on an analysis made by the 4 German TSOs (4GTSOs) working group on the regulatory constraints for DC grid control architecture in multi-TSO context. This working group includes 50Hertz, Amprion, TenneT and TransnetBW.

9.10.2.1 Security and operation principles

The DC grid control architecture of a multi-TSO system shall consider security and operation principles established by the involved TSOs. A list of conceptual guidelines can be derived from applicable regulatory framework presented in Subsection 9.10.5, as presented below.

Separation of partners

Each TSO shall be treated as external to the other TSOs. Therefore, there shall be a clear definition of zones and their responsible TSOs, where the safety rules of that TSO apply and the definition of responsibilities is unambiguously defined. These areas are referred in this text as TSO zones.

Furthermore, systems ownership and, especially, responsibility must be clearly defined for the entire system and/or all subsystems. Note, system ownership and responsibility do not necessarily have to match for certain hardware, functionalities or activities, such as setting power flow. Yet, due to potential consequences in operating switchgears (personal injuries, property damage or financial costs), its responsibility always lies with the owner. For the responsibility there must be exactly one legal person that can be accounted for.

From a technical point of view, the assigned responsibility needs to be reflected in the technological capabilities, such that, only the responsible legal person can issue the respective commands. Therefore, the choice of TSOs zones is a critical step in the system design and shall consider technical aspects of the specific use case to guarantee an appropriate system operation.

High availability

The systems shall be designed to be resilient to ordinary adverse events, i.e. a single error or shutdown/unavailability of a system or a device shall never result, directly or indirectly, in the loss of the intended function nor to a loss of the supervisory control and data acquisition capabilities of the MTDC system. This principle implies:

- ***Hardware redundancy***: Multiple instances of the same hardware to be able to implement functions such as seamless master role switch over.

- ***Communication redundancy***: Communication failure probability shall be as low as possible by design, with redundant links, e.g., communication network topology such as ring or mesh.

Compliance with data and information regulation

The common applicable standards and laws for cybersecurity require the fulfilment of cybersecurity requirements for any project regardless the number of partners. It is based on three pillars of information security: confidentiality, integrity and accessibility. The need-to-know-principle is to be followed. One tool for that is network segmentation. Where applicable and technically possible, network segmentation shall be realized by physical means to strictly separate systems of different functionalities and explicitly separate process and control systems from administrative functionalities. Nevertheless, segmentation shall not have an impact on operational functionality, nor shall it influence the independent functionality of the segmented zone. This segmentation also includes preventing uncontrolled or unintended transferring of information between segmentation zones. Additionally, this holds especially true for a multi-party project, where certain data is strictly forbidden to be shared between the partners, e.g. process data.

To summarize, the implementation of the DC grid control shall at least fulfil the requirements of data privacy, communication protocols standards and documentation practices, as described in Subsection 9.10.5. Note requirements these are derived from ENTSO-E and government requirements for the TSOs.

Compliance with power schedule processes and regulation

Power transmission must be able to follow power schedule coming from processes based on generation forecasts and market-based instances, using when applicable power flow optimization to operate the HVDC system. This operation shall also comply with Electricity Market Regulation, which stipulates a certain level of cross-border transmission capacity and critical elements availability for European cross-zonal electricity trading. Moreover, provision of data due to compliance with market transparency laws for overall system must be foreseen. Eventual local feed-in priority rules and redispatch process, e.g. respectively German regulation EEG (Erneuerbare-Energien-Gesetz: Renewable Energy Sources Act) and RAS (Redispatch-Abwicklungsserver: Redispatch Processing Server), shall also be considered in power dispatch.

Other criteria for evaluation of DC grid control architecture

It is noteworthy that the list of principles outlined above is not exhaustive. DC grid control architecture is also assessed through different criteria related to system operation and planning. These criteria include, for instance, the reaction time to contingencies, and costs and updates related to the expandability of the system in later planning stages.

9.10.2.2 DC grid control functional development constraints

The provided principles are expressed into specific requirements that apply to DC grid control implementation:

- Separation of partners in sequential control
  - Operation of switches and activation of control sequences can be carried out only by responsible TSO, i.e. within its own TSO zone[55];
  - Automatic sequences are limited to individual converter in accordance with TSO ownership;
  - Sequences across responsibility zones require safe intermediate states and communication between the involved responsible parties.
- Continuous control
  - EPC (Emergency Power Control) is in scope of local converter logic and not of the DC grid control, however EPC actions or information might need to be coordinated to keep the entire system stable;
  - Overlaying processes at TSOs and ENTSO-E level, which consider contingency analysis and emergency situations, will define the framework conditions for power regulation:
    - Power setpoint (e.g. schedule) per onshore converter ;
    - Permissible power band in the form of an upper and lower setpoint limit per onshore converter.

These requirements bound the design of the DC grid control architecture and some of them raise important implementation questions. A key issue that arises is determining the necessary adaptations to

[55] Note TSO zone is the area of responsibility of the TSO. As reminder, note this is independent from ownership.

ensure compliance with partner separation constraints, particularly regarding the operation of switches exclusively by the relevant TSO. Furthermore, these constraints highlight the need for an organizational and communication framework to interface the different TSOs between themselves and with upper-level (ENTSO-E) processes.

In the next section, aspects related to DC grid control architecture, topology and functions implementation are then discussed in an attempt to provide potential solutions for DC grid control architecture implementation in multi-TSO projects.

9.10.3 Control architectures, hardware topology and functions implementation

The different regulatory and functional constraints delimit the implementation options of the DC grid control functional requirements. Moreover, they establish guidelines also for aspects such as the number of hardware instances and communication topology, which can be relevant to the choice of the overall hardware topology. These elements are discussed in this subsection to describe potential solutions in multi-TSO context. First, the basic definitions of control architecture and hardware topology within the scope of this section are described in Subsection 9.10.3.1. Next, Subsection 9.10.3.2 discusses control functions required for the DC grid control. Subsection 9.10.3.3 gives an overview of the architectures considered within this workstream, while Subsections 9.10.3.4 and 9.10.3.5 further describe the implementation of these architectures. Finally, Subsection 9.10.3.6 elaborates the function implementation in these different architectures.

9.10.3.1 Basic definitions

Disclaimer: *The definitions provided in this subsection are intended solely for use within its context. They do not establish formal guidelines or standardized terminology for DC grid control architecture. Instead, they are introduced here to facilitate the reading and understanding of the section's content.*

Control architecture

Control architecture can be defined as the theoretical or logical framework that defines the fundamental structure and organization of a control system. It provides a high-level blueprint that outlines the control hierarchy without specifying their physical location or detailed configuration. Furthermore, it does not describe the specific communication network structure, the number of control entity instances, or the implementation details.

- **Control layers**

  The DC grid control architecture is constituted of the three fundamental layers illustrated in FIGURE 184: AC/DC grid dispatch layer, DC grid operational layer and Subsystems control layer. The AC/DC grid dispatch layer is expected to deal with security and dispatch aspects in a timescale of several minutes, defining schedules for power and devices maintenance. The DC grid operational layer is the main focus of this section. It can be seen as the layer where the main functionalities with a need of coordination are implemented. Its implementation timescales can range from tens of milliseconds up to a few minutes depending on the function. The Subsystems control layer encompasses the controllers of subsystems, i.e. Conversion Station (CS) controller, Power Park Module (PPM) controller and DC Switching Station (DCCS) controller.

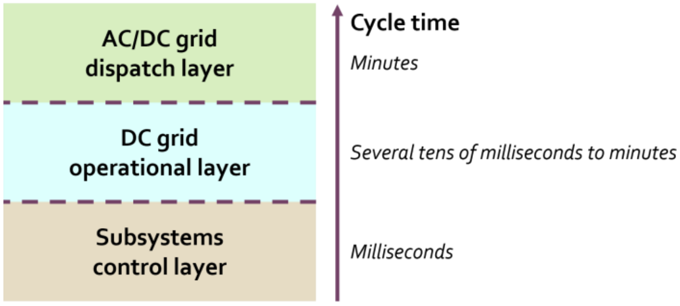


FIGURE 184: Control layers in DC grid control context.

- **Controllers**

  In these layers, the implementation of functions is done in physical control entities that are named controllers. Three types of controllers are discussed in this document in the DC grid operational layer: DC Grid Controller (DCGC), TSO-DC Grid Controller (TSO-DCGC) and Hub Controllers (HC). These controllers are implemented in different control architectures as it will be further discussed in the next subsections presenting the potential control architectures.

Hardware topology

The hardware topology is defined in this section as the hardware layout considering the number of controllers and how they are connected from a communication point of view. A given hardware topology is said to be decentralized regarding a given controller if at least two instances of this controller exist, regardless of the location of the instances (same place or geographically separated). Examples illustrating centralized and decentralized topologies with respect to controller type A are depicted in FIGURE 185. Moreover, the communication network topology between these elements can be redundant or non-redundant. Communication network topology is also illustrated for controllers of the same type (between type A controllers) and for controllers of different type (between type A and type B controllers) with examples of redundant (meshed and ring) and non-redundant (point-to-point) communication topologies in FIGURE 185.

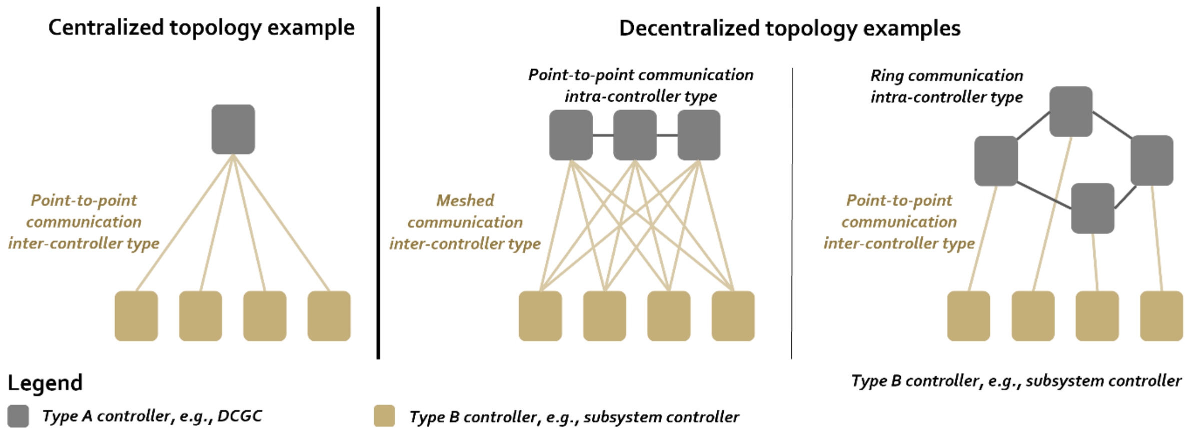


FIGURE 185: Examples of centralized and decentralized topologies, with redundant and non-redundant communication network represented by lines connecting different elements.

The implementation of several instances of the same controller type requires them to be coordinated. The coordination can be applied by roles such as master/slave. This is defined in this section as the operation strategy.

- **Operation strategy**
  The operation strategy is defined as the control hierarchy between controllers of same type (on the same stage). The two main operation strategies relevant for the DC grid control are centralized (*e.g.* master-slave) and distributed. The centralized operation strategy is characterized by having one controller operating as a master, which is actively and exclusively sending references and commands to other controller instances operating as slaves. Furthermore, all controllers - master and slave - are receiving measurement and status signals from their subordinate controllers, while additionally the slave controller instances transmit these signals to the master controller. In this centralized operation strategy, it is also possible to have controllers instances performing slave-like monitoring and communication functions, but prepared to take over the master role, named hot standby. On the other hand, in distributed operation strategy, the controllers operate in a cooperative manner without a single central authority, in such a way there is a functional parity. Examples illustrating centralized and distributed operation strategies with respect to controller type A are depicted in FIGURE 186.

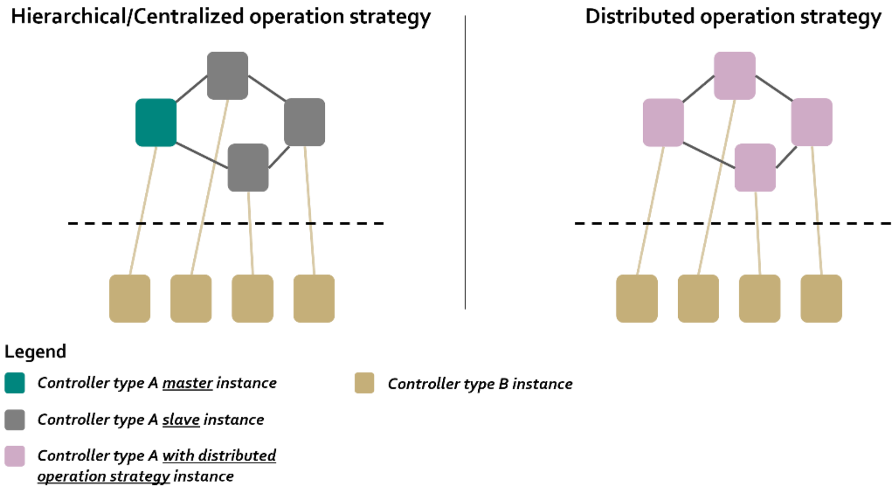


FIGURE 186: Examples of different operation strategies for controller type A in decentralized topologies.

An important nuance is that it is possible to have different operation strategies (centralized or distributed) for different functions using the same controllers. For instance, in principle, in a decentralized hardware topology for a given controller, it is possible to implement a centralized operation strategy for one function (e.g. DC power flow) and a distributed operation strategy for another function (e.g. PPM curtailment). The definition of these functions is further developed for clarity in the next subsection.

To summarize, a schematic gathering all the information about control architecture, hardware topology, operation strategy, including signals, is referred in this section as an **implementation of control architecture**. The implementation of control architectures discussed in this section are developed in Subsections 9.10.3.4 and 9.10.3.5.

9.10.3.2 Functions of DC grid control

It is also important to define the functions required for the operation of an HVDC system which can be implemented in different control layers:

- **Power schedule**: Definition of AC power setpoints for onshore converter stations. The implementation of this function requires sending AC power schedules to TSOs and relevant control instances.
- **DC power flow computation**: Computation of all the voltages and power setpoints for converters through the computation of voltage and currents in the HVDC system respecting security constraints. The implementation of this function requires receiving AC power schedules from upper control levels and sending AC power and DC voltage setpoints for converters to relevant controllers that communicate with converters stations.
- **Secondary control coordination**: Coordination of converters voltage and power setpoints to maintain or restore the power flow and DC node voltages within the specified limits after a contingency. The implementation of this function requires sending appropriate power and DC voltage setpoints to relevant controllers that communicate with converters stations.
- **Control mode management**: Coordination of the control modes and their associated parameters, such as DC voltage droop, when there is a need, such as a change of topology, according to predefined criteria. In this section, this includes coordinating the ramp rate of individual converter stations or unit to ensure the power balance during the ramping process.
- **N-1 contingency analysis**: Algorithm able to predict whether a system will respect operation limits or not after a given N-1 contingency.
- **Curtailment coordination**: Algorithm able to manage curative PPM power curtailment among different PPMs considering online system status (measurements, devices availability and actual generation). Such a curative PPM power curtailment coordination could lead to reduced total power curtailed in the system. It is furthermore important to distinguish between the demand of curative and preventive curtailment. Curative curtailment is related to an emergency need to ensure system security, while preventive curtailment is related to actions handled at the dispatch level. The implementation of this function requires receiving multiple measurement signals and sending power limits signals to the PPMs.
- **Sequential control coordination**: Implementation of an algorithm able to realize switching actions and **implementation of power flow modifications** considering online system status guaranteeing system security. Moreover, it includes being able to operate the switchgears of the system. Consequently, the implementation of this function requires receiving measurement signals and switches status and sending commands to them.
- **Sequential control requests and clearance**: Procedure where a TSO either request macro-sequences (e.g. start-up, reconfiguration etc.) or clear (accept) requests from other TSOs through low speed communication (e.g. phone calls) or through the DCGC. In this way, all relevant TSOs authorize a sequence before its implementation. In the case of using a DCGC, the sequential control request-clearance mechanism involves the following steps: 1. A request from a TSO of a macro-sequence to the DCGC; 2. The DCGC proposes detailed sequential actions to implement the TSO request (open/close DC Switching Unit, change of CS control modes etc.) to the TSO grid control centers of the relevant TSOs; 3. All relevant TSOs approve (clear) the sequence and send an approval signal to the DCGC; and 4. The DCGC commands the different subsystems to

implement the actions safely. Note this does not entail the DCGC to control individual switchgear, see Chapter 5 on sequential control for more details.

Note that this is not an exhaustive list of all core functions required in DC systems. Additional functions, such as power capacity/reserves computation, could also be included. However, discussions on these topics were not considered mature enough within the workstream to reach a consensus, and they are not deemed essential for analysing different control architectures at the current stage of discussions.

9.10.3.3 Overview of potential architectures of DC grid control

Two main solutions were discussed in this workstream: single-stage and two-stage DC grid operational layer architectures. An overview of these architectures, including also upper (AC/DC grid dispatch) and lower (subsystems control) layers, is presented in FIGURE 187. In this figure, CS, PPM and DCSS, stand for Converter Station, Power Park Module and DC Switching Station, respectively.

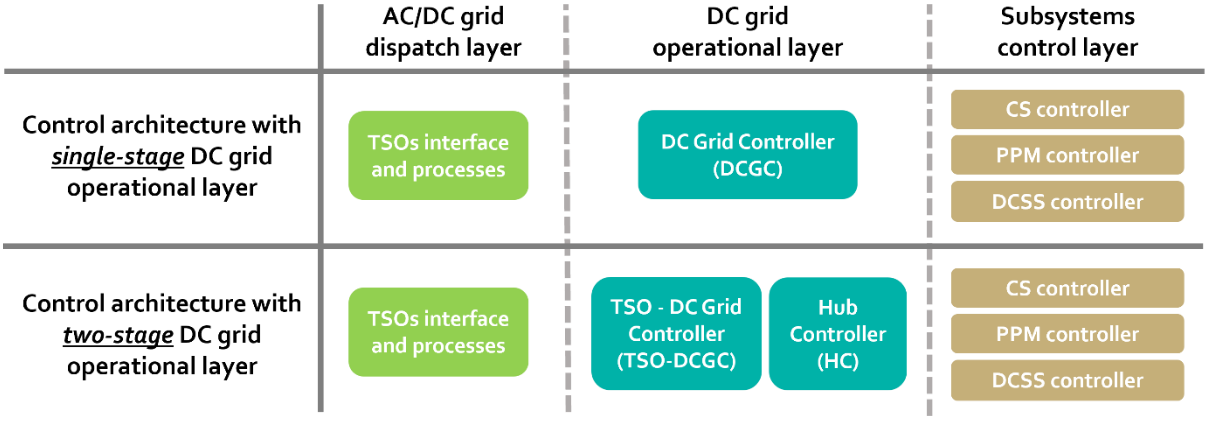


FIGURE 187: Conceptual overview of DC grid control architecture solutions discussed in the framework of the workstream AC/DC Security and Dispatch.

The first architecture implements all DC grid control functions in one stage[56]. These functions are appropriately coordinated at this level in the DC Grid Controller (DCGC).

Meanwhile, the second architecture, proposed by the 4GTSO working group, originates from a need to propose a way to comply with regulatory constraints, such as the separation of partners in multi-TSO projects. In this two-stage architecture, DC grid control functions are mostly implemented in two controllers: TSO-DC Grid Controller (TSO-DCGC) and Hub Controller (HC). In short, the TSO-DCGC is a controller with a relatively slow cycle time used by each TSO as an interface between its TSO grid control center and the HC. In turn, at a lower level, the HC controls the entire HVDC hub with respect to functions that require faster implementation. In this context, a hub shall be understood as a multiterminal HVDC system, that is operated individually. In the discussions in this workstream, an MTDC system is considered as a hub, and connection between different hubs is left for future discussions.

It is noteworthy that none of the DC grid control architectures discussed are in their final versions and there is no consensus on whether they may require adaptations in order to comply with all the requirements and on their feasibility.

[56] Control stage is used in this document as a subdivision of a control layer.

The operation strategy adopted for most functions is implemented in a centralized operation strategy, i.e. with only one master controlling the subsystems at a given instant[57]. A preliminary summary of the implementation of these architectures is proposed in Table 48. This implementation of each architecture is further discussed in the dedicated subsections.

Table 48: Classification of DC grid control architecture solutions discussed in the framework of the workstream AC/DC Security and Dispatch.

Architecture	Controller	Hardware topology	Operation strategy
Single-stage	DCGC	Decentralized	Centralized (Master-Slave)
Two-stage	TSO-DCGC	Decentralized	Centralized (Master-Slave)
	HC	Decentralized	Centralized (Master-Slave)

To discuss these architectures, a 4-Terminal DC system, operated by 2 TSOs which own each one a point-to-point link, is used as elementary case study. This case study is depicted in FIGURE 188, presenting the hardware layer of the system and highlighting the 2 TSO responsibility zones.

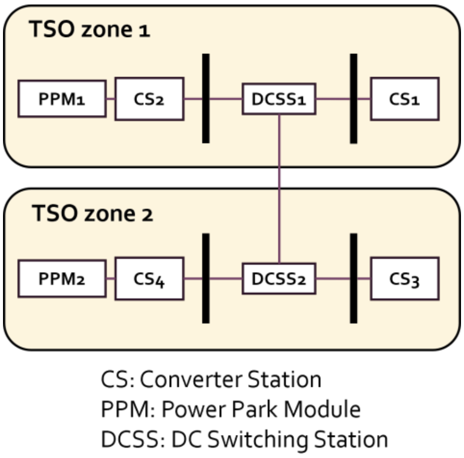


FIGURE 188: Hardware layer of 4-terminal and 2-TSO DC system example for discussing architectures of DC grid operational layer.

9.10.3.4 Single-stage architecture

The single-stage architecture consists of an implementation of the core functions of the DC grid control at a single control level. The controller at this level, namely DC Grid Controller (DCGC), implements then DC power flow computation, sequential control coordination, control mode management, secondary control coordination, N-1 contingency analysis and PPM curtailment coordination.

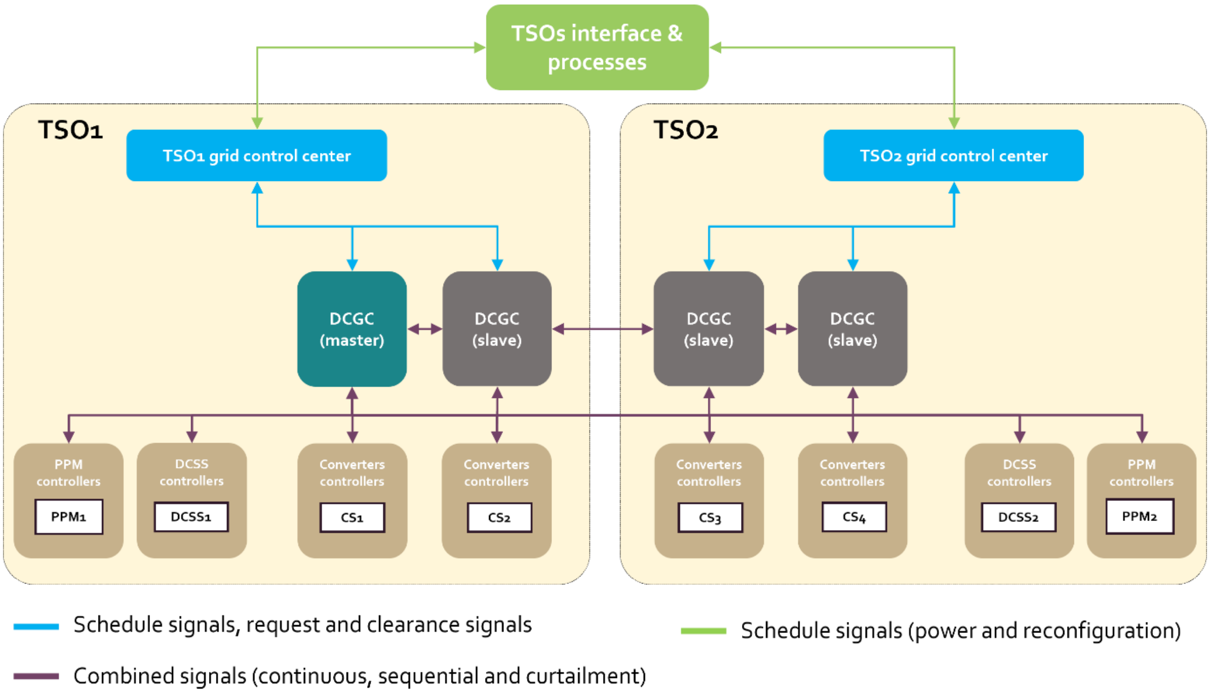
There can be as many instances of DC Grid Controller as necessary, but only one DCGC acts as master in an HVDC system. The hardware location of a DCGC is not predefined, but it can be eventually placed in the TSO grid control centers or in the converter stations, for example. It is important to note there might be required a dedicated interface in TSO grid control centers to adequately communicate with the DCGCs.

[57] Note that different scopes of functionalities are considered in the single-stage and two-stage architecture, as further discussed in sections 9.10.3.4 and 9.10.3.5.

To attempt to comply with separation of partners constraints, a request-clearance mechanism between DCGC and TSO grid control centers can be implemented especially for sequential control actions.

The implementation of single-stage architecture for the 4T-2TSO DC system case study is depicted in FIGURE 189 to illustrate the communication and signals exchanged in this control architecture. An upper-level control is assumed in the AC/DC grid dispatch layer (TSOs interface and processes), where power schedule is decided. These signals are sent to the TSO grid control centers, which then send this power and reconfiguration schedule to the DCGC instances within their respective TSO zones. The master DCGC implements the power schedule sent by TSO grid control center in the same TSO zone and sequential control is handled using the aforementioned request-and-clearance mechanism.

The master DCGC coordinates all necessary functions and sends signals related to continuous control, sequential control, and PPM curtailment to each subsystem across the system and to the slave DCGC instances. These signals include power and voltage references for converters, control modes and parameters for converters, open/close commands for DCSSs, and curtailment orders for PPMs, when required. All DCGC instances also receive measurements from subsystems and send to the TSO grid control centers relevant measurements for monitoring purposes. Both TSO grid control centers receive these measurements exclusively from DCGCs in their respective TSO zones[58]. The bidirectional arrows represent a two-way communication flow: higher-level controllers send commands to lower levels, while measurements flow in the opposite direction for monitoring and feedback. Additionally, DCGC shall have a typical cycle time at the timescale of few hundreds of milliseconds to ensure a stable operation of the system. Slave or hot-standby DCGC instances simply receive and transmit the signals from the master and collect measurements from subsystems. In the event of a master failure, these instances seamlessly assume control based on a predefined priority protocol.



[58] Note there is no consensus on the need of separating communication between DCGCs and TSO grid control center by TSO zone. Some partners claim a separation of assets can be achieved by providing separated cards and communication channels, although the DCGCs do not belong to individual TSOs.

FIGURE 189: Implementation of single-stage architecture of DC grid control for the 4-terminal and 2-TSO DC system example.

Note the communication network topology between DCGCs depicted in the figure represents a simple point-to-point connection for simplicity, but in practice this communication network topology shall be redundant (ring, meshed etc.) to comply with high availability requirements. The same applies to the communication between DCGCs and subsystem controllers.

9.10.3.5 Two-stage architecture

The two-stage architecture primarily addresses the need to ensure compliance with separation of partners constraints. Furthermore, it seeks to standardize communication between controllers and converter stations while improving liability management within defined responsibility zones.

This DC grid control architecture relies fundamentally on the separation of control functions in two control levels: TSO DC Grid Controllers (TSO-DCGC) and Hub Controllers (HC). The first could be physically located in each TSO grid control center, whereas the second could be located in each converter station.

Accordingly, the control layer for the 4T-2TSO DC system is depicted in FIGURE 190. Note that the operation strategy adopted in this implementation of the architecture is also essentially functionally centralized, i.e. with one single instance of the controllers operating as master at each control stage of the DC grid operational layer. This means only one TSO-DCGC operates as master per HVDC system. Conversely, TSO-DCGCs from other TSOs operate as hot standby. Moreover, the sequential control is implemented in the TSO grid control center, but not in the TSO-DCGC. This aims to ensure only the TSO can operate switches within its zone. Additionally, there is no direct communication between a TSO-DCGC and subsystems of another TSO. The TSO-DCGC implement functions such as DC power flow computation, considering information about system topology, control modes and availability of systems and subsystems. This information shall be communicated either by the TSO grid control center or by the HCs. It serves as an intermediate interface for continuous control between the TSO grid control center and HCs. Any sequential control coordination is done in upper levels using the TSOs interface, which can include low speed communication between TSOs. PPM curtailment coordination is also deliberately left out of the controllers of such an architecture a priori because this topic has not been fully addressed by the 4GTSO working group yet.

Correspondingly, HCs serve as an intermediate between TSO-DCGC and all the subsystems for continuous control. They also distribute the measurements, setpoints and switches status and represent the interface between different TSOs on a system level. It is noteworthy that the Hub Controller of a TSO does not communicate directly with subsystems of other TSOs. However, HC do communicate with HCs of the other TSOs, sending setpoints to subsystems of other TSOs indirectly. This aims at complying with separation of partners requirements. From an operation strategy functional point of view, only one HC operates as master per HVDC system and other HCs (from same TSO and other TSOs) operate as slave or hot standby. The functions included in this control level are the control mode management, as well as eventually secondary control and N-1 contingency analysis. Consequently, the master HC is responsible for effectively coordinating these functions, while slaves HCs transmit signals to other controllers.

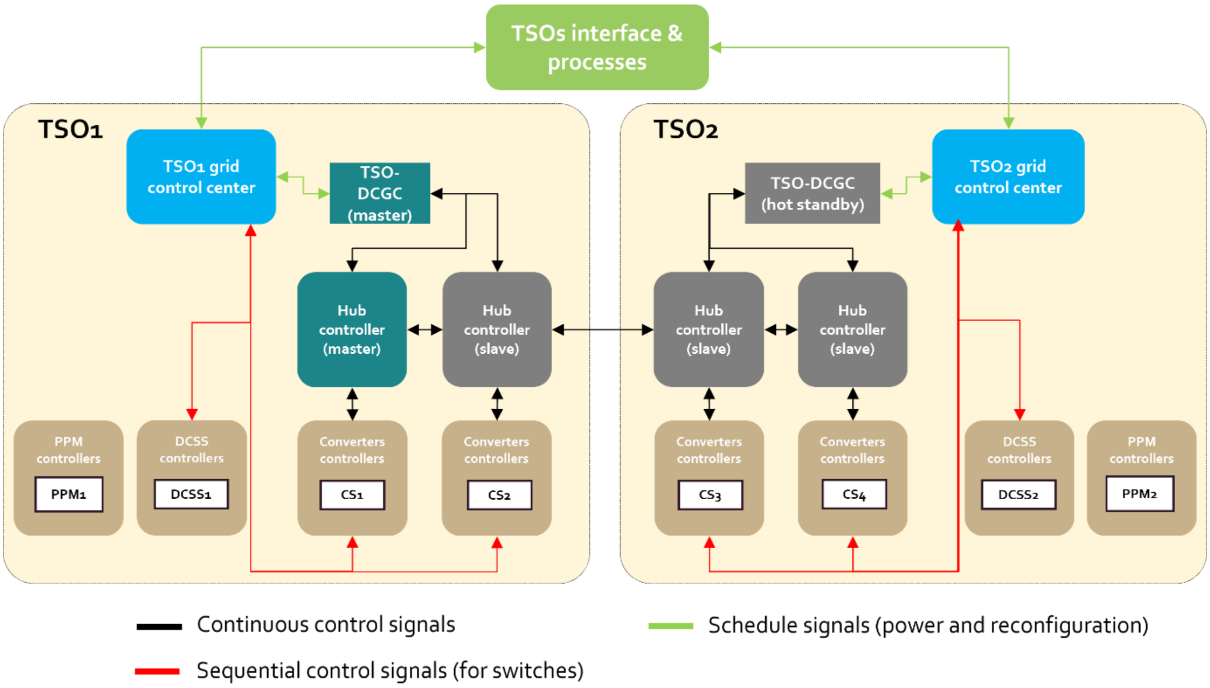


FIGURE 190: Implementation of two-stage architecture of DC grid control for the 4-terminal and 2-TSO DC system example.

Note the communication network topology between Hub Controllers depicted in the figure represents a simple point-to-point connection, but in practice this communication network topology shall be redundant (ring, meshed etc.) to comply with high availability requirements.

9.10.3.6 Functional view of DC grid control architectures

To summarize both architectures function implementation discussed so far, a schematic is depicted in FIGURE 191. The differences between these control architectures implementation can be summarized in the functions allocation in the layers and, consequently, exchanged signals.

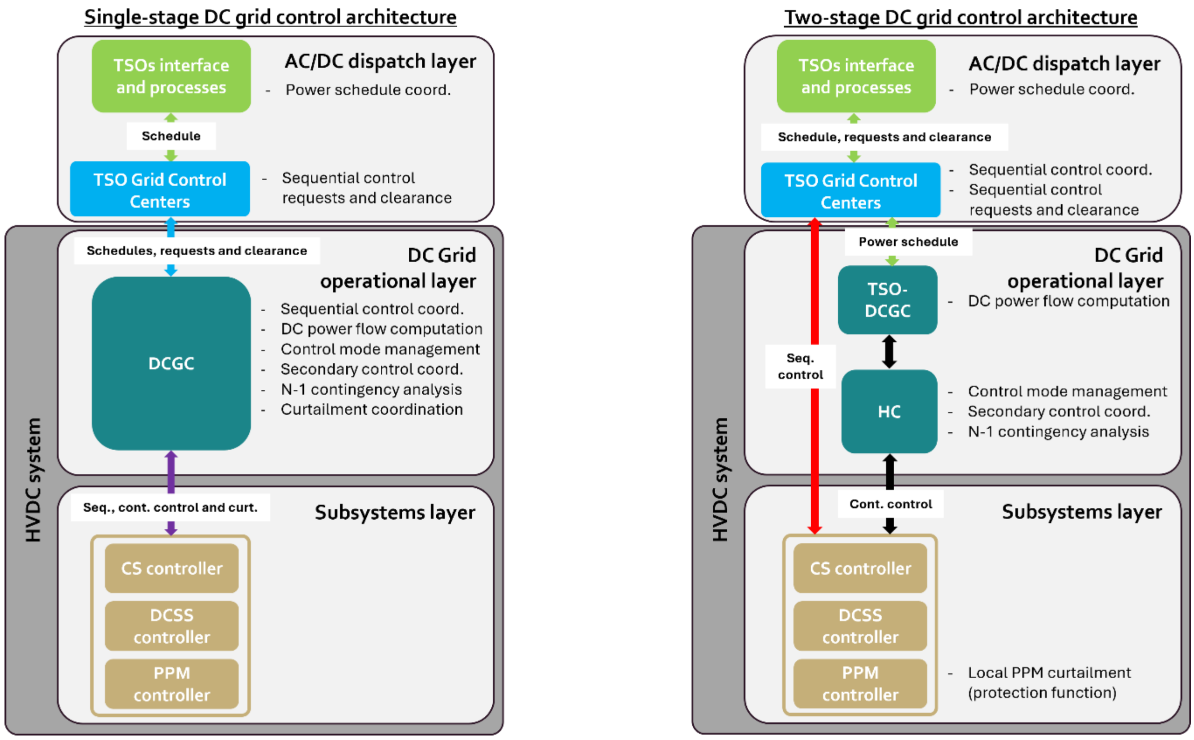


FIGURE 191: Functional assignment of DC grid control architectures implementation with single-stage and two-stage operational layer.

In the single-stage architecture implementation presented above, all types of signals are expected to be centralized in the DCGC, which communicates with basically every other control layer and also TSO zones. Meanwhile, the two-stage architecture implementation depicted above, proposed by the 4GTSO working group, specifically addresses the separation of partners constraints by keeping sequential control signals out of the scope of DC grid operational layer and being exchanged exclusively between TSO grid control center and subsystems.

In this sense, this single-stage architecture implementation uses DCGC to interface and coordinate TSOs sequential requests, while the two-stage implementation does not rely on fast communication but could rather rely on low speed communication to coordinate TSOs and communicate sequences such as reconfiguration, start-up, system split and so on. Moreover, by centralizing sequential control coordination, this single-stage architecture implementation can ensure a fast transition between safe states once the authorization is provided by the TSOs. On the other hand, the two-stage architecture implementation is unanimously recognized for its compliance with separation of partners constraints, avoiding any possibility of one TSO to control a switch out of its own TSO zone.

Moreover, the discussions in the workstream also highlighted different perspectives on the curative PPM curtailment coordination implementation. Indeed, although a potential need for some degree of curative curtailment coordination at the DC grid operational layer is rather acknowledged, the exact implementation of this is function was not fully addressed within the scope of 4GTSO working group and is therefore not detailed in this document for the two-stage grid control architecture.

Above all, it is important to note that the functional assignments and implementations described above are not the only possible solutions for these architectures. For example, alternative approaches could include a single-stage architecture designed to clearly comply with the separation of partners constraints.

In such a scenario, in the same way of the presented two-stage architecture implementation, sequential control coordination could be implemented in the TSO grid control center. As a result, sequential control signals are separated by TSO zones, with switches being operated only by the relevant TSO. The functional view of this alternative single-stage architecture implementation is illustrated in FIGURE 192 side-to-side to the two-stage control architecture previously presented.

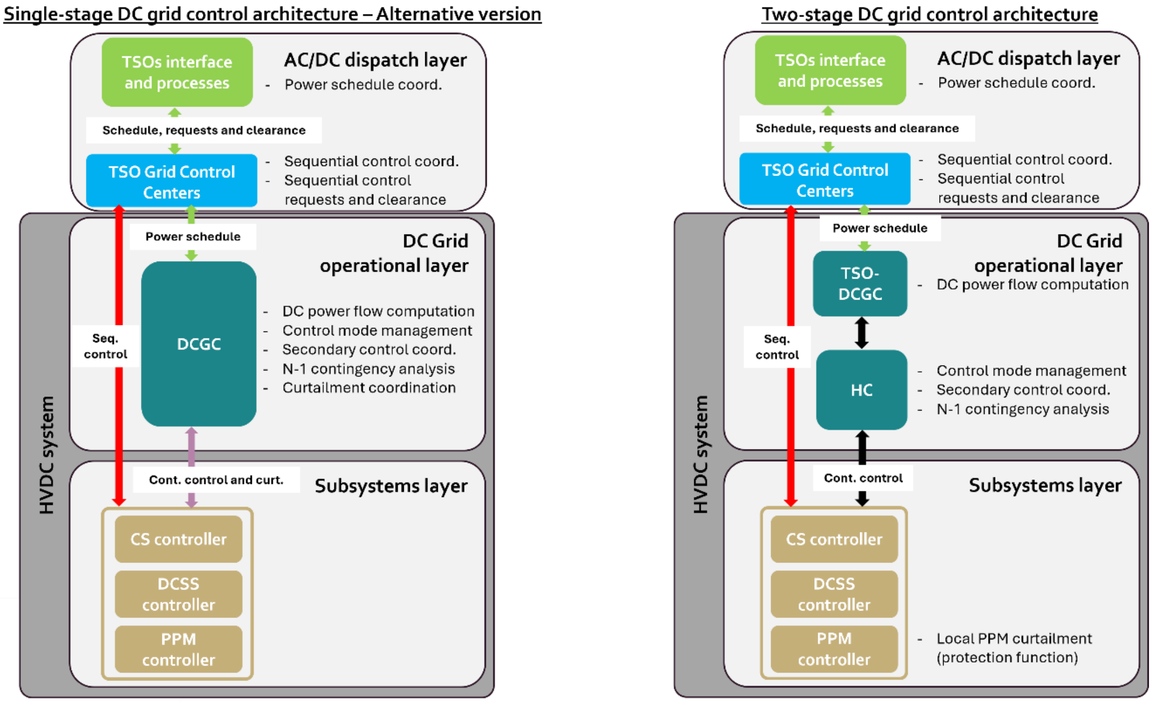


FIGURE 192: Functional assignment of DC grid control single-stage (alternative version) and two-stage architectures.

9.10.4 Concluding remarks

This section addressed some of the practical aspects of DC grid control implementation in the context of multi-TSO projects. The analysis revealed that the two architectures discussed share some structural similarities: both adopt a centralized operation strategy with a single master and are topologically decentralized. However, the allocation of functions across controllers and the exchange of signals can vary depending on the specific implementation of these architectures.

An important conclusion of the discussions is the acknowledgment of regulatory constraints related the separation of partners and their potential impact on the allocation of functions on different control layers and entities in the case of multiple TSOs in a project. Therefore, at the current state of the discussions, there are different views on whether the first option of single-stage DC grid control architecture implementation (see FIGURE 191) comply or not with the separation of partners constraints, specific to multi-TSO projects. In this architecture implementation, the separation is expected to be implemented rather software-based thanks to communication parametrization than fully hardware-based. On the other hand, there is a common understanding that the alternative version of the implementation of the single-stage architecture and the two-stage (see FIGURE 192) comply, a priori, with the separation of partners requirements.

A point that merits further investigation is the cycle time requirements for the different functions and how this could impact the function allocation in different controllers. Some participants of the workstream also highlighted stability issues could arise for high cycle time for the implementation of certain functions, such as DC power flow computation, especially during master/slave swap in decentralized hardware topologies where controllers are geographically far from each other.

In addition, in the discussions within the workstream some participants raised the risk of additional challenges that concern both system performance and safety related to implementing sequential control at the TSO grid control center. However, it is imperative to note that the choice of TSO responsibility zones must be carefully chosen to cope with these potential challenges, considering technical design choices related to both operation and protection of the system. Likewise, low speed communication between TSOs is acknowledged to have an important role to address these challenges, as it is necessary to coordinate sequential actions in the system.

More generally, it was noted that depending on the chosen control architecture, system operation responsibilities may shift between TSOs and vendors, a factor that should be carefully considered when defining the architecture and allocating functions.

Some other points have not been thoroughly addressed within the discussions in this workstream, such as the potential implementation of curative power curtailment coordination in the two-stage control architecture, and also expandability, cost and reaction time to contingencies for both control architectures. In the context of expandability, a key point for future discussions is understanding how different control architecture implementations can accommodate the connection of multiple hubs.

More generally, some other topics that could further be addressed revolve around the operation of an HVDC system. The operating states, as defined in the System Operation Guideline (SOGL), offer a baseline for such discussions. Among relevant questions are:

- Can the definition of the "Normal state" be limited to voltage ranges, or should a more complex approach based on online N-1 security be followed?
- What action shall be performed after entering an Alert state? What is the objective and scope of secondary voltage control?
- In which cases shall PPM curtailment be triggered? Which mechanisms, coordinated or local, may be relevant to perform such action?
- What are the available remedial actions, both preventive or corrective, that can be taken to ensure the security of the HVDC system?
- How can sequential control coordination at the DC grid operational layer enhance the operation and security of the HVDC system?

To conclude, a common understanding on DC grid control architecture constraints and choices has been achieved and the awareness about these topics is seen as sufficient to ensure that InterOPERA demonstrator results will be exploitable. We assess this workstream partially clarified the main points regarding DC grid control architecture, but that the points highlighted as open questions could benefit from reopening this workstream discussions later on the project.

9.10.5 Data and information security regulation

This subsection lists part of the data and information security regulation reviewed and considered in this workstream. Note this is not intended to be a complete list of all the possible regulation for HVDC grid control architecture.

TABLE 49: SECURE SYSTEM ARCHITECTURE

ID	Requirement text	Reference
Table 49.1	The system shall be developed in respect to safe operation.	
Table 49.2	The contractor shall name and explain all deviations from the specifications of this requirements definition listed below. Alternatives shall be proposed and discussed.	
Table 49.3	Where applicable and technically possible, network segmentation shall be realized by physical means to strictly separate systems of different functionalities and explicitly separate process and control systems from administrative functionalities. Tunnelling shall be avoided.	IEC62443-3-3 9.3.3.1 SR 5.1 RE 1 Physical network separation ISO/IEC 27019:2017 13.1.2 Security of network services BDEW-WP 2.0 4.4.2 Secure Network Structure ICS-Security Kompendium 2.2.6 Physical separation
Table 49.4	Segmentation shall not have an impact on operational functionality, nor shall it influence the independent functionality of the segmented zone. This includes preventing of uncontrolled or unintended transferring of information between segmentation zones.	
Table 49.5	In respect to vertical network segmentation, where applicable and technically possible, the underlying network structure of the system shall be divided into zones with different functions and different protection requirements. Where technically possible, these network zones shall be separated by firewalls, filtering routers or gateways. Communication with other networks must take place exclusively via communication protocols approved by the client in compliance with the applicable security rules.	
Table 49.6	In respect to horizontal network segmentation, where applicable and technically possible, the network structure on which the system is based shall also be divided horizontally into independent zones (e.g. by location), whereby the zones must also be separated by firewalls, filtering routers or gateways.	
Table 49.7	Communication between different security zones shall be encrypted. This communication shall explicitly not be wireless.	ISO/IEC 27019:2017 13.1.2 Security of network services BDEW-WP 2.0

ID	Requirement text	Reference
		4.4.1 Used Protocols and Technologies
Table 49.8	The telecontrol connection of the IT/OT components to the grid control centers shall be realized by dedicated gateway systems.	
Table 49.9	Defined events or messages shall be recorded and it shall be possible to feed them into a central evaluation system ("Security and Event Management" (SIEM)) of the clients.	ISO/IEC 27019:2017 12.4.1 Event logging BDEW-WP 2.0 4.5.6 Logging
Table 49.10	The Process Network shall not be able to communicate with the Internet.	ISO/IEC 27019:2017 5.1.1 Policies for information security BDEW-WP 2.0 4.4.1 Secure Network Structure
Table 49.11	The Process Network shall not have IP-based connectivity to external networks, nor shall it be connected to external or further client entities. External networks and entities cover all networks or entities, respectively, that do not belong to the same Transmission System Operator.	ISO/IEC 27019:2017 5.1.1 Policies for information security BDEW-WP 2.0 4.4.2 Secure Network Structure
Table 49.12	Control functions for controlling the critical infrastructure shall not be hosted in the cloud.	
Table 49.13	Remote access shall only be possible via centrally managed access servers under the control of the system operator. The access servers shall be operated in a DMZ and ensure isolation of the process network. A 2-factor authentication procedure must be used. Remote access shall be possible only for dedicated roles.	BDEW White Paper Version 2.0 4.4.4 Secure Remote Access
Table 49.14	File exchange shall only be permitted via a defined, specially protected storage area.	ISO/IEC 27019:2017 12.5.1 Installation of software on operational systems BDEW White Paper Version 2.0 4.7.3 Configuration and Change Management, Rollback
Table 49.15	A corresponding network zoning/segmentation concept shall be designed by the contractor. This concept shall be agreed on by the client.	Amprion NET-4
Table 49.16	The network zoning/segmentation concept shall include which information flow may take place between the network segments and how the network transitions are technically protected accordingly.	Amprion NET-5
Table 49.17	The transition between different network zones shall be designed according to their risk level. For example, the use of a "Packet Filter – Application-Level Gateway – Packet Filter" (P-A-P) structure can be appropriate for critical network transitions.	

ID	Requirement text	Reference
Table 49.18	When logically coupling process control systems and their associated communication links with external third parties (not belonging to the same Transmission System Operator), it should be ensured that only authorized communication and information flows, as well as operationally required control commands and messages, can be exchanged over the communication link.	
Table 49.19	When logically coupling process control systems and their associated communication links with external third parties (not belonging to the same Transmission System Operator), the nature and scope of the authorized communication, including the necessary control commands and the exchange of data and messages, shall be defined in advance.	

TABLE 50: REDUNDANCY

ID	Requirement Text	Reference
Table 50.1	The systems shall be designed as a redundant system, i.e. a single error in or a shutdown/unavailability of a system or a device – regardless of being virtualized or not – shall never result, directly or indirectly, in the loss of the intended function nor to a loss of the supervisory control and data acquisition capabilities of the DCMT system.	ISO/IEC 27019:2017 17.2.1 Availability of information processing facilities BDEW White Paper Version 2.0 4.1.1 Secure System Architecture
Table 50.2	After a system fault the system shall always enter a safe state.	
Table 50.3	The contractor shall provide proof of redundancy mechanisms.	ISO/IEC 27019:2017 17.2.1 Availability of information processing facilities BDEW White Paper Version 2.0 4.1.1 Secure System Architecture

TABLE 51: CONFIDENTIAL DATA

ID	Requirement Text	Reference
Table 51.1	Confidential data shall be stored and transmitted by means of encryptions.	ISO/IEC 27019:2017 10.1.1 Policy on the use of cryptographic controls BDEW-WP 2.0 4.1.5 Encryption of Sensitive Data ENCS SPR.01 Cryptographic Algorithms and Key Lengths

Table 51.2	The protection of confidential data shall include information security and the applicable data protection requirements.	

TABLE 52: TECHNOLOGIES, PROTOCOLS

ID	Requirement Text	Reference
Table 52.1	All virtual and physical devices shall support Radius, LDAP or TACACS communication for authentication of users, policies, reporting and network devices and shall be compatible for one or more of these protocols with the clients' Central authentication Systems.	ISO/IEC 27019:2017 9.1.2 Access to networks and network services BDEW White Paper Version 2.0 4.4.1 Used Protocols and Technologies
Table 52.2	All virtual and physical Network devices shall support communication to a Network Access-Control system that controls access, based on 802.1x. All virtual and physical communication-network devices shall enforce 802.1x, besides being able to act in client device.	ISO/IEC 27019:2017 9.1.2 Access to networks and network services BDEW White Paper Version 2.0 4.4.1 Used Protocols and Technologies
Table 52.3	All systems and components shall be protected against unauthorized or unintended system access or improper session handling. In addition to direct access, access via auxiliary applications must also be effectively prevented. This requirement shall also be explicitly applied to the delimitation of ownership and operational responsibility of the clients involved.	ISO/IEC 27019:2017 14.2.5 Secure system engineering principles
Table 52.4	All virtual and physical devices shall only use secure and state-of-the-art protocols for communication. Therefore the virtual and physical devices shall support only secure versions like (SSHv2, SNMPv3, TLS 3.0 , HTTPS etc.). Unsecure services shall be made possible to disable, without losing functionality.	ISO/IEC 27019:2017 9.1.2 Access to networks and network services 14.1.3 Protecting application services transactions BDEW White Paper Version 2.0 4.4.1 Used Protocols and Technologies 4.4.4 Secure Remote Access
Table 52.5	Web services shall be developed according to Application Security Verification Standard of OWASP at least level 2. For critical web services the client shall be able to demand an implementation on basis of level 3.	BDEW White Paper Version V2.0 4.5.4 Web Applications and Web Services
Table 52.6	In accordance with technical feasibility, only standardized IEC protocols shall be used in all areas. The contractor shall name all implemented protocols.	ISO/IEC 27019:2017 13.1.4 ENR – Securing process control data communication BDEW White Paper Version 2.0

ID	Requirement Text	Reference
		4.4.1 Used Protocols and Technologies
Table 52.7	The private area of these communication protocols shall only be used if technically necessary. Exceptions must be clearly documented and agreed upon with the employer.	ISO/IEC 27019:2017 13.1.4 ENR – Securing process control data communication BDEW White Paper Version 2.0 4.4.1 Used Protocols and Technologies
Table 52.8	If needed, only the OPC UA protocol version developed with security aspects in mind shall be used of the OPC system family.	
Table 52.9	Protocols using UDP as transport layer shall not be used. The following are exceptions to this: • PTP (Precision Time Protocol) • NTP / SNTP (Network Time Protocol / Simple Network Time Protocol) • SNMP (Simple Network Management Protocol, at least version 3) • RADIUS (Remote Authentication Dial In User Service)	BDEW White Paper Version 2.0 4.4.1 Used Protocols and Technologies
Table 52.10	All virtual and physical OT devices shall not implement wireless technologies. This does not apply to GPS/ DCF/ GLONASS.	ISO/IEC 27019:2017 13.1.3 Segregation in networks BDEW White Paper Version 2.0 4.4.5 Wireless Technologies
Table 52.11	The overall system shall have a uniform system time and offer the option of synchronizing this system time with an external, secure time source.	
Table 52.12	All virtual and physical devices shall support NTP protocol (version 4 or higher) to synchronize its internal clock.	ISO/IEC 27019:2017 12.4.4 Clock synchronisation BDEW White Paper Version 2.0 2.4.6 Logging, Audit Trails, Timestamps, Alarm Concepts. ICS-Security Kompendium 5.6.2 Securing of services and protocols
Table 52.13	All virtual and physical C&P and communication devices shall support the PTP protocol (version 2.1 or higher) to synchronize its internal clock with high precision according to IEC61850-9-3.	ISO/IEC 27019:2017 12.4.4 Clock synchronisation BDEW White Paper Version 2.0 2.4.6 Logging, Audit Trails, Timestamps, Alarm Concepts. ICS-Security Kompendium 5.6.2 Securing of services and protocols
Table 52.14	Failures in the availability of the time signal or external time synchronization shall have no or only well-defined	

ID	Requirement Text	Reference
	effects on control functions. If necessary, a redundant time source shall be provided.	
Table 52.15	The system shall support logging of all security-related actions, events and faults in a suitable format. The logged data shall be archived.	IEEE1686 6.11 Storage for records IEC62443-3-3 12.4.2 Protection of log information ISO/IEC 27019:2017 12.4.1 Event logging 12.4.2 Protection of log information BDEW White Paper Version 2.0 4.5.6 Logging ENCS SLR.02 Storage Space for Security Events ICS-Security Kompendium 5.6.10 Logging and analysis.
Table 52.16	All virtual and physical C&P devices shall monitor safety- and security-related activity and make the information available through a (real-time) communication protocol for transmission to a Supervisory AND (separate) Monitoring system. All virtual and physical devices shall support both the IEC 103/104/61510/… and SNMPv3 at the same time for these security-related events.	ISO/IEC 27019:2017 13.1.1 Network controls BDEW White Paper Version 2.0 4.4.1 Used Protocols and Technologies
Table 52.17	All virtual and physical communication devices shall support a SNMP communication to a centralized network management system with the full FCAPS function.	ISO/IEC 27019:2017 13.1.1 Network controls BDEW White Paper Version 2.0 4.4.1 Used Protocols and Technologies
Table 52.18	The authenticity and integrity of process data, whose falsification in the direction of reporting or command can directly or indirectly lead to mismanagement in plant or network operations, shall be cryptographically secured based on a risk analysis.	ISO/IEC 27019:2017 14.1.3 Protecting application services transactions BDEW White Paper Version 2.0 4.4.1 Used Protocols and Technologies
Table 52.19	To ensure the authenticity and integrity of process data, whose falsification in the direction of reporting or command can directly or indirectly lead to mismanagement in plant or network operations, either security extensions at the application protocol level	ISO/IEC 27019:2017 14.1.3 Protecting application services transactions BDEW White Paper Version 2.0

ID	Requirement Text	Reference
	(e.g., according to IEC 62351) or securing data transmission at lower network levels shall be used.	4.4.1 Used Protocols and Technologies

TABLE 53: DOCUMENTATION AND WORKING GUIDELINES

ID	Requirement Text	Reference
Table 53.1	The system shall be developed by reliable and trained employees using a secure development process, including quality management. Potential subcontractor must be subject to at least the same safety requirements as the contractor.	ISO/IEC 27019:2017 14.2.1 Secure development policy BDEW White Paper Version 2.0 4.6.1 Secure Development Standards, Quality Management and Approval Processes ENCS SUR.03 Secure Coding Practices
Table 53.2	Access to insecure networks shall not be possible from the development/test systems.	
Table 53.3	The development environment as well as the test systems shall be provided with secure logical access protection and protected against unauthorized physical access.	
Table 53.4	The documentation of the entire system shall always be kept up to date throughout the entire project.	
Table 53.5	The documentation shall define the following security-relevant development steps: Definition of security requirements Threat modelling and risk analysis Derivation of requirements for system design and implementation The processes and procedures as well as the corresponding results of the above-mentioned development steps shall be documented in a comprehensible manner and can be viewed by the client on request.	
Table 53.6	The documentation shall include a concept for administration of all virtual and physical network devices.	
Table 53.7	The documentation shall include relevant emergency and crisis scenarios containing procedures and recovery plans.	
Table 53.8	Out of these scenarios, the documentation shall explicitly describe the consequences on functions of the system or devices in case of a system split.	
Table 53.9	The documentation shall include consequences of incorrect configuration of the system.	
Table 53.10	The documentation should include vulnerability management process and a patch management process.	ISO/IEC 27019:2017 12.6.1 Management of technical vulnerabilities

ID	Requirement Text	Reference
		BDEW White Paper Version 2.0 4.7.4 Handling of Vulnerabilities ENCS SDR.04 Vulnerability Handling Process
Table 53.11	The documentation should include description for malware protection system and the management processes for actualizing this system. The system shall be integrable without any impact on the system. It should be described how a centralized system can manage the malware protection system.	IEC62443-3-3 7.4 Protection against malware ISO/IEC 27019:2017 12.2.1 Controls against malware BDEW White Paper Version 2.0 4.3.2 Malware Protection ICS-Security Kompendium 3.3.11 Malware
Table 53.12	The decision-making process for design questions shall be documented including descriptions of its advantages and disadvantages.	
Table 53.13	The documentation shall include all side agreements and changes until the handover of the system.	
Table 53.14	The documentation for networks, network services, and network components shall include the following: • Requirements for the network, network service, and network component • Security functions • Hardening measures • Responsibilities • Processes • Network/zone concept with resulting segmentation • Monitoring	