MULTI-TERMINAL MULTI VENDOR HVDC GRID DESIGN STUDIES - PART II: DYNAMIC STUDY

Julien Pouget[1] , Carmen Cardozo[1], Pierre Rault[1], Sébastien Dennetière[1]*

[1]*Electromagnetic Transients and Power Electronics, RTE, 2119 avenue Henri Schneider, 69330 Jonage, France*
**julien.pouget@rte-france.com*

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Abstract

Multi-Terminal (MT) HVDC networks have been studied for over a decade, with recent efforts increasingly focusing on enabling multi-vendor interoperability to support a competitive and scalable deployment framework. Concurrently, protection selectivity is receiving renewed attention in the context of large-scale offshore connections based on 2 GW bipolar building blocks, where the maximum loss of infeed has become a critical planning constraint. This three-part series addresses early-stage system-level studies of MT HVDC grids using generic models, which are essential to support primary design. As part of the InterOPERA project, involving HVDC vendors traditionally responsible for DC-side design in point-to-point schemes, a methodology is proposed to refine, and eventually instantiate, project-specific technical requirements at the DC point of connection of AC/DC converters. This second part focuses on dynamic studies, quantifying maximum DC voltage excursions resulting from single and bipole outages, as well as temporary loss of power caused by converter blocking and grid-side AC faults. The variability of these excursions is examined as a function of two key design parameters: AC/DC converter reactor sizing and control settings. Time-domain simulations reveal that relatively higher stresses observed at one location are caused by large oscillations triggered by a specific blocking event. Frequency-domain assessment provides further insight into the underlying resonance phenomena.

1 Introduction

Driven by the increasing scale of Offshore Wind Farms (OWFs) and the growing need for greater cross-border interconnection capacity, bipolar High Voltage Direct Current (HVDC) systems based on Modular Multilevel Converter (MMC) technology are expected to play a key role in future transmission networks. However, concerns regarding the techno-economic feasibility of relying exclusively on Point-to-Point (P2P) links have prompted the industry to address the challenges of transitioning to Multi-Terminal (MT) grids.
In this context, the InterOPERA project was launched to enable future HVDC systems from different suppliers to operate together, paving the way for the actual implementation of Europe's first MT, Multi-Vendor (MV), multi-purpose HVDC projects. InterOPERA has already achieved several key milestones, including the development of common functional specifications [1] and minimum interface requirements [2].
A Real-Time (RT) demonstrator is currently being deployed to validate and refine the proposed methods and processes, ensuring their practical applicability. This work focuses on activities supporting the implementation of the RT demonstrator, particularly HVDC grid design studies using vendor-agnostic generic models, that provide input to detailed subsystem specifications. Three study packages were defined, with key findings presented in this three-paper series:

- The first part establishes preliminary settings for the static characteristics of the continuous and limited DC Voltage Sensitive Modes (DCVSMs) [1], namely droop gains and boundaries for the normal (secure) operating range, derived from a DC Load Flow (LF)-based contingency analysis [3].
- This second part examines **dynamic** stresses at the DC Point-of-Connection (DC-PoC) of various subsystems during the primary control response to selected contingencies.
- The third and final part addresses DC short-circuit currents and Temporary Overvoltage (TOV) during DC faults [4].

1.1 Background on the InterOPERA Technical Specifications

As proposed in [5], the InterOPERA demonstrator adopts a bipolar configuration rated at 2 GW per converter station (1 GW per pole). The detailed technical specifications [6], developed jointly by project stakeholders, introduce new DC-side requirements; most notably DC voltage operating ranges and primary DC voltage control specifications in line with [1]. Additionally, dedicated system design studies were conducted to establish appropriate numerical values for these requirements as applied to the InterOPERA demonstrator.
Specifically, dynamic performance requirements for the primary DC voltage control are expressed in terms of characteristic indicators such as rise time, settling time, response time, and overshoot. These apply to **individual subsystems**, namely AC/DC converter stations, with compliance verified through standalone tests using well-crafted grid equivalents [1].
When considering grid-connected investigations, three types of studies must be distinguished:

- HVDC grid design studies with generic models; the focus of this work;
- Control development within detailed **subsystem design** and the Original Equipment Manufacturer (OEM) scope; and
- Interaction studies conducted at the integration stage using vendor models [7].

1.2 InterOPERA HVDC Grid Design Studies – Dynamic Part

HVDC grid dynamic design studies characterise temporary excursions of key electrical quantities, namely DC voltage, current, and power, across subsystems within the *dynamic* timeframe, i.e., prior to secondary control action. The resulting dynamic bands are then specified as minimum operating ranges for all DC-connected subsystems to prevent inadvertent protection operation following selected contingencies.
Although beyond the formal scope of design studies, standalone tests were conducted on the generic model used in this work to provide *indicative* values for compliance verification; these are omitted here for brevity (refer to [6]).
As introduced in the first part of this series [3], the conventional boundary between dynamic and transient design studies becomes less distinct in MT topologies with fault-handling capabilities, since parts of the system must withstand DC faults. In InterOPERA, a separation was drawn based on the type of simulated event to manage workload, while recognising that a comprehensive and iterative approach remains necessary in practice. The contingency list includes single and bipole infeed/export losses. In practice, these disturbances may result from terminal (one pole) or station (both poles) outages, as well as AC faults. Permanent outages may be modelled through forced converter blocking followed by tripping, which, for the **affected** unit, constitutes a *transient* event.
This work focuses on the dynamic response of **surviving** units during outages (affected converter excluded), while also considering the affected unit in cases of properly cleared AC faults, since return to normal operation is the expected.
The contributions of this paper are threefold:

1. A general methodology is proposed for conducting HVDC grid **dynamic** design studies using generic models.
2. Its application to the InterOPERA demonstrator setup provides insight into the expected stress levels in such systems.
3. A parametric analysis highlights the result sensitivity to assumptions on subsystem design parameters, falling within the OEM scope and uncertain during early-stage studies.

Section 2 describes the proposed methodology and key modelling assumptions. Sections 3 and 4 present simulation results, starting with Time-Domain (TD) responses for a representative case and then quantifying DC voltage excursions across all predefined scenarios. The influence of AC/DC converter smoothing reactor sizing and control settings is examined. Section 5 complements the TD results with a Frequency-Domain (FD) assessment of the observed oscillatory behaviour, arising from resonance phenomena. Finally, Section 6 concludes with the derived DC voltage operating ranges and further generalises them by exploring alternative system configurations.

2 Assumptions, Methodology and Modelling

The detailed HVDC grid design study task included an assumption alignment phase involving subsystem vendors to refine the demonstration scope and establish relevant generic parameter values.

A Three-Terminal (3T) base case, shown in Fig. 1, was defined, comprising three AC/DC converters, without upfront assumptions on whether stations are onshore or offshore, and four DC Switching Stations (DCSSs). Only the North-West (NW) and the central DCSS (#1 and #5) are equipped with DC Circuit Breakers (DCCBs). Three configurations were investigated:

- GGG: all three AC/DC converter stations connected to asynchronous onshore grids;
- GGW: one station (North-East (NE)) connected to an OWF;
- WWG: only one onshore station (NE, outage excluded).

For brevity, results in this paper are limited to the GGW case.

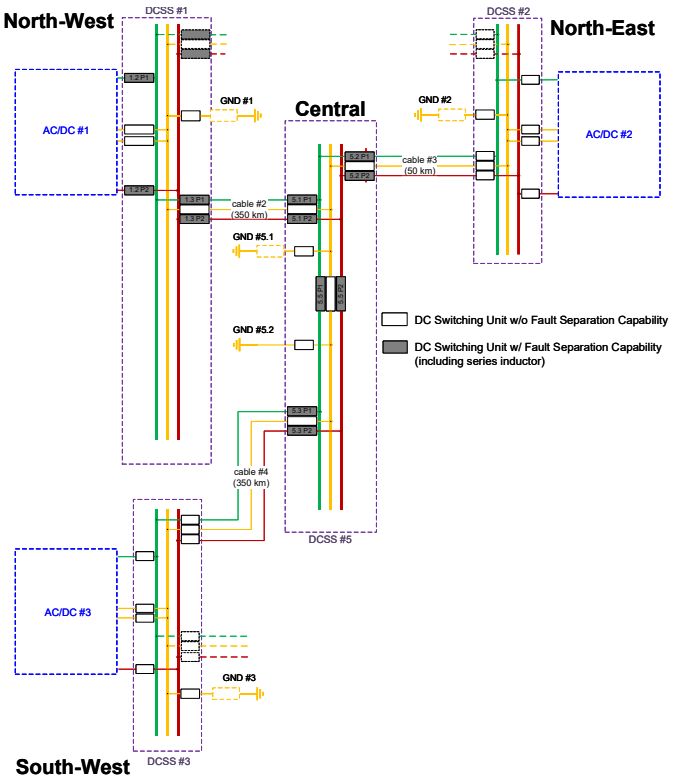

Fig. 1. InterOPERA Demonstrator 3T DC grid topology

2.1 Key Assumptions for Dynamic Design Studies

System dynamic behaviour strongly depends on the modelling assumptions applied to both the DC grid and the connected devices, notably AC/DC converters. Considerable effort was therefore devoted to parameterising the 3T base case generic model to ensure a *realistic* dynamic response.
That said, the underlying choices represent **study assumptions** and are not intended for *direct* adoption in technical specifications, as design parameters, including control strategies, remain within the scope of OEMs and cannot be prescribed. Accordingly, requirements must remain functional to preserve vendor competition. While no guarantee can be provided at this stage, there is reasonable confidence that proprietary solutions will outperform the generic model used in the InterOPERA HVDC grid studies, rendering the results conservative and therefore suitable for system design purposes.

However, although conservatism in input assumptions is necessary to accommodate the diversity of independently optimised technical solutions from OEMs, it is equally important to avoid overdesign. To that end, conservative assumptions should remain within plausible bounds and must not result from the compounding of uncorrelated worst-case scenarios.

2.1.1 Key design premises: from the DC LF study [3]:

- For simplicity, a single cable dataset is used [8].
- The continuous operating range is defined as ±5% of the nominal DC grid voltage ($V_{DC,Nom}$), set at 500 kV. Accordingly, the maximum continuous operating voltage is 525 kV (1.05 pu, with $V_{DC,Base} = V_{DC,Nom}$).
- The system must remain within Operational Security Limits (OSLs), defined as the continuous operating range, **after** the primary DC voltage control response (only considered remedial action) for predefined contingencies (see Fig. 2).
- Only onshore stations participate in DC voltage regulation; OWFs and Dynamic Braking Systems (DBSs) are excluded. Although both could be integrated into future primary control schemes, practical constraints, such as curtailment speed limits and immature DBS coordination, currently limit their use as emergency measures (for OSL violation).
- Offshore stations operate in VF mode, which from the DC-side perspective corresponds to a constant-power mode.
- DC voltage control is implemented pole-wise using a multi-slope droop-type controller based on pole-to-neutral quantities when multiple onshore stations are considered. In WWG, the onshore station (NE) operates in fixed DC voltage control mode. No local balancing strategy is applied.

Specifically, two types of DCVSMs are considered in line with [1]. Both employ the classical droop equation (1) but operate within specific bands and apply dedicated settings (s_i):

$$p_{DC} = P_{DC,0} + \frac{1}{s_i}(V_{DC,0} - v_{DC}) \quad (1)$$

- DCVSM operates under normal conditions to maintain continuous power balance and regulate the DC voltage while distributing the control effort across participating units.
- Limited DCVSM (LDCVSM) provides stronger DC voltage support when the voltage approaches OSLs, typically during severe disturbances that create large power imbalances.
- Power and voltage setpoints ($P_{DC,0}$, $V_{DC,0}$) are, in practice, provided by the DC Grid Controller (DCGC).

Key outcomes from Part I [3] highlighted the need for configuration-specific settings in the GGW case, which exhibited the narrowest margins when enforcing the design criteria. These settings are illustrated in Fig. 2. An initial secure operating range is proposed at [487.5, 505] kV ([0.975, 1.01] pu) and applied to all AC/DC converter stations, with the following preliminary parameters for primary DC voltage control:

- DCVSM droop gain (s_1) set to 10%; and
- LDCVSM droop gain ($s_{2,u} = s_{2,o}$) set to 1%.
- Thresholds for the limited modes ($V_{DC,1u}$ and $V_{DC,1o}$) aligned with the secure operating range boundaries ([0.975, 1.01] pu), with the knee points *sliding* along these limits as the operating point varies.

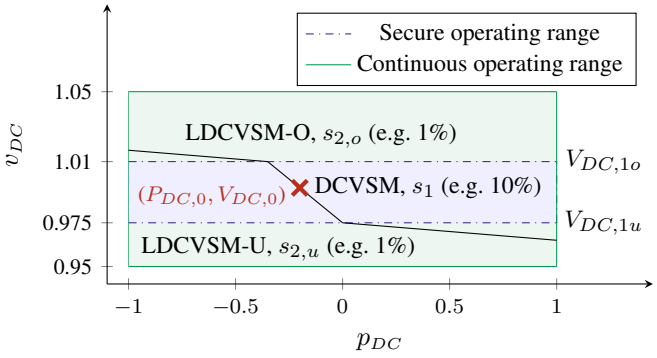

Fig. 2 Continuous and secure operating ranges and DCVSMs slope differentiation in the p_{DC}-v_{DC} plane (GGW case)

2.1.2 Onshore AC Grid: to limit study scope, InterOPERA grid design studies focused on DC-side dynamics, representing onshore AC-sides by Thevenin equivalents under strong-grid assumptions, which lead to maximum transient stresses (refer to Part III – Transient Study [4]). In the general case, weak grid conditions should also be investigated, as they may prove critical for control tuning and overall system stability.

2.1.3 Offshore Grid and Wind Power Plants (WPPs): in InterOPERA, four 500 MW WPPs per bipole are considered, represented here by aggregated generic models. Each WPP connects to one of the two transformers per pole at the offshore converter. The offshore grid operates at 66 kV.

2.1.4 DC Switching Unit Reactor: although detailed modelling of DCCBs is not required for dynamic studies, DC Switching Units (DCSUs) equipped with DCCBs typically include reactors to limit the rate of fault current rise, which significantly impacts system dynamic behaviour [9]. In this work, generic values are adopted, with **200 mH** for the inductance and **100 mΩ** for the resistance. The resistance is deliberately chosen lower than in DC LF-based design studies. While selecting upper-bound values is conservative for voltage drop estimation, it tends to increase system damping in dynamic studies, potentially yielding overly optimistic results. In the absence of a dedicated sensitivity analysis, the extent to which these effects balance out or affect the results remains uncertain.

2.1.5 AC/DC Converter Reactors: similarly, arm inductance (L_{arm}) and smoothing reactor size (L_{DC}) are important parameters. Depending on technology-specific current capabilities, OEMs may need to select relatively high values in the MT context to comply with emerging DC-Fault Ride-Through (DC-FRT) requirements (see Part III - Transient Study [4]). Here, a single value of **35 mH** is used for the arm inductance, while the DC-side smoothing reactor is varied across three values: **10, 150, and 300 mH**, to assess sensitivity.

2.1.6 Dedicated Metallic Return (DMR) temperature assumption: under normal (bipolar) operation, the DMR current is expected to remain near zero, keeping its temperature relatively low. In this study, a value of 20 °C (7.21 mΩ/km) is assumed. This revises the assumption used in DC LF-based design studies, where the DMR was set to 70 °C (as for the pole conductor) to represent a worst-case scenario for voltage drop under asymmetrical post-contingency steady-state operation.

2.1.7 AC/DC Converter Control: this work adopts a classical Grid-Following (GFL) control scheme, even though InterOPERA also includes the demonstration of Grid-Forming (GFM) capability. The choice is primarily motivated by the lack of well-established generic dynamic models for GFM HVDC converters and is further justified by the strong onshore grid assumptions adopted in this study. In practice, GFM introduces stronger dynamic coupling between the DC and AC sides, potentially altering both the impact of AC contingencies on the DC system and the performance of DC voltage control, depending on implementation. Consequently, excluding GFM from the system design phase increases interoperability risk at later stages, which are expected to be mitigated through appropriate control tuning during integration. That said, there is currently insufficient evidence to rule out the possibility that these combined effects could impose greater subsystem stresses than those observed under GFL assumptions, potentially requiring additional primary design margins. Beyond the choice of synchronisation scheme, other control loops, particularly DC voltage and energy controls, play a decisive role in dynamic performance and, therefore, in DC voltage excursions. This work assesses changes in DC voltage envelopes resulting from two control-setting variants, *Ctrl_reducedVdc* and *Ctrl_reducedEn*, relative to the base case (*Ctrl_initial*), further detailed in Appendix A.

2.1.8 OWF Curtailment and DBSs: DBSs are designed to temporarily absorb surplus energy when export to the AC grid is not possible. In InterOPERA, one DBS per pole, connected to the neutral, is considered at onshore stations only; however, they are excluded from this work. For the 3T topology and all listed contingencies, sufficient inherent active power headroom is available to adjust power flows without resorting to OWF power curtailment. Furthermore, the primary DC voltage control settings have been specifically configured to maintain DC voltages within the OSL in the post-contingency steady state. As a result, *permanent* activation of DBSs (within their energy ratings to support OWF curtailment) is not anticipated. In practice, DC voltage dynamics may trigger *temporary* DBS activation, depending on the coordination strategy and parameterisation. Such activation should support voltage control, mitigate DC voltage excursions, and thereby reduce subsystem stress. Consequently, excluding DBSs from dynamic operating range quantification can be considered a conservative assumption suitable for system design purposes. However, potential adverse interactions between DBS operation and converter DC voltage control should be thoroughly evaluated in practice, particularly in alternative topologies such as 4T configurations.

2.1.9 Inputs from the Insulation Coordination Study: this paper presents the final results using the same model as for the transient study, i.e., with the neutral system grounded at the central DCSS (#5) via a **5** Ω resistor and considering surge arresters (refer to [4]). Generally, these parameters have limited impact on the dynamic study and, along with other simplifications, may initially be neglected as a first approximation. Although it has been common practice to conduct transient studies before dynamic ones, the InterOPERA HVDC grid design studies were carried out in reverse order; an approach that may become increasingly relevant in the context of MT grids. However, iterative coordination between both studies remains necessary.

2.2 Modelling Considerations for Dynamic Design Studies

The 3T base case model was implemented in EMTP®. This section provides relevant details for dynamic investigations.

2.2.1 AC/DC converters: are modelled using the generic MMC model available in EMTP® [10], specifically the Average Arm Model (AAM) variant (model #3 in [11]), which offers a balance between accuracy, complexity, and computational efficiency, even during blocked states, for studies based on generic models. For InterOPERA, a bipolar configuration was developed by connecting two identical MMCs, where the negative terminal of the positive converter pole and the positive terminal of the negative converter pole are connected to the DMR. Each terminal is controlled independently via a hierarchical control structure with classical upper- and lower-level layers [12]. Protection functions are disabled for dynamic analysis to assess the magnitudes of observed quantities under characteristic disturbances. The multi-slope droop control is implemented by inserting a reference calculation ($v_{dc,ref}$) upstream of the classical PI-based DC voltage control loop. Different droop gains, as introduced in Fig. 2, are applied depending on the operating condition (i.e., the DC voltage range). The specific implementation, shown in Fig. 3, uses a variable active power knee point, $\Delta P_{1o/u}(t)$. Inputs include DC voltage and power setpoints ($V_{DC,0}$ and $P_{DC,0}$), as well as active power measurement filtered at 10 Hz. The resulting DC voltage reference is constrained within the continuous range ([0.95, 1.05] pu). In practice, behaviour beyond the OSL is not specified [6], allowing OEMs to implement different solutions for the DC voltage and power limiting modes (DCVLM and PLM as defined in [1]).

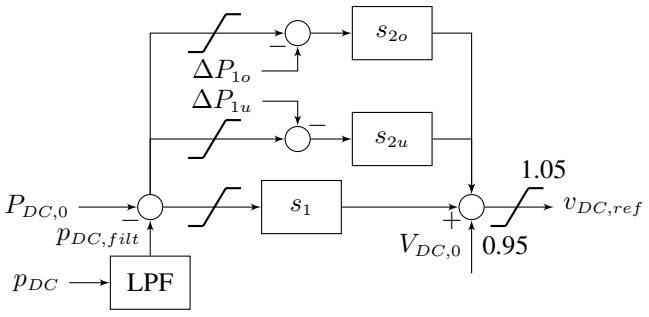

Fig. 3. Schematic representation of the droop implementation

When applied to highly inductive DC grids, the publicly available MMC control architecture, originally designed for P2P links, exhibited oscillatory behaviour. To improve damping and robustness, an energy-based control loop was incorporated, following established literature practices [13]. In addition, the DC voltage control point was relocated upstream of the DC-side inductance, while performance evaluation at the converter remained focused on the DC-PoC, as shown in Fig. 4. In the base case control settings (*Ctrl_initial*), the DC voltage control gains were set to $K_p = 8$ and $K_i = 200$, with the DC voltage reference limit fixed at 1.3 pu. In the *Ctrl_reducedVdc* variant, these gains were reduced to 4 and 100, respectively, while in the *Ctrl_reducedEn* variant, the reference limit was lowered to 1.2 pu (see Appendix A). Minor additional adjustments, such as implementing a current-limiting function in VF mode at the offshore station, were introduced to enable AC fault analysis, while preserving the model's generic nature.

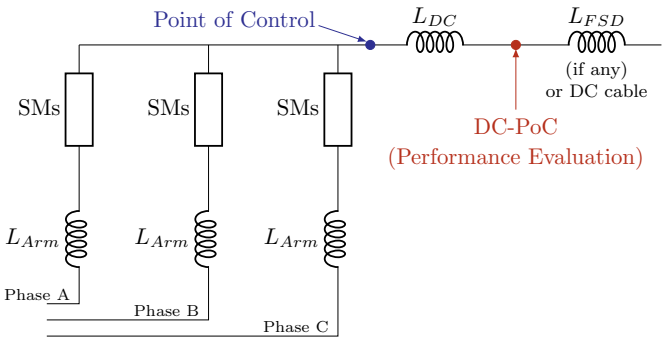

Fig. 4. DC-PoC and point of control definition

2.2.2 DC Grid – DC Cables: a submarine cable with sheath, armour, and XLPE insulation is considered [8], modelled using a wide-band approach that captures the frequency dependency of cable parameters as well as the mutual coupling between the core and both the screen and armour conductors [14]. Resistance values are defined based on temperature assumptions. The same cable model is also used in Part III [4].

2.3 Scenario Definition

For the GGW configuration, eight initial operating conditions (N situations) were defined based on the DC LF-based contingency analysis [3]. These include full-power import, full-power export, and near-zero power at different DC voltage levels for the onshore stations (NW and South-West (SW)), while only the latter two conditions apply to the offshore station (NE), as inverter operation is not relevant in this case. On the AC side, a coupled busbar configuration is considered for the onshore stations, whereas a decoupled busbar arrangement is assumed for the offshore station. The Contingency List includes:

- Six possible outages, covering both terminal and station outages, for each N situation, resulting in a total of 48 (6×8) scenarios simulated for each variant of subsystem settings.
- Solid three-phase AC faults are also simulated, as the resulting temporary power loss is perceived by the DC grid as contingencies equivalent to outages within the dynamic time frame (≈ hundreds of milliseconds). The fault duration is set to 100 ms, which is typical for transmission grid fault clearing times. Given AC side topology assumptions, AC faults on the onshore side lead to bipolar disturbances, whereas faults on the offshore side affect only one pole.

2.4 Key Performancce Indicators (KPIs)

Although verifying subsystem performance requirements is not the primary objective of design studies, inadequate representativeness of generic models can significantly affect the recorded dynamic DC voltage and current excursions, potentially imposing unnecessary constraints on equipment. To mitigate this, the behaviour of the generic model was verified to ensure realistic results. This assessment must be conducted across a wide range of operating conditions, modes and event types, making classical evaluation by visual inspection of TD signals unsuitable. Instead, KPIs are reported in an aggregated manner alongside the identified dynamic stresses, confirming that these stresses are not unduly influenced by overly restrictive design assumptions or limitations of the generic model.
In this work, dynamic performance is characterised by adapting two KPIs defined in IEC 61400-21 [15]:

- Settling time: *elapsed time from the start of a step change event until the observed value continuously stays within the predefined tolerance band of the target value*.
- Overshoot: *difference between the maximum value of the response and the steady-state final value*.

When characterising step responses, the tolerance band is typically expressed as a percentage, often 5% or 10%, of the nominal value. This approach, however, is poorly suited to quantifying DC voltage recovery following disturbances, as variations often remain below 5% of nominal. In this work, **fixed tolerances of 1 kV and 50 A** are adopted, enabling meaningful comparison across different scenarios. Box plots are used, where the box represents the interquartile range (±25%), and the whiskers extend to the 5th and 95th percentiles. Similarly, overshoots are reported in SI units, as the final state may be close to zero depending on the simulated scenario. To characterise dielectric stress exposure, time-dependent profiles are proposed; these are DC-TOV-*like* representations that capture both temporary overvoltage and undervoltage excursions. The proposed KPI, termed Absolute Time (AT) outside OSL, represents the maximum time required to permanently return within the DC voltage continuous operating range. As illustrated in Fig. 5 for a selected case, different points on the curve indicate the duration spent beyond specific DC voltage thresholds, starting from its first breach. It must nonetheless be noted that the final envelopes do not represent individual, physically measured voltage trajectories but rather the maximum durations recorded above each discretised voltage level across all scenarios. Depending on the converter design, values at the lower end of the envelope may lead to short periods of over-modulation, but must not trigger protective blocking of the converter [6].

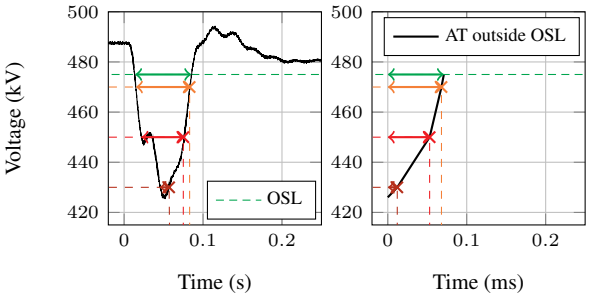

Fig. 5. AT outside OSL for $V_{DC,NW}$, SW → NW, outage SW

For brevity, Section 3 focuses on outages caused by forced converter blocking (followed by tripping), while results in Section 4 are limited to AC faults. However, the specified operating ranges cover both event types, as summarised in Section 6. Generally, the affected unit experiences the largest disturbance and is included in range quantification only for AC faults (excluding converters that trip, which represent the affected unit for the outage study). It will be shown that, as a result, AC faults impose the more stringent constraints. While it may be premature to generalise, this suggests that focusing solely on AC faults could suffice for dynamic design considerations.

3 Results for Various DC Inductance Values

This section presents a sensitivity analysis of dynamic performance and stresses for varying AC/DC converter DC reactor values. Section 3.1 illustrates the TD system response for a representative scenario. Section 3.2 evaluates overall system performance following outages across all GGW scenarios, while Section 3.3 quantifies the resulting DC voltage excursions.

3.1 Onshore converter blocking (outage) example

Fig. 6 shows the DC voltage and current at the converters' DC-PoC following the single outage of the NW negative pole. In this scenario, the OWF connected at NE converter injects full power (2 GW), initially exported to the NW AC grid, while SW compensates for system losses.

After the NW converter blocks and is disconnected from the DC grid, SW permanently assumes full power export on its negative pole toward the AC grid according to its primary DC voltage control settings. As noted earlier, the blocking event causes a large di/dt, leading the affected converter to experience a transient peak voltage of up to 800 kV, depending on the reactor size. This peak lasts only a few milliseconds and belongs to transient assessment. The system then settles to its new operating point within the OSL in approximately 150 ms, meeting the design criteria. In the surviving units the dynamic response varies slightly with on the applied smoothing reactor.

3.2 System Performance Evaluation

DC voltage settling time and overshoot at the surviving units can be determined from TD signals. Aggregated results for all GGW scenarios are presented in Fig. 7, illustrating that the

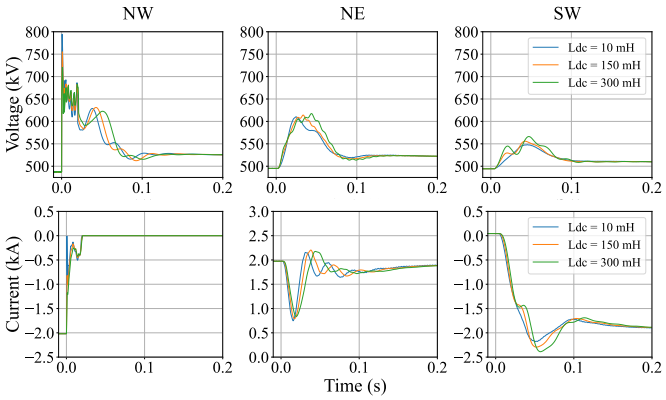

Fig. 6 NW (Left), NE (Middle), SW (Right). Unit outage at NW. Affected pole: DC voltage (Top), DC current (Bottom)

generic control exhibits good robustness across varying operating conditions and events. Nonetheless, settling times tend to increase with larger values of the DC smoothing reactor. Overshoot shows a less consistent trend, tending to increase at NW and SW, but decreasing at NE. Section 5 will demonstrate that, at this location, DC voltage excursions are exacerbated by the excitation of a natural DC circuit resonance during the blocking of NE converters, explaining the larger amplitudes observed.

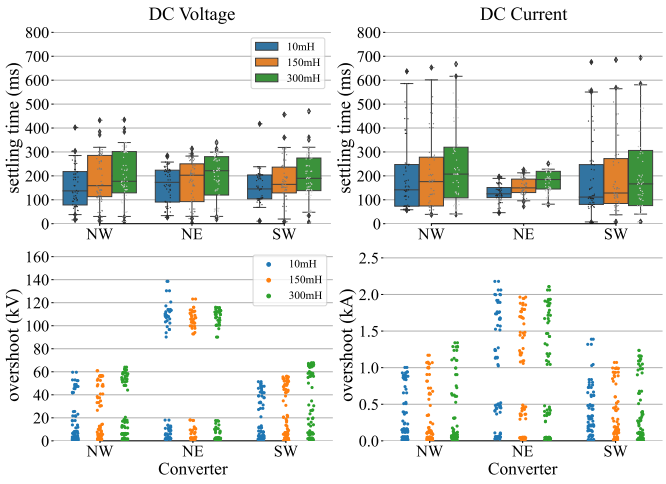

Fig. 7 KPI for units surviving an outage: DC voltage (Left), DC current (Right), Settling time (top), Overshoot (bottom)

3.3 Dynamic stresses: AT outside OSL

By systematically simulating the blocking of both receiving and sending ends for each N situation, half of the scenarios result in overvoltage and the other half in undervoltage, allowing evaluation of the dynamic ranges required to accommodate these temporary excursions in both directions. Fig. 8 first illustrates that dynamic stresses may be location-dependent. Although the topology and cable routing are similar between NW and SW, differences arise due to the presence of reactors associated with the DCSUs at specific locations.

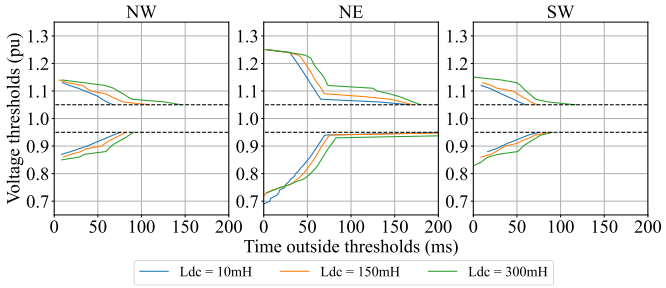

Fig. 8. AT outside OSL: surviving units. Outages only

Considering only unit outages, DC voltage excursions are contained within ±15% ([425, 575] kV, [0.85, 1.15] pu), with a return to the OSL occurring within 150 ms for onshore stations (NW and SW). For the offshore station (NE), excursions extend to ±25-30% ([350, 625] kV, [0.7, 1.25] pu), with a return time of approximately 200 ms. The overall dynamic performance at this station is reduced due to its operation in constant-power mode. Consistent with previous observations, larger reactor sizes lead to longer excursions beyond the continuous voltage operating range at all locations. Nevertheless, this amplification remains reasonable for the L_{DC} values considered, thereby confirming that the applied DC grid control philosophy yields acceptable system-level dynamic performance across different L_{DC} values and that the proposed generic model is suitable for supporting the definition of AC/DC converter requirements.

4 Results for Various Control Settings

This section examines the impact of varying control-setting assumptions on dynamic performance during grid-side temporary AC faults, with the DC reactor L_{DC} fixed at 150 mH. As before, Section 4.1 presents the TD system response for a representative scenario, while Sections 4.2 and 4.3 focus on performance metrics and DC voltage excursions, respectively.

4.1 Onshore Converter AC-FRT Example

Fig. 9 shows the DC voltage and current at the converters' DC-PoC during and after a temporary three-phase solid fault applied to the equivalent AC grid connected to the NW converter. The initial operating conditions are the same as in the previous scenario, with full power transfer from NE to NW.
In this case, SW takes over power export only *transiently* in accordance with its primary DC voltage control settings, as NW returns to its initial power reference once the fault is cleared, as expected. During the initial stage of the fault, the dynamic responses of the unaffected units are similar to those observed in the equivalent scenario with converter blocking (outage study; see Section 3.1). In contrast, the behaviour of the affected station, which remains operational in this case, differs significantly, as DC voltage regulation is maintained through the MMC energy and DC voltage controllers, making it highly dependent on the applied control settings.
To highlight the impact of converter control on DC voltage dynamics during AC-FRT, two control variants are explored:

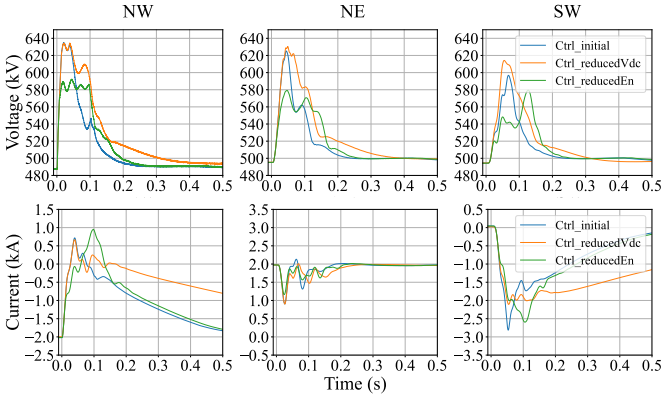

Fig. 9 NW (Left), NE (Middle), SW (Right). AC fault on converter NW: DC voltage (Top), DC current (Bottom)

- *Ctrl_reducedVdc*, shown in orange, with reduced gains in the DC voltage control loop; and
- *Ctrl_reducedEn*, shown in green, emulating tighter regulation through stricter limitations. In practice, more sophisticated vendor-specific solutions may be able to maintain continuous controllability within the linear domain.

Reducing the DC voltage control gains tends to slow voltage regulation, resulting in prolonged excursions. Maximum voltages at the affected station remain similar to the base case, while slightly higher peaks occur at the surviving stations, highlighting the close link between control design and system performance. Alternatively, limiting the DC voltage reference within the MMC energy loop to lower thresholds effectively contains DC voltage excursions. The stiffer DC voltage control during the fault shifts the DC current peak by 50 ms, followed by a recovery similar to the base case. At the SW station compensating the power disturbance, the stress is slightly reduced and distinctly delayed. Nonetheless, careful attention is required regarding fluctuations in Submodule (SM) capacitor voltages under these conditions, as they may cause unacceptable energy variations. Further insight into SM stress for this type of disturbance likely requires more detailed investigations, beyond the validity limits of the generic modelling approach based on the AAM, which assumes perfect SM balancing.

4.2 System Performance Evaluation

Fig. 10 shows that overshoots remain significant during AC faults, reaching up to 150 kV at both NW and SW, and 250 kV at NE for the first two control variants. These values are notably higher than those observed in the outage study, primarily due to dynamic stresses at the affected converter, which is now included as it remains in operation.
Consistent with previous observations, the third control variant (*Ctrl_reducedEn*) mitigates overvoltage at the DC-PoC, but this comes at the expense of slower DC current dynamics. Consequently, prolonged excursions occur. Although these are not captured by classical performance indicators such as settling times (see Appendix B), they are reflected by the proposed AT outside OSL metric, as discussed in the following section.

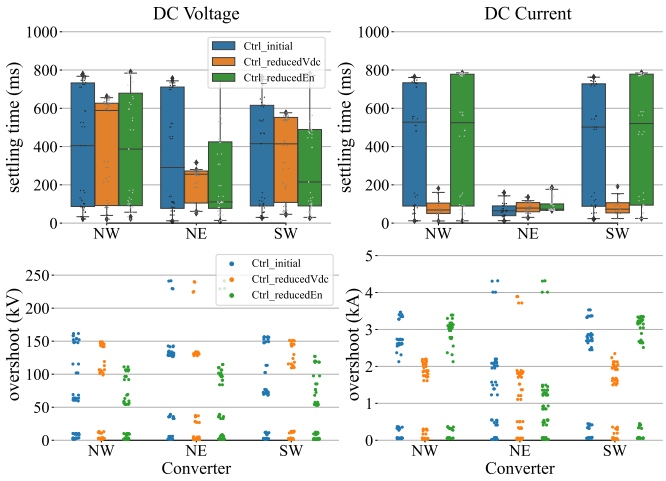

Fig. 10 KPI on converter for a temporary AC fault: Settling time (Top) and Overshoot (Bottom).

The *Ctrl_reducedVdc* case exhibits reduced DC current overshoots. For the same power unbalance, relaxing the control settings leads to larger DC voltage deviations, which in turn limit DC current variations. The rapid settling of the DC current at NE (offshore) is due to its VF control mode, which effectively behaves as a constant power mode on the DC side, while the temporary disturbance is explained by the energy controller response.

4.3 Dynamic stresses: AT outside OSL

Fig. 11 confirms that a dynamic band of ±30% ([350, 650] kV or [0.7, 1.3] pu), with a 200 ms return to the OSL, adequately captures the DC pole-to-neutral voltage excursions caused by 100 ms properly cleared AC faults across all three control variants, assuming a representative DC reactor of 150 mH.
It should be noted, however, that the similarity in results is due to the consideration of a single DC grid topology and configuration (GGW) at this stage, with the same disturbance applied, i.e., a temporary loss of active power. Moreover, all converter units remain operational, with those participating in DC voltage control effectively responding to the deviation, while NE remains at constant DC power.

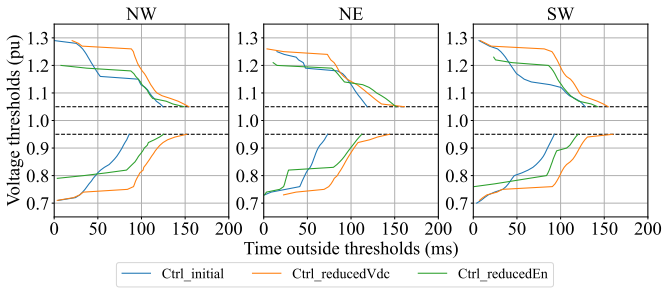

Fig. 11 AT outside OSL: AC faults only including affected unit

Additionally, this study is limited to strong onshore grid assumptions, with WPPs represented as aggregated equivalents and protections excluded. The AC fault analysis is further restricted to solid three-phase faults. While impedance faults are expected to impose less severe constraints, unbalanced faults could introduce second-harmonic components into the DC voltage, potentially creating energy imbalances within the affected converter. Such effects are typically managed through established negative-sequence control techniques but should nonetheless be carefully considered in detailed design studies.

5 Frequency-Domain Analysis

Detailed analysis of TD simulation results from the InterOPERA HVDC grid dynamic design studies revealed the excitation of specific resonances following certain events.
As reported in a previous work [9], blocking the NE converter led to large and sustained oscillations around 85 Hz. These oscillations were attributed to a natural grid mode, since the blocked converter's participation could be naturally excluded, although the other terminal on the healthy pole could provide some damping in practice. This hypothesis was further supported by a FD analysis of the passive DC grid with all converters fully excluded. Oscillations around 30 Hz and 145 Hz were also observed in DC voltage step tests for the GGG configuration (see Fig. 12). These are not excited in the GGW case, as NE operates in VF mode, which prevents the application of a step at this location.

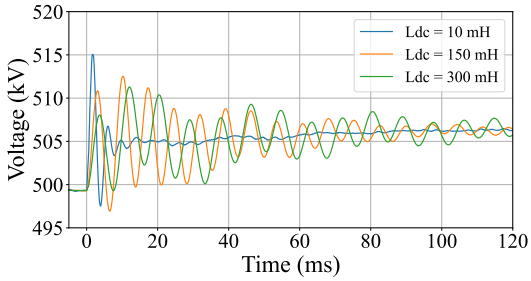

Fig. 12. DC voltage following a reference step (GGG case)

In this work, the focus is placed on the impact of converter DC-side reactor size on the system's frequency-dependent impedance as observed from the NE DC-PoC. To this end, a DC grid frequency scan is reconducted, this time including a partial representation of the converters, limited to their passive LC components: the six arm inductances, the 6 × N capacitors, and the DC inductance, with equivalents calculated as follows:

$$C_{eq} = 6\frac{C_{sm}}{N_{sm}} \tag{2}$$

$$L_{eq} = \frac{2}{3}L_{arm} + L_{DC} \tag{3}$$

This yields an equivalent capacitance of 345.6 μF (when considering N_{sw} =300 SMs and a capacitance of C_{SM} =17.23 mF) per SM and an inductance of 173 mH (for L_{DC} = 150 mH).

Converter controls were excluded from the analysis, as the frequency response of the generic model has limited practical relevance. In reality, converter controls significantly influence system dynamics, particularly at low frequencies.
The frequency scan was performed using EMTP®'s frequency scan functionality, which enables rapid analysis of the entire grid impedance at the converter DC-PoC by injecting a 1 A current at each scan frequency and measuring the resulting voltage [16]. In this study, the scanning device was connected between pole and neutral at the DC-PoC.
Fig. 13 shows the DC voltage at the DC-PoC of NE during a blocking event at this terminal, which excites the grid's natural 85 Hz mode. The frequency scan on the right confirms that the amplitude of this resonance peak is largely unaffected by the converter-side reactor value. Complementary investigations, omitted here for brevity, indicate that this resonance frequency is sensitive to the DCSS reactor value.
In contrast, other modes, most notably the largest anti-resonance, shift from slightly above 100 Hz to beyond 200 Hz depending on L_{DC}. This mode is observed during the classical step test applied at the NE station (in the GGG configuration) as illustrated in Fig. 12.

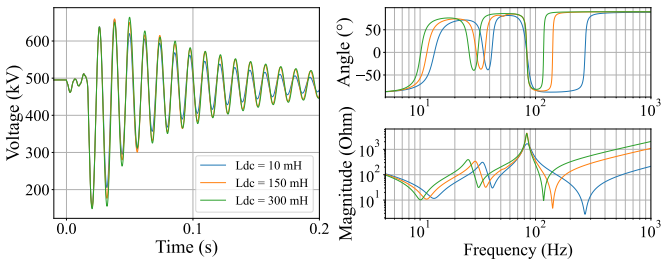

Fig. 13 DC voltage at the NE station during a blocking event (Left). Frequency scan of the passive elements of the DC grid, including the converter DC inductances and valve capacitors (Right) for different DC smoothing reactor values

6 Conclusion and Discussion

The results presented so far illustrate that the DC grid topology, along with station design and location, influences stress level experienced by the subsystems. However, technical specifications should avoid geographical discrimination. It is therefore more appropriate to define robust envelopes that encompass various configurations, based on station types (onshore and offshore) rather than specific connection points. To this end, Section 6.1 presents DC voltage dynamic bands including the other two configurations investigated in InterOPERA, while Section 6.2 concludes with the maximum envelopes by station type and assumption set, aggregating results for all configurations.

6.1 On the Configurations: Onshore vs. Offshore Stations

Fig. 14 shows that, as mentioned earlier, AC faults impose the highest constraints in terms of magnitude; however, outages can be more severe in terms of duration in certain cases (GGG).

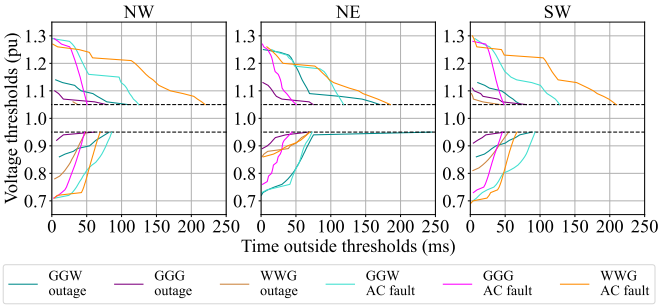

Fig. 14. AT outside OSL: All events and configurations

AC faults in the WWG case represent the worst-case scenario, prompting closer assessment of the modelling of the offshore grid and VF control mode. The GGW case ranks second, with maximum excursions driven by resonance phenomena at NE.
Two important points must be note:

- In the GGG case, the resonance is not excited to the same amplitude following NE converter blocking, as the phenomenon is exacerbated by the behaviour of the WPP during the event; specifically, the sudden interruption of the DC current, which drops sharply from its nominal value to zero upon breaker opening (protection triggered at the WPP). This occurs because the WPP continues injecting full power even after its converter blocks, causing the current to flow through the valve diodes.
- In the WWG case, the NE outage is not simulated, as the system is not expected to survive the loss of the only DC voltage-controlling station.

These observations highlight the importance of accounting for all relevant operating modes, conditions, and events in design studies; a task that becomes increasingly complex in the context of MT grids, even for a relatively simple 3T topology. Overlooking critical phenomena at an early stage increases the risk of interoperability issues in operation. Put another way, **HVDC grid design studies are a critical step towards achieving interoperability by design.**

6.2 Dynamic Operating Ranges Including All Variants

Fig. 15 aggregates results by station type and compares the impact of study assumptions on the design of AC/DC converters, related to both physical and control components, showing that the robustness of requirements can be enhanced by varying selected parameters within a relevant range.
The results corresponding to the *Ctrl_reducedVdc* case are only included to illustrate the importance of fine-tuning the generic model to achieve realistic results that align with expected performance. Failure to do so may impose unnecessary burdens in subsystem design. The green envelope should therefore be disregarded. Instead, it may be relevant to assess the impact of alternative control modes in future investigations, as these are anticipated to significantly influence the resulting envelope.

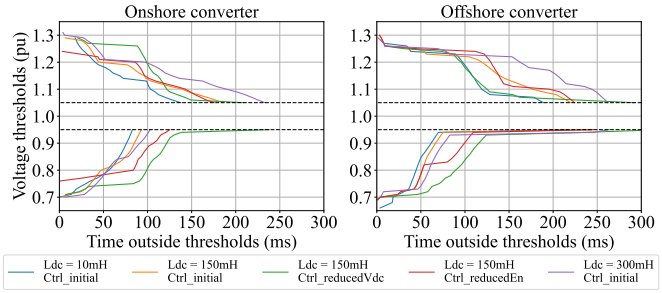

Fig. 15. AT outside OSL: envelops of all variants

While one might be tempted to simply adopt the majorant envelopes, there is no guarantee of compatibility with available equipment capabilities. Put another way, whether these constraints, which add to classical AC-side requirements, can be met by off-the-shelf equipment or will require costly redesign can only be determined after detailed subsystem design by OEMs. More generally, project-specific considerations for extreme cases may be a sensible way to mitigate the risk of overdesign arising from premature standardisation.

A potentially more relevant and open question concerns the translation of system-wide requirements regarding operating ranges into subsystem (standalone) specifications. Applying the envelopes as hard profiles at the DC-PoC may impose significantly higher constraints on the AC/DC converter, in terms of energy management for instance, than the physical signals in an actual grid-connected event would.

6.3 InterOPERA HVDC Grid Design Studies – Transient Part

The next part of this paper series focuses on transient stresses arising from DC faults. With reference to Section 2.1.9, a final takeaway is that, although the same detailed transient model was used in this work, certain simplifications may be acceptable as a starting point for preliminary dynamic design studies to validate the generic model before conducting full transient analyses. An iteration must always be performed.

A Details on Control Variants

Fig. 16 provides a schematic representation of the implemented energy loop, highlighting the investigated control variants.

The generic MMC control model used in this work adopts a classical cascaded structure, in which references for the Grid Current Controller (GCC) are provided by outer loops. For onshore stations, a PI-based DC voltage controller is employed, with its reference ($v_{DC,ref}$) determined by the droop scheme shown in Fig. 3. As noted earlier, the DC voltage dynamics are strongly dependent on the tuning of this controller. The *Ctrl_reducedVdc* variant is obtained by adapting the PI gains (k_p and k_i) at this level. Alternatively, the DC voltage response can be tightened or relaxed by adjusting the limitations at the output of other control loops, for example, the Z-sequence Σ current controller in the energy-based scheme proposed in [17], resulting in the *Ctrl_reducedEn* variant.

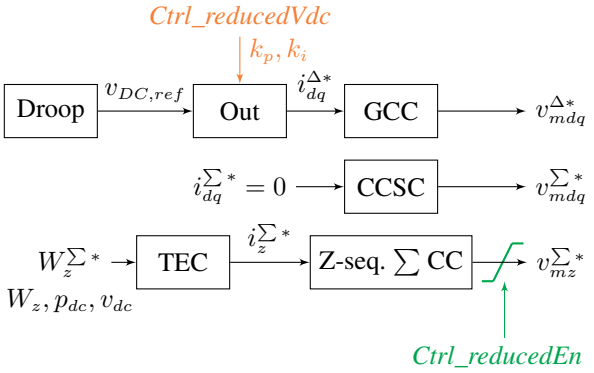

Fig. 16 Schematic representation of the implemented energy loop, highlighting control variants, adapted from [17]

B Discussion on the KPI Calculation

The KPI presented in this paper were computed using a fixed tolerance band of 1 kV or 50 A, with the corresponding results highlighted in orange in Fig. 17. These values were carefully selected through sensitivity analysis and are intended primarily for comparison rather than for precise determination of absolute values. For standalone compliance verification, however, standardised methods should be applied.

Fig. 17 shows how the calculated settling times vary with tolerance choice. As expected, increasing the tolerance tends to (potentially artificially) reduce the obtained KPIs, but may also exclude small disturbances that remain within the predefined band, thereby preventing accurate calculation. This explains why the average in the 2 kV–10 A case may slightly increase, while the overall trend at the extremes remains consistent.

Conversely, overly tight tolerances produce excessively long and non-meaningful settling times. Signal filtering is recommended to suppress numerical noise.

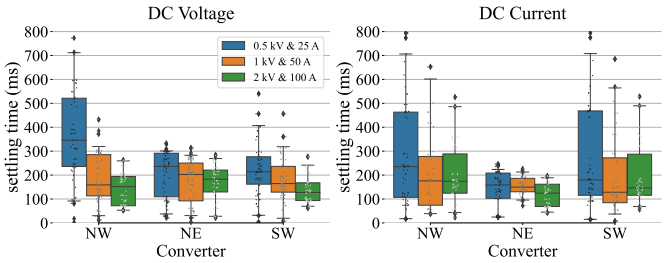

Fig. 17 KPI for units surviving an outage with Ldc=150mH, for different tolerance bands used in the computation

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