MULTI-TERMINAL MULTI VENDOR HVDC GRID DESIGN STUDIES – PART III: TRANSIENT STUDY

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Abstract

Multi-Terminal (MT) HVDC networks have been studied for over a decade, with recent efforts increasingly focusing on enabling multi-vendor interoperability to support a competitive and scalable deployment framework. Concurrently, protection selectivity is receiving renewed attention in the context of large-scale offshore connections based on 2 GW bipolar building blocks, where the maximum loss of infeed has become a critical planning constraint. This three-part series addresses early-stage system-level studies of MT HVDC grids using generic models, which are essential to support primary design. As part of the InterOPERA project, involving HVDC vendors traditionally responsible for DC-side design in point-to-point schemes, a methodology is proposed to refine, and eventually instantiate, project-specific technical requirements at subsystem DC point-of-connection. This third part focuses on transient studies, quantifying maximum DC short-circuit currents and overvoltages induced by pole-to-ground faults throughout the fault separation process. The variability of system-level electrical stress is assessed as a function of two key design parameters: AC/DC converter reactor sizes and DC circuit breaker's maximum fault neutralisation times. Broader discussions on insulation coordination considerations and DC fault ride-through requirements are also provided.

1 Introduction

Driven by the increasing scale of Offshore Wind Farms (OWFs) and the growing need for greater cross-border interconnection capacity, bipolar High Voltage Direct Current (HVDC) systems based on Modular Multilevel Converter (MMC) technology are expected to play a key role in future transmission networks. However, concerns regarding the techno-economic feasibility of relying exclusively on Point-to-Point (P2P) links have prompted the industry to address the challenges of transitioning to Multi-Terminal (MT) grids.

In this context, the InterOPERA project was launched to enable future HVDC systems from different suppliers to operate together, paving the way for the actual implementation of Europe's first MT, Multi-Vendor (MV), multi-purpose HVDC projects. InterOPERA has already achieved several key milestones, including the development of common functional specifications [1] and minimum interface requirements [2].

A Real-Time (RT) demonstrator is currently being deployed to validate and refine the proposed methods and processes, ensuring their practical applicability. This work focuses on activities supporting the implementation of the RT demonstrator, particularly HVDC grid design studies using vendor-agnostic generic models, that provide input to detailed subsystem specifications. Three study packages were defined, with key findings presented in this three-paper series: Part I introduces a DC Load Flow (LF)-based contingency analysis [3], while Part II examines the system dynamic response following unit outages [4]. This third part addresses transient electrical stresses at the DC Point-of-Connection (DC-PoC) of various subsystems during and following **DC faults**. As introduced in the companion papers [3, 4], InterOPERA adopts a bipolar configuration rated at 2 GW per converter station with DC fault-handling capabilities [5]. DC Switching Units (DCSUs) equipped with DC Circuit Breakers (DCCBs) are implemented in selected DC Switching Stations (DCSSs), incorporating reactors to limit the fault current rise rate and enable fault separation. As illustrated in Fig. 1, the inclusion of DCCBs introduces the concept of Fault Separation Zones (FSZs), requiring parts of the system to withstand and recover from *external* DC faults; a structural assumption that significantly influences the results presented in this work. This notably implies that AC/DC converters must comply with DC-Fault Ride-Through (DC-FRT) requirements, which may necessitate revisiting their design. Although two topologies are considered in the project: a Three-Terminal (3T) and a Five-Terminal (5T) DC grid, both including a central DCSS, this paper series focuses on the 3T base case.

1.1 Background on Transient DC-side Requirements

In practice, the solutions delivered by vendors are developed to comply with contractually binding technical specifications. Transient DC interface requirements, typically expressed in terms of Short-Circuit Current (SCC) and DC-Temporary Overvoltage (TOV), have been incorporated into the specifications of P2P HVDC projects due to the separation of converter station and cable procurement processes. These requirements are generally derived from pre-design studies supported by Electromagnetic Transient (EMT) simulations, using generic models tailored with project-specific assumptions.

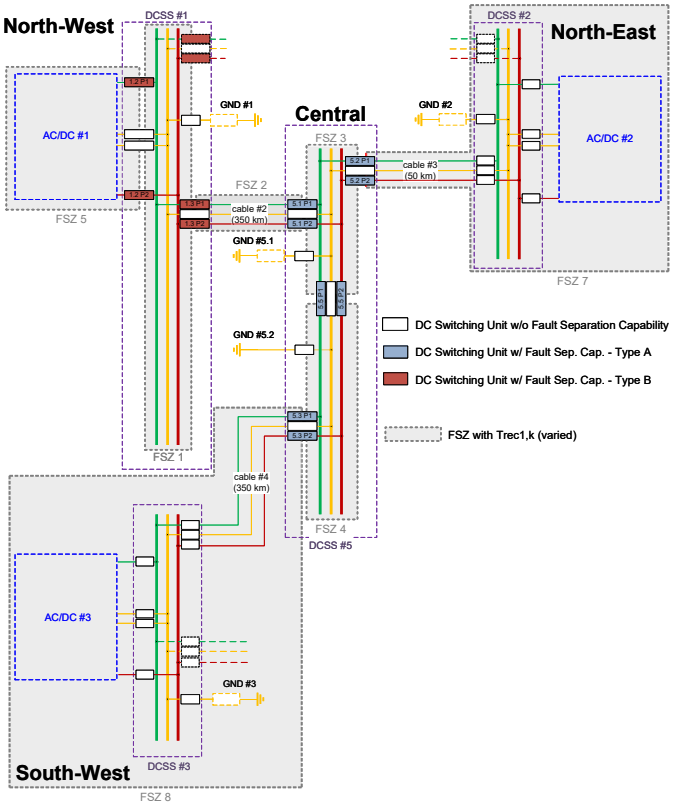

Fig. 1. 3T DC grid topology highlighting seven relevant FSZs

More recently, initiatives have emerged to define common specifications across similar HVDC projects, aiming to reduce pre-design workload while preserving cost-effectiveness by balancing conservatism against the risk of overdesign [6]. Although a relevant first step towards standardisation, challenges associated with bipolar configurations, MT topologies, the MV framework, and DC fault-handling requirements remain unresolved; gaps that InterOPERA seeks to bridge.

1.2 InterOPERA Technical Requirements and Design Studies

In the context of InterOPERA, technical specifications have been established jointly by project stakeholders, primarily introducing new DC-side requirements [7], which are applied cumulatively with conventional AC-side requirements. Detailed HVDC grid design studies were undertaken to specify DC voltage operating ranges applicable to the demonstrator [3, 4]. In particular, transient studies verify that maximum electrical stresses, typically SCC and overvoltages, remain within prescribed equipment capabilities for selected protection settings and insulation coordination assumptions, thereby confirming the suitability of the envisioned requirements (i.e., withstand voltages and maximum fault neutralisation time) for the planned system topology and protection scheme.
Given the significant differences between the technical capabilities of vendor-specific solutions, both for AC/DC converters and DCSSs, dedicated subsystem-level parameters were implemented in the InterOPERA design studies to reconcile the enforcement of DC-FRT requirements with the current limitations of available technologies.

In this paper, key findings from the InterOPERA HVDC grid transient design studies are partially generalised through sensitivity analysis, offering an alternative approach to cope with the potential absence of Original Equipment Manufacturer (OEM) involvement at an early stage.
In the general case, once contracts are awarded, it is advisable to verify that final subsystem characteristics remain within the conservative assumptions adopted during the initial design phase. This helps mitigate interoperability risks stemming from possible misalignments in primary design; a crucial aspect further addressed by InterOPERA's Work Package 5.
Summarizing, the contributions of this work are threefold:

1. A general methodology is proposed for conducting HVDC grid **transient** design studies using generic models.
2. Its application to the InterOPERA demonstrator setup provides insight into the expected stress levels in such systems.
3. A parametric analysis highlights the sensitivity of key electrical stress metrics to:
   - subsystem design parameters, falling within the OEM scope and uncertain during early-stage studies, and
   - fault separation requirements applied to selected DCSSs.

In the following, Section 2 outlines the proposed methodology and key modelling assumptions, aligned with the study scope. Sections 3 and 4 present the simulation results, beginning with Time-Domain (TD) responses for a representative case, followed by a quantification of transient electrical stresses across various scenarios. Variations in AC/DC converter smoothing reactor sizing (a subsystem design parameter that cannot be prescribed) and the maximum neutralisation time of fault separation devices, specifically DCCBs (a functional parameter defined in specifications), are investigated. Section 5 provides background on the insulation coordination study, further detailed in a subsequent work. Section 6 concludes with the derived DC voltage operating ranges and a broader discussion of the DC-FRT requirements adopted in InterOPERA.

2 Study Scope, Methodology and Modelling

The topology of the InterOPERA demonstrator was initially proposed in [5]. The detailed HVDC grid design study task included an assumption alignment phase involving subsystem vendors to refine the demonstration scope and establish relevant generic parameter values. A 3T base case, illustrated in Fig. 1, was defined, comprising three AC/DC converter stations and four DCSSs, of which only two, located at North-West (NW), DCSS #1, and the centre, DCSS #5, are equipped with DCCBs. In practice, the desired level of selectivity is expected to be determined through a detailed techno-economic assessment, which lies outside the scope of InterOPERA.

2.1 Key Assumptions for Transient Design Studies

This configuration results in seven FSZs for the 3T topology. FSZ #6 is associated with a second AC/DC converter station at NW in the 5T topology and is not relevant for the 3T case. The DCCB positions alone qualitatively determine

these FSZs, i.e., the expected behaviour of the overall protection scheme in terms of resulting system-split scenarios. Protection performance is further characterised by a grid-level *functional* parameter: the maximum partial voltage recovery time, denoted T_{rec1}. Different T_{rec1} values may be assigned to specific areas of the HVDC network, thereby defining distinct *subgrids* consisting of one or more FSZs. For each subgrid, $T_{rec1,k}$ is set equal to or greater than the largest maximum fault neutralisation time ($T_{N,Max,i}$) within the subgrid, depending on whether an additional buffer margin (t_b) is applied [1]. Hence, the choice of $T_{N,Max}$ directly establishes the minimum fault separation requirements for the DCSSs, but also determines the withstand capability required to AC/DC converters through T_{rec1}. The latter is illustrated in Fig. 2, which shows the voltage-based DC-FRT requirement applicable to subsystems connected to the DC grid.

As a result, both interdependent requirements strongly influence subsystem design parameters within the OEM scope, which in turn affect system-level performance. In AC/DC converters, for example, the DC-FRT requirement entails a trade-off between reactor sizing and current-carrying capability, alongside other potential design constraints [1, 8]. While higher inductance helps limit current rise during faults, it can also challenge DC voltage control performance [4], increase footprint and losses [3], and introduce mechanical constraints.

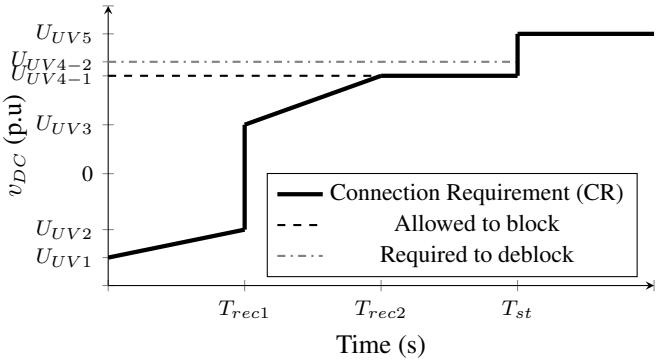

Fig. 2. DC-FRT requirements. Adapted from [1]

2.1.1 Maximum Fault Neutralisation and Partial Voltage Recovery Times: although the InterOPERA design studies considered two distinct subgrids with specific $T_{rec1,k}$, this paper assumes a uniform value across the entire system. Nonetheless, three values are considered: **3, 5 and 7 ms**, representing possible functional parameter specification based on plausible assumptions for the maximum (worst-case) fault neutralisation time associated with available DCCB technologies (here, $T_{rec1} = T_{N,Max}$). $T_{N,Max}$ includes both the protection relay pick-up time (T_R) and the internal current commutation time (T_I), but only up to the point where the current stops increasing. The former spans from fault inception at DCCB terminal, thus excluding wave propagation phenomena, until the trip command is issued [9]. The latter includes the breaker operation and voltage rise. The effective fault neutralisation time (T_N, i) results from subsystem design and must simply remain below the specified $T_{N,Max}$. In practice, T_R depends on the fault type, location, impedance, and protection algorithm, while T_I depends on the breaker technology. The other time settings in the DC-FRT profile, T_{rec2} and T_{st}, correspond to the expected return to the dynamic and continuous operating ranges, respectively; outcomes of the design studies.

2.1.2 Reactor Sizes for DCSUs and AC/DC Converters: a single inductance value of **200 mH** is assumed for all DCSUs with fault separation capabilities (L_{FSD}). For converters, the arm inductance is fixed at **35 mH** (L_{Arm}), and the DC-side reactor (L_{DC}) is varied across three values: **10, 150 and 300 mH**. For design studies applied to the InterOPERA demonstrator, device-specific reactor values were computed through DC-FRT standalone tests for a given $T_{rec1,k}$ and vendor-declared current capability ($I_{Arm,Max,i}$). To remove dependence on the latter, likely unavailable at the early design stage, this work computes the underlying, indicative current capability *requirements* (not explicitly imposed) from explicit assumptions on T_{rec1} and L_{DC} (see Section 6.3). Consequently, for certain parameter combinations in the sensitivity analysis, very large arm currents may result, which could exceed the capabilities of some available converter technologies. It should be noted, however, that assuming this capability as *unlimited* would, in practice, introduce a risk of indirect technology exclusion, which was not acceptable in InterOPERA, as all partners delivering solutions must be eligible to participate in the demonstrator.

2.1.3 Exploring the Temporary Blocking Functionality: in line with the InterOPERA functional requirements [1], AC/DC converters may be allowed to block temporarily during a DC fault, provided they remain connected (CR in Fig. 2) and can resume normal operation after fault clearance. To reflect this behaviour in design studies, automatic triggering of the AC Circuit Breaker (ACCB) upon blocking has been disabled. In this work, the arm current threshold for blocking ($I_{Arm,Blk}$) is set to a generic value of **3.5 kA**. However, the deblocking feature has not been implemented due to the absence of a widely accepted functional specification or generic model. As a result, once a converter blocks (based only on the arm current criterion), it remains connected and blocked for the rest of the simulation. Arm currents continue to be monitored in the blocked state and constitute a key outcome of the study, as they represent the maximum current that converters would be required to withstand while remaining connected under practical grid-connected conditions. They also provide an indicative estimate of the conservatism introduced by the DC-FRT standalone requirements applied in InterOPERA. In practice, the decision to permit temporary blocking lies with the relevant System Operator. If allowed, voltage and power recovery, along with potential interaction risks during the deblocking of multiple converters, must also be evaluated. In InterOPERA, these will be investigated during the demonstration phase using vendor-provided solutions. In the absence of a detailed design study, the specifications at this stage remain relatively open [7].

2.1.4 DC Cable TOV, Rated and Withstand Voltages: the InterOPERA demonstrator is based on 525 kV bipoles, for which IEC and CIGRE recommend different Switching Impulse Withstand Voltages (SIWVs) values [10, 11]. For the InterOPERA demonstrator, a preliminary SIWV of 1050 kV is retained. Based on this, two possible Lighting Impulse Withstand Voltages (LIWVs) can be defined: 1050 kV and 1175 kV. In this study, the higher value is assumed, and the DC-TOV profile proposed in [5] is adopted for the DC poles. For rating the Dedicated Metallic Return (DMR), standardised practices are currently lacking. Preliminary investigations suggested adopting a highest voltage (Um) of 52 kV RMS (defined for AC systems). According to IEC 60071-1 [12], the associated LIWV is 250 kV, and the short-duration power-frequency withstand voltage is 95 kV. This assumption has, in practice, limited influence on the study outcomes, as it primarily affects the neutral cable insulation thickness. In contrast, the assigned protective level is critical for DC transient stress analysis. In this work, the DMR rating was, in fact, derived from the required protective level, an outcome of the insulation coordination study, thus applying a reverse logic compared to the conventional approach used for pole cable design.

2.2 Modelling Considerations for Transient Design Studies

The 3T base case EMTP® model developed in the previous study package [4, 13] is reused in this work. This section provides additional details relevant to transient investigations.

2.2.1 AC/DC converters: the converter is modelled using an Average Arm Model (AAM). Its accuracy, including during the blocked state, is deemed sufficient for transient design studies with generic models, provided that only external disturbances are of interest. Results should, nonetheless, be interpreted with caution due to inherent limitations of this simplified representation; most notably, the assumption of ideal Submodule (SM) capacitor voltage balancing. Excessively steep transients in the total SM capacitor voltage may, for instance, indicate the need for explicitly modelling balancing control, which is highly dependent on the vendor-specific control implementation. A simplified converter *protection* model is implemented primarily to achieve reasonable system-level behaviour–that is, to ensure that converters in faulted zones trip as intended, avoiding the introduction of unrealistic stresses–rather than to precisely reproduce detailed internal protection. For blocking, the maximum of all arm currents is monitored, with command issued upon reaching the $I_{Arm,Blk}$ threshold. For tripping (ACCB opening), simplified voltage-based logics detect uncleared DC faults or non-viable islanding conditions, ensuring that converters in faulted protection zones are disconnected.

2.2.2 DCCBs: two generic model structures are considered, parameterised to achieve equivalent fault neutralisation times. As illustrated in Fig. 1, Type A DCCBs (in blue) are located at the central DCSS (#5). They represent a Voltage-Sourced Converter (VSC)-assisted resonant current technology consisting of individual modules connected in series. Each module comprises three branches: a main branch with a fast mechanical switch, a resonant branch including a capacitor and a VSC, and an energy-absorbing branch [14]. From a system-level perspective, this DCCB can be represented as a single aggregated module, with the resonant branch simplified using passive components only. Type B (in red) are located at NW (#1) and represent hybrid DCCBs as described in [15]. They consist of two branches: a main branch composed of multiple cells connected in series, where each cell includes an Insulated-Gate Bipolar Transistor (IGBT) in parallel with an energy absorber; and an auxiliary branch comprising a fast disconnector and an auxiliary DC breaker. In this work, protection relay modelling is excluded; instead, a constant delay is added to emulate the pick-up time. A fault arrival detection function based on local voltage measurement was implemented to account for the dependency of wave propagation delay on the fault location.

2.2.3 DC Grid – DC cables: wideband models have been developed based on [16], considering 50 km sections to capture wave propagation effects and enable fault inception and overvoltage monitoring along Cables #2 and #4 routes, each 350 km long, hence represented by seven identical sections. Each section is separated by a junction in which the sheath is connected to the ground with a resistance of 1 Ω. Besides the sheath and the armour of the cable are connected by a resistance of 0.1 Ω at each junction as proposed in previous work [6]. This approach is deemed sufficient to assess maximum electrical stress at subsystem interfaces. However, it may not be conservative if internal cable stresses were the primary concern, in which case more detailed models, based on accurate manufacturer data, would be required.

2.2.4 DC Grid – Neutral system: the DC grid is grounded at the central DCSS (#5) via a **5** Ω resistor. This preliminary value results from the InterOPERA demonstrator design study. In practice, slightly higher values may be required to ensure AC fault current zero-crossing during single-phase faults on the converter side of the transformer, depending on vendor-specific implementations [17]. To provide design margin, InterOPERA technical specification foresees connecting up to a 10 Ω resistor [7].

2.2.5 Surge Arresters: the generic voltage-current (V/I) characteristic defined in IEC 60071-11 [10] is used to modelled surge arresters, which are placed at subsystem interfaces and DCSS busbars. Suitable protective levels for the InterOPERA demonstrator, proposed during the design study phase, are retained for this complementary analysis. For the poles, the Lighting Impulse Protective Level (LIPL), defined at 10 kA, is set to **980 kV** after applying a safety factor of 1.2 to the selected LIWV [10]. For the DMR, the LIPL is set to **83 kV** following parametric investigations. These settings result in a vertical translation of the V/I characteristic, which is anchored using a single reference point (the selected LIPL at 10 kA); all other points on the V/I curve are scaled accordingly.

2.2.6 AC grids: onshore stations are modelled using Thevenin equivalents under strong grid assumptions, while OWFs are represented by aggregated generic models. Refer to Part II - Dynamic Study [4] for details.

2.3 Scenario Definition

The InterOPERA demonstrator considers three configurations for the 3T base case depicted in Fig. 1:

- GGG: the three AC/DC converter stations are connected to asynchronous onshore grids;
- GGW: one station, North-East (NE), connects to an OWF;
- WWG: there is only one onshore station (NE), operating in fixed DC voltage control mode.

For brevity, results presented in this work are limited to the GGW configuration, for which eight initial operating conditions (N situations) were defined by the DC LF-based contingency analysis [3]. Simulated events include pole-to-ground faults along the DC cables and at the DCSS busbars. InterOPERA design study also examined single-phase faults on the converter-side of the transformer however, the results are omitted. In total, twenty-two pole-to-ground faults are analysed:

- 18 cable faults, modelled as core-to-sheath short circuits to represent insulation failures;
- 3 busbar faults (one at DCSS #1 and two at DCSS #5); and
- one additional case at the DC-PoC of the NW converter.

2.4 Key Performance Indicators

Transient stresses for design purposes are defined in this work as the maximum DC voltages and currents observed at subsystem terminals following DC faults, with a focus on the AC/DC converters. Arm currents are also reported. Voltage-versus-duration characteristics are used to quantify the time spent beyond specific DC voltage thresholds. The observation window is deliberately limited to 100 ms after the event, as the focus is on the *transient* range. That said, in a MT context, a certain level of dynamic performance is expected to enable recovery of unaffected parts of the system. Box plots are used, where the box represents the interquartile range (±25%), and the whiskers extend to the 5th and 95th percentiles.

3 Results for Various DC Inductance Values

This section presents a sensitivity analysis of transient stresses for varying AC/DC converter DC reactor values and a fixed maximum fault neutralisation time of 5 ms. Section 3.1 illustrates the TD system response for a selected scenario. Section 3.2 discusses overall system performance following DC faults across all scenarios and variants. Section 3.3 focuses on DC fault currents, while Section 3.4 quantifies DC voltage excursions. Maximum arm currents are reported in Section 3.5.

3.1 One Example in the Time-Domain

Fig. 3 shows simulation results for a pole-to-ground fault on Cable #2 (junction #2). In this scenario, the NE converter injects full power (2 GW), which is exported by South-West (SW), while NW compensates for system losses. The fault is cleared and isolated by the opening of the DCCBs at both the NW and the central DCSS, resulting, in the 3T base case, in the disconnection of the NW converter **from the DC grid**. In the 5T topology, a parallel cable between NW and NE motivates the interest of NW survival. Increasing the AC/DC converter reactor size reduces the DC SCC peak but also leads to larger DC voltage excursions on both the affected and healthy poles. In all cases, power transfer on the affected pole is maintained by the surviving units, with SW restoring its pre-contingency full power export within 50 ms.

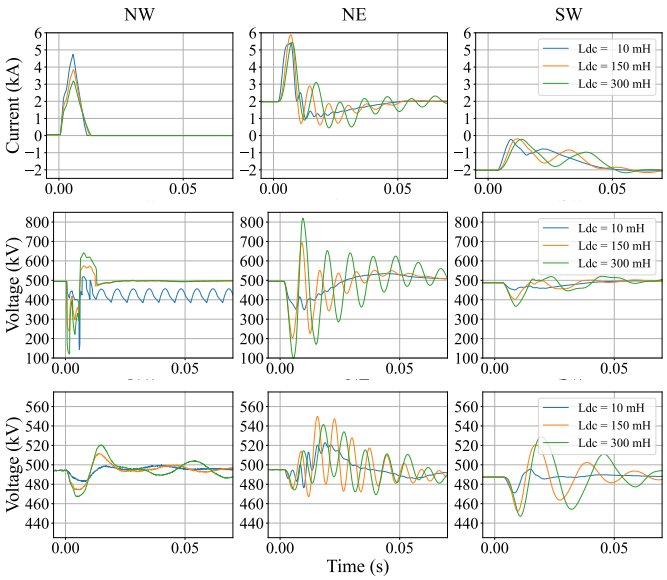

Fig. 3 NW (Left), NE (Middle), SW (Right). Affected pole DC current (Top), affected pole DC voltage (Middle), healthy pole DC voltage (Bottom). Pole-to-ground fault along Cable #2 (J2)

Fig. 4 shows arm currents at NW for the three converter reactor settings, with the blocking threshold exceeded only for the 10 mH case. As previously mentioned, even though a converter blocks, the ACCB does not operate. Consequently, the NW converter remains connected **to the AC grid**, keeping the DC side energised. However, when blocked, it behaves as a diode rectifier bridge, which explains the pulsation observed in the 10 mH case (Fig. 3-Middle-Left).
It is also worth noting that at NE, the DC current reaches similar levels, yet normal operation is maintained for the given reactor value, as arm currents remain below the blocking threshold (see Fig. 4-Bottom). Careful attention must be paid to the distinction between these two quantities, which depends on additional factors such as operating point, AC-side connection, and other system conditions.

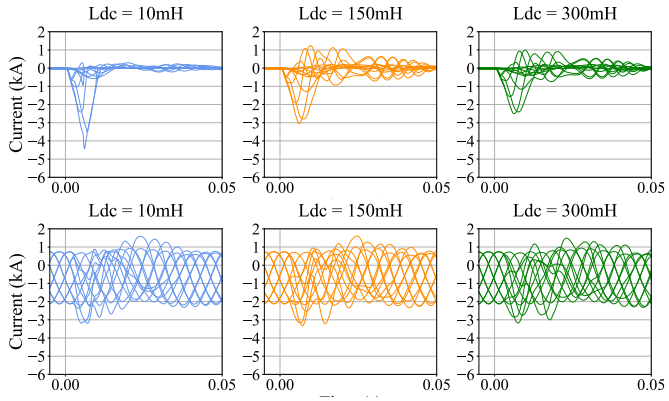

Fig. 4 Arm current at NW (Top) and NE (Bottom) for different converter reactor values. Pole-to-ground fault, Cable #2 (J2)

3.2 Overall Performance of the Protection Scheme

Fig. 5 shows aggregated results for all 176 simulated scenarios (8 N situations × 22 DC-pole to ground faults, refer to Section 2.3) across the three predefined L_{DC} variants, uniformly applied to all converters. In all cases, the overall protection scheme performs as intended, with ACCB operation (red bars) triggered for faults at the converters' DC-PoC in the corresponding FSZ: FSZ #5 for NW, FSZ #7 for NE, and FSZ #8 for SW. The latter two zones also include faults along Cable #3 (simulated only at the terminations) and Cable #4 (eight locations), respectively. Additionally, the NE converter trips for faults in FSZ #3, as the DC cable disconnection at the remote end results in an islanded condition on the DC side, which is non-viable due to absence of DC voltage control capability. For all other FSZs (#1, #2, and #4), all converters remain connected, as expected.

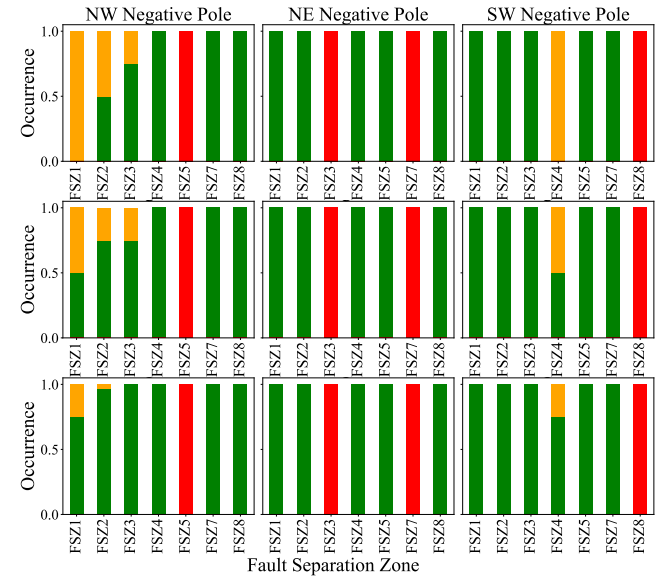

Fig. 5 AC/DC converter final state and L_{dc} ($T_{N,Max}$ =5 ms): (Top) 10 mH, (Middle) 150 mH and (Bottom) 300 mH. Operational (green), Blocked (yellow) and Tripped (red)

Given a fixed maximum fault neutralisation time (here, 5 ms), reducing the DC-side reactor value at the converter level tends to increase the number of converter blocking events. Notably, for the highest inductance value (300 mH), the NW converter remains operational for most faults along Cable #2 (FSZ #2) and for all remote faults at the central DCSS (FSZ #3), whereas lower inductance values result in blocking under several scenarios. Similarly, the SW converter always blocks for faults in FSZ #4 when the lowest inductance value (10 mH) is applied. For a given reactor value and FSZ, the final state–operational or blocked–depends on the initial operating conditions, with inverter mode naturally representing the most favourable case.

3.3 DC Short Circuit Current at DC-PoC

Fig. 6 shows the maximum DC SCC at the converters' DC-PoC. For a meaningful assessment, the results are categorised by the final operating state: operational, blocked, or tripped, as the requirements focus on normal operation and, to some extent, the blocked state. Values associated with tripping are included for reference but are primarily relevant to OEMs, particularly for detailed subsystem design, where internal faults should also be considered. For operational converters, results are further distinguished between affected and healthy poles.
As expected, the maximum SCC tends to decrease with increasing DC smoothing reactor size (see blocked and tripped converters), while reactors at all DCSUs with fault separation capability are maintained at 200 mH and the fault neutralisation time at 5 ms. For operational converters, no clear trend emerges; however, comparing current peaks in such cases is of limited relevance, as the results are effectively truncated. Reducing inductance increases arm currents, which in turn tend to trigger blocking and shift the data point to a different figure.

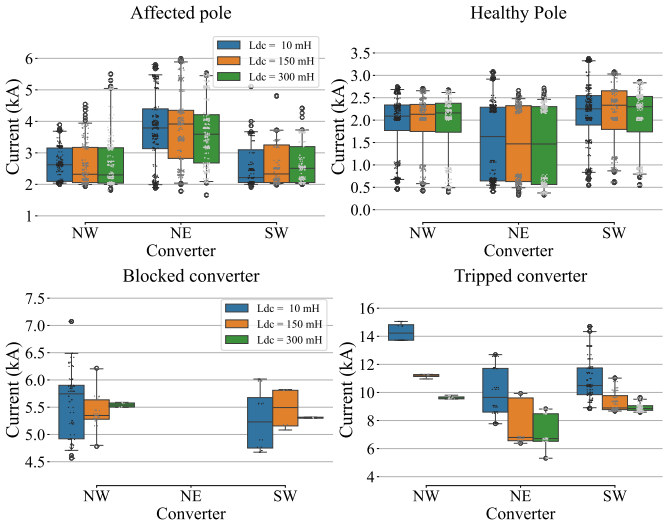

Fig. 6 Maximum SCC at DC-PoC and L_{DC}. Operational converters (Top): Affected pole (Left), Healthy pole (Right). Blocked converters (Bottom-Left) and Tripped (Bottom-Right)

Peak DC fault currents in the blocked state may reach 7 kA. In scenarios where faults are cleared by ACCB operation (with converters tripped), DC currents may rise to 15 kA, due to the opening delay (set here to 40 ms), but can be mitigated to 10 kA by increasing reactor size to 300 mH.

3.4 Pole-to-Neutral DC Temporary Overvoltage at DC-PoC

Fig. 7 confirms that converter-level overvoltages increase with larger DC-side reactor values. This effect is particularly pronounced at NE, likely related to the resonance phenomena discussed in Part II [4]. The maximum voltage on the affected pole increases from 650 kV up to 850 kV (Fig. 7, Top-right). In the lower voltage range, excursions reach 300 kV under minimal inductance and approach zero under the highest inductance setting, and may experience polarity reversal if the converter enters the blocked state (Fig. 7, Middle-Left). A similar trend is observed on the healthy pole, though with more moderate amplitude, limited to a few tens of kilovolts (Fig. 7, Bottom). By construction, the number of data points varies across figures, and for some converters that block in only a few cases, the bars appear very thin; this does not imply a lack of variation across scenarios for given settings in reality.

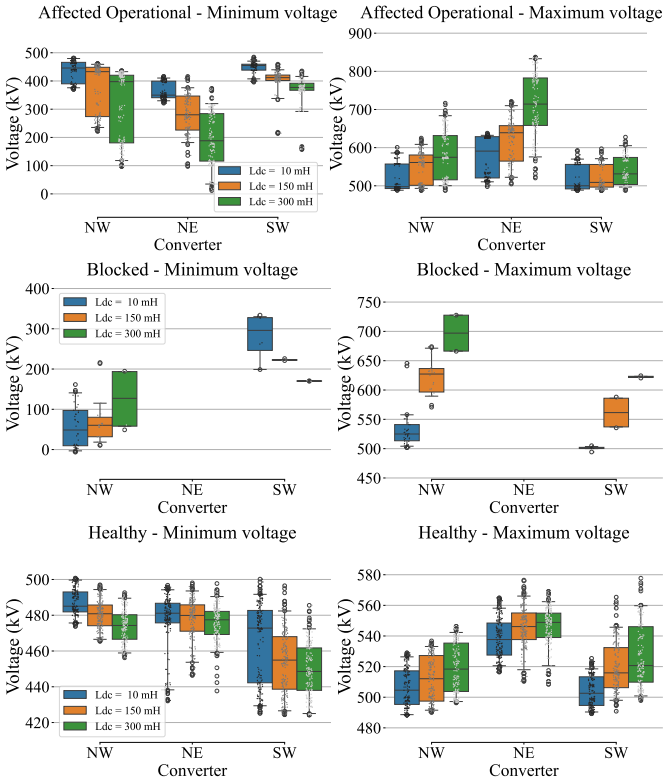

Fig. 7 DC voltage at DC-PoC and L_{DC}. Affected pole Operational converters (Top), Blocked converters (Middle) and Healthy pole (Bottom). Minimum (Left) and Maximum (Right)

3.5 Arm Currents

Since the blocking threshold is treated as an input, the arm current maximum, a key aspect of valve design, is reported only for blocked and tripped converters. Fig. 8 shows that, in the blocked state, maximum arm currents may reach between 5 and 6.5 kA depending on the DC reactor size (for a $T_{N,Max}$ of 5 ms). During tripping events, maximum arm currents range between 10 and 15 kA, aligning with maximum DC SCCs. At NE, DC SCC is relatively low because it is connected to an OWF, which feeds far less current than onshore grids, illustrating why the GGG configuration and strong AC grid assumptions represent the worst case from this perspective.

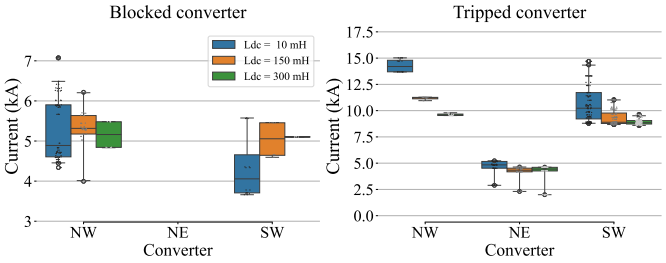

Fig. 8 Maximum arm current and L_{DC}. Blocked converter (Left) and Tripped converters (Right)

4 Results for Various Maximum Fault Neutralisation Times

This section discusses the impact on transient performance under DC faults of varying assumptions on the maximum fault neutralisation time while maintaining L_{dc} fixed at 150 mH. Section 4.2 addresses overall system behaviour, while Sections 4.3, 4.4 and 4.5 focus on DC SCC, DC voltage excursions and arm currents, respectively. As before, the TD response of one exemplary case is first presented in Section 4.1.

4.1 One Example in the Time-Domain

The same scenario presented in Section 3.1 is considered here, with full power transfer from NE to SW before a DC pole-to-ground fault is applied on Cable #2. As before, the fault is cleared by DCCBs at both ends, resulting in the isolation of Cable #2 and the disconnection of NW from the DC grid while it remains connected to the AC network. Fig. 9 illustrates the corresponding increase in maximum DC SCC with $T_{N,Max}$ and shows limited influence on the first voltage peak, as this is linked to fault inception. A more pronounced effect is observed on the second peak, associated with the clearing process. At SW, on the affected pole, the expected trend is visible: the slower the breaker operation, the higher the interrupted current and the resulting overvoltage. This effect becomes less evident at the other terminals. At NW, the behaviour reflects the recovery voltage imposed by the DCCB, simply shifted in time, while at NE, it is dominated by the response of the VF control mode. On the healthy pole the disturbance manifests within the *dynamic* time frame as it propagates via the DC voltage control.

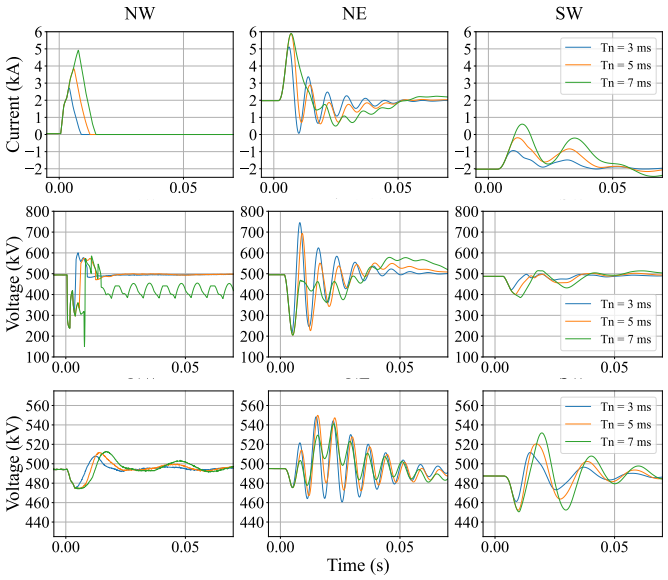

Fig. 9 NW (Left), NE (Middle), SW (Right). Affected pole DC current (Top), affected pole DC voltage (Middle), healthy pole DC voltage (Bottom). Pole-to-ground fault, Cable #2 (J2)

4.2 Overall Performance of the Protection Scheme

Similarly, the slower the DCCBs are in clearing the fault, the higher the resulting DC SCC maximum, thereby increasing the likelihood of converter blocking. For $T_{N,Max}$ equal to 3 ms, there are almost no blocking cases. As in previous cases, significant performance variations are observed at NW and NE for faults occurring in FSZs #1, #2, and #3. In the specific case of NE, FSZ #4 may also be included. For SW, the most relevant events in this regard are at DCSS #5 busbar (FSZs #3 and #4). It is noteworthy that none of the simulated faults lead to a situation where all converters (temporarily) block. However, for faults in FSZ #3, there are cases where no converter remains operational when $T_{N,Max}$ is set to 7 ms.

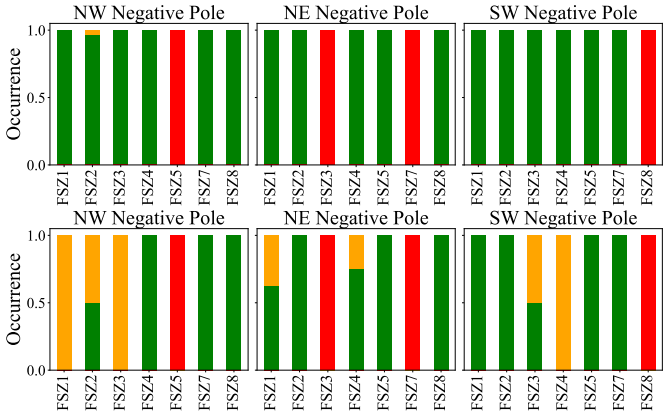

Fig. 10 AC/DC converter final state and $T_{N,Max}$ (L_{dc} =150 mH): (Top) 3 ms and (Bottom) 7 ms. Operational (green), Blocked (yellow) and Tripped (red)

4.3 DC Short Circuit Current at DC-PoC

Maximum DC fault currents are expected to increase with longer fault neutralisation times. This trend is clearly visible in Fig. 11, particularly at blocked NW and SW, with fault currents exceeding 7 kA when $T_{N,Max}$ is set to 7 ms. Nonetheless, this parameter has no influence the observed current when the AC/DC converter trips as intended, as the DC-side fault remains uncleared at the affected converter end, which continues to feed the short circuit. In such cases, the dominant delay is the ACCB operation time, during which the DC SCC reaches a *steady-state* value independent of $T_{N,Max}$. When the fault occurs between the converter (NW) and the DCCB, the fault is fed from the AC side. In SW, variability is explained by the fault location, which affects the equivalent impedance.

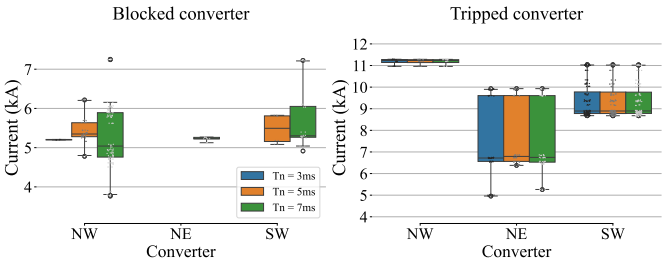

Fig. 11 Maximum SCC at DC-PoC and $T_{N,Max}$. Blocked converters (Left) and Tripped (Right)

4.4 Pole-to-Neutral DC Temporary Overvoltage at DC-PoC

Fig. 12 shows that the direct impact of the specified maximum fault neutralisation time (conservatively implemented in the simulations as the effective T_N) on voltage stresses is marginal. The associated risk arises indirectly via the DC-FRT requirements, and hence through T_{rec1}, which may necessitate larger reactor sizes. The resulting consequences were addressed in the assessment presented in the previous section.

4.5 Arm currents

Fig. 13 shows that slower fault neutralisation times impose greater stress on valve currents in the blocked state, with the maximum value increasing from less than 5 kA to more than 7 kA when $T_{N,Max}$ increases from 3 ms to 7 ms. As previously noted, this parameter has no impact on the maximum arm current in the case of converter trip, as the fault current is supplied from the AC side until the ACCB operates.

5 A Word about the Insulation Coordination

Transient design studies must also ensure that stresses in other subsystems, particularly along cables, within surge arresters and the grounding resistor, remain within acceptable limits.

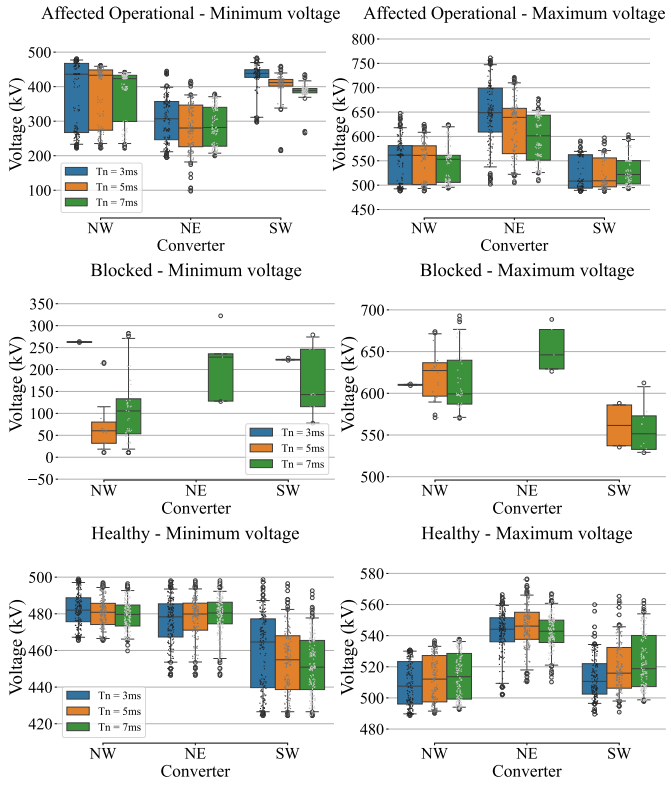

Fig. 12 DC voltage at DC-PoC and $T_{N,Max}$. Affected pole Operational converters (Top), Blocked converters (Middle) and Healthy pole (Bottom). Minimum (Left) and Maximum (Right)

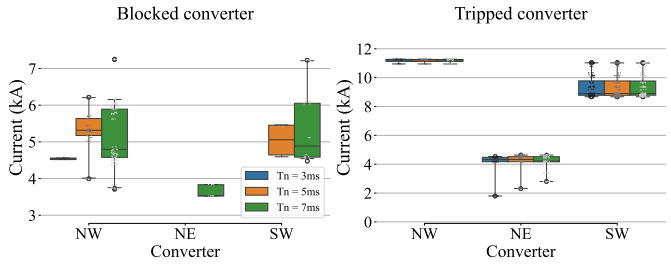

Fig. 13 Maximum arm current and $T_{N,Max}$. Blocked converter (Left) and Tripped converters (Right)

5.1 DC cable

To facilitate comparison, envelopes of the DC voltage trajectories observed along the cables, considering all measurement locations and scenarios, are computed, as illustrated in Fig. 14. For meaningful comparison, individual time series have been time-shifted to synchronise the voltage surge at fault clearance, compensating for propagation delays and, eventually, differences in DCCB operating speeds.

Bearing in mind the disclaimer in Section 2.2.3, Fig. 15 presents the resulting envelopes for different variants compared against the DC-TOV profile proposed in [5], to assess the sensitivity of results to design assumptions. Both the converter DC-side inductance value and the fault neutralisation time influence the first voltage peak.

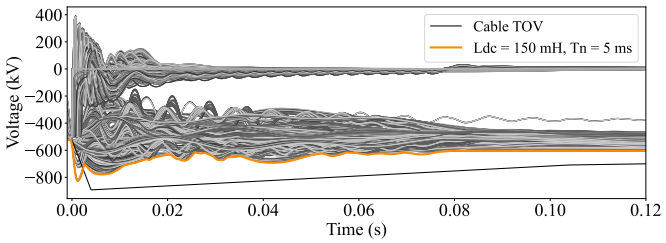

Fig. 14 Calculation of DC-TOV envelops from measurements along the DC cables (affected pole)

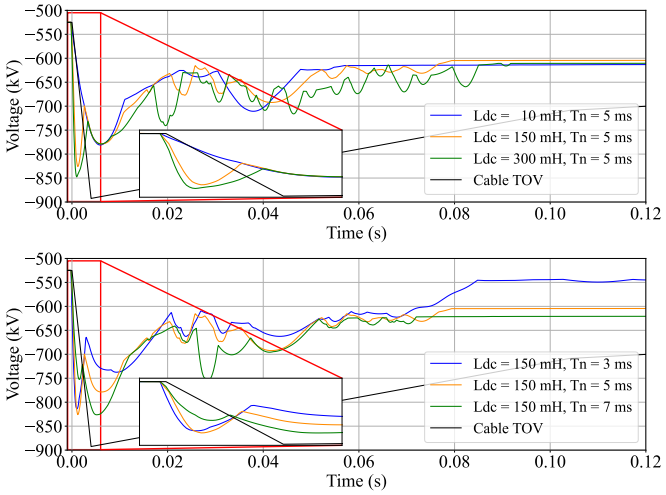

Fig. 15 DC-TOV along the DC cables (affected pole) for varying L_{DC} (Top) and $T_{N,Max}$ (Bottom)

However, the sensitivity is lower than that observed at the AC/DC converter DC-PoC. Additionally, beyond a certain threshold, surge arresters limit the peak amplitude, thereby reducing the influence of these parameters. In contrast, the second peak is primarily affected by the fault neutralisation time, following a more intuitive trend: slower operation tends to increase the constraint.

5.2 Surge Arresters

Fig. 16 shows the surge arrester energy absorption across all simulated scenarios. For the selected protective levels, pole arresters rarely conduct, and when they do, the absorbed energy remains very low (below 3 MJ). In contrast, neutral-system arresters tend to experience longer conduction periods, resulting in significant energy absorption exceeding 30 MJ; particularly at DCSS #3, associated with SW, and linked to faults in FSZ #8 caused by ACCB operation delays.

The trend with respect to fault neutralisation time is consistent and as expected, leading to a slight increase in absorbed energies, while remaining within the same order of magnitude. The impact of the converter DC reactor is minimal.

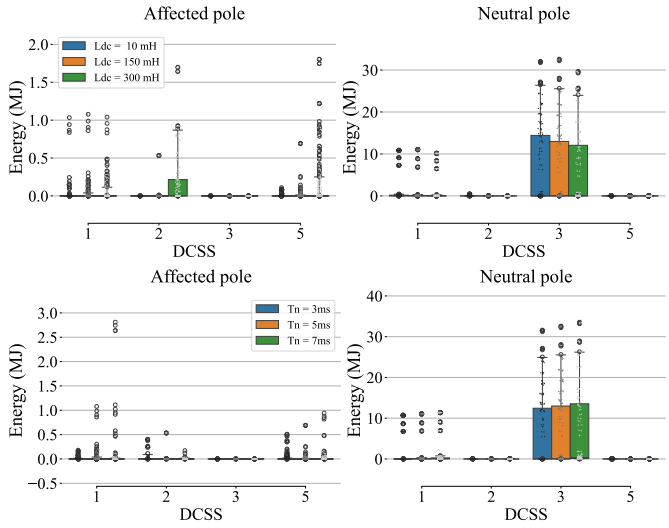

Fig. 16 Surge arrester energy for various L_{DC} (Top) and $T_{N,Max}$ (Bottom). Affected pole (Left), Neutral (Right)

5.3 Grounding Resistor

Fig. 17 shows similar trends in the fault current through the grounding resistor, which increases with both parameters. The associated energy, approaching 40 MJ in the InterOPERA design study setup, varies only marginally with the parameters.

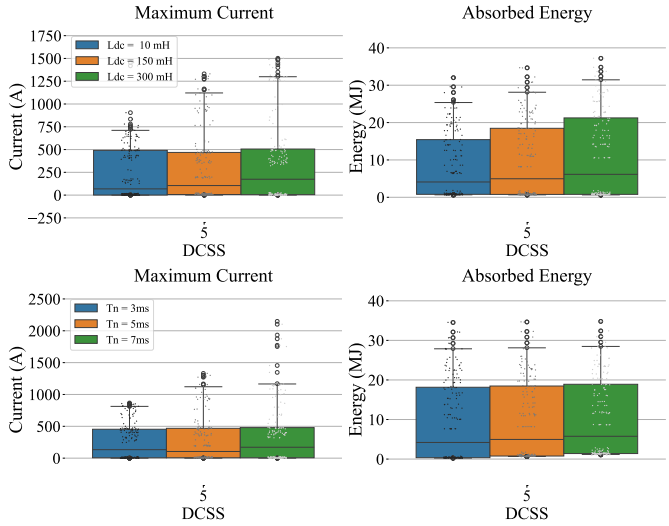

Fig. 17 Current (Left) and energy (Right) on the grounding resistor for various L_{DC} (Top) and $T_{N,Max}$ (Bottom)

6 Conclusion and Discussion

This work builds on pre-design study methodologies, addressing data unavailability challenges and the need for standardisation introduced for P2P systems, to conduct HVDC grid design studies for the InterOPERA demonstrator.

It primarily focuses on the unique constraints introduced by the MT setup, particularly the integration of DCSSs and the potential interoperability issues—broadly understood beyond control interactions—that may arise within the MV framework. The InterOPERA demonstrator includes several DCCBs, which, together with the 200 mH inductance assumed per DCSU with fault separation capabilities, result in relatively low SCC peaks at the DC grid side, even for *slow* DCCBs and low converter reactor values. In this scenario, the main challenges are ensuring DC-FRT from AC/DC converters and understanding the impact of various OEM design choices on the overall system, which may typically manifest as overvoltages.
In InterOPERA, compliance with DC-FRT requirements is enforced through standalone tests [1], while accounting for the capabilities of readily available solutions to accommodate all vendors in the demonstrator; specifically, DCCB speed and converter current ratings. To facilitate compliance, temporary blocking is considered allowed and available, although the System Operator may choose otherwise in practice. At early project stages, defining location-specific settings may not be feasible; therefore, this work presents and generalises the proposed methodology for HVDC grid transient design studies. The pole-to-neutral DC voltage operating ranges, covering both transient and dynamic time frames, identified in this work from DC pole-to-ground faults are presented in Section 6.1. Section 6.2 extends the key findings to other configurations (GGG and WWG), proposing operating range requirements by station type irrespective of location. Section 6.3 discusses the DC-FRT requirements applied to the InterOPERA demonstrator.

6.1 Requirements on Operating Ranges

The main outcome of this study are the maximum DC voltage excursions outside Operational Security Limits (OSLs) recorded at the converters' DC-PoC during DC faults and throughout the clearing process. As a reminder, in InterOPERA, DC voltage OSLs are defined based on the continuous operating range of 525 kV DC cables [3, 4]. Results are shown in Figs. 18 and 19, aggregated by station type: onshore (Top, including NW and SW) and offshore (Bottom, NE only), while distinguishing between final states, i.e., whether the converter maintained normal operation (Left) or blocked (Right).
Consistent with previous observations, DC voltage excursions increase with the size of the converter DC reactors, both in peak value and dynamic range. For example, in operational converters at NW and SW, overvoltages may rise from 1.2 pu to 1.4 pu, and reach up to 1.7 pu at NW for the largest considered L_{DC} value. The impact of $T_{N,Max}$ is more moderate, though still notable in blocked converters, not in terms of magnitude, but in the duration of the overvoltage. These results support the definition if the DC-FRT profile settings. Since the deblocking functionality was not implemented in the generic model, the observed dynamic ranges do not fully reflect the expected system behaviour over the dynamic time frame ($\approx$ hundreds of milliseconds). Analysing the system response with converters in the blocked state allows, nonetheless, characterising the

conditions under which deblocking may be required, thereby supporting the definition of the requirement.

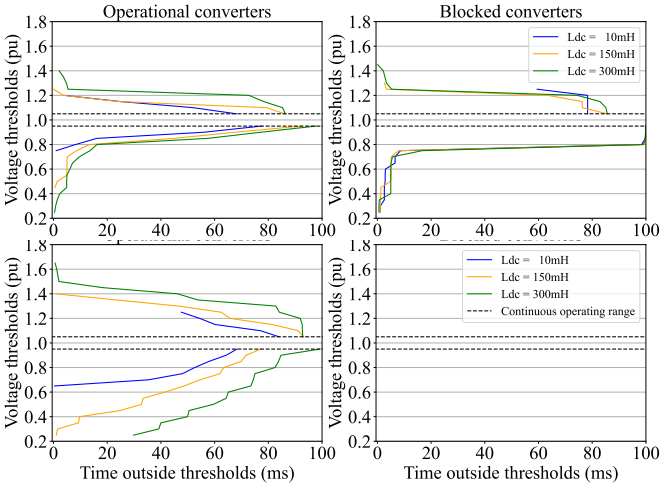

Fig. 18 Time outside OSLs for various L_{DC} ($T_{N,Max} = 5$ ms). Operational (Left), Blocked (Right). Onshore (Top), Offshore (Bottom)

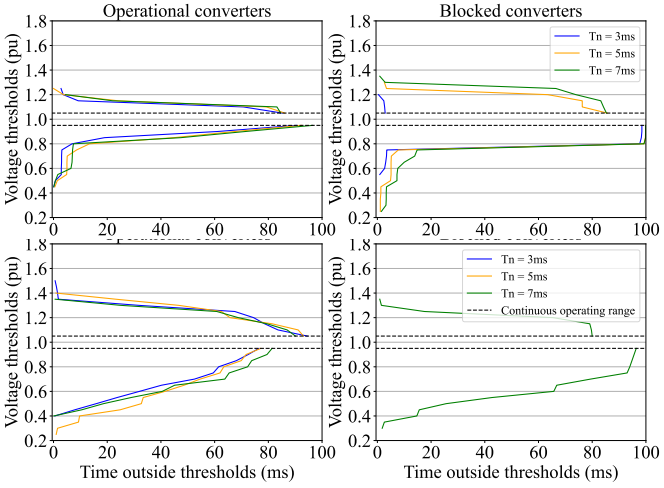

Fig. 19 Time outside OSLs for various $T_{N,Max}$ ($L_{DC} = 150$ mH) Operational (Left), Blocked (Right). Onshore (Top), Offshore (Bottom)

6.2 On the Configurations: Onshore vs. Offshore Stations

As shown in the previous two parts [3, 4], the GGG configuration is favourable from both static and dynamic perspectives, as more units contribute to the DC voltage control. However, this is not always the case from a transient viewpoint, particularly under the assumption of strong onshore AC grids, where fault current contributions tend to be higher for GGG. Fig. 20 shows the configuration impact on the observed DC voltage envelops.

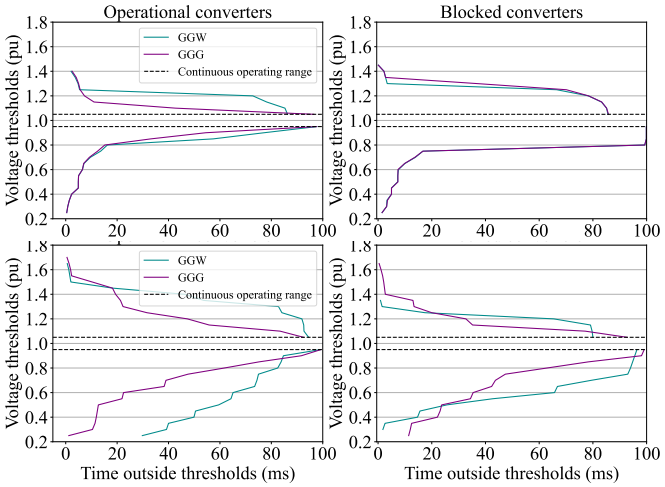

Fig. 20 Time outside OSLs all variants and configurations. Onshore (Top), Offshore (Bottom)

6.3 Discussion on DC-FRT standalone test

InterOPERA functional specification defines DC-FRT requirements by time-dependent DC voltage profiles [1]. Compliance is demonstrated through dedicated standalone test, whose parameters depend on the selected value of T_{rec1}, as outlined in Tab. 1. Provided the subsystem passes this test, OEMs are free to implement any combination of reactor size and current capability. For the T_{rec1} and L_{dc} values considered in this study, the resulting minimum current capability (understood here as the maximum permissible arm current in the blocked state, before triggering an irreversible trip) can be estimated, reaching up to 20 kA in the worst case (highest $T_{N,Max}$ and smallest reactor).

Table 1 Maximum arm current in standalone test (kA)

Test Parameters	T_{rec1} / U_{UV1}	3 ms -0,52 p.u.	5 ms -0,38 p.u.	7 ms -0,25 p.u.
L_{DC}	10 mH	16	20	20
	150 mH	9	12	13
	300 mH	7	8	10

Observed values in system-level simulations remain below 8 kA, indicating maximum arm current levels that are significantly lower than those observed in standalone tests. While effectively ensuring conservativeness, DC-FRT requirements based on voltage profiles may, depending on the applied level of selectivity, prove overly restrictive as reported in the literature [18].

Additionally, standalone test circuits deliberately omit current-limiting contributions from other subsystems, requiring each unit to provide sufficient inductance independently to limit current rise. In actual grid-connected conditions, however, limitation of the current rise is collectively supported by all interconnected subsystems. Moreover, advanced functionalities, such as proactive action and current-limiting strategies, if available, may offer further opportunities for design optimisation.

7 Acknowledgements

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