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B4 DC systems and power electronics**PS3 New technologies and concepts of DC and FACTS enabling energy transition****Insulation coordination in bipolar multi-terminal HVDC grids****Benoît DE FOUCAUD*****RTE****France****benoit.foucaud@rte-
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france.com****SUMMARY**

Driven by large-scale offshore wind integration targets, HVDC technology is evolving from traditional point-to-point links toward meshed, multiterminal (MT), multivendor (MV) HVDC grids, for which interoperability must be de-risked; the core objective of the InterOPERA project. To support the definition of functional specification, a study process for early-stage HVDC grid design based on generic models and EMT simulations has been proposed and applied to the three-terminal demonstrator base case. This paper presents both the general methodology for conducting preliminary insulation coordination studies and the transient analysis of DC faults in the ± 525 kV (highest voltage), 2 GW bipolar benchmark. Key outcomes include the validation of DC-side equipment withstand voltage requirements and the definition of suitable neutral system parameters. Numerical results illustrate the need for a coordinated assessment of the grounding configuration and the surge arrester design, providing guidance on the standardisation efforts required to support the development of future MT MV HVDC grid.

KEYWORDS

Multi-terminal HVDC grids, Bipolar HVDC, Insulation coordination, DC circuit breakers.

1 Introduction

High Voltage Direct Current (HVDC) systems have traditionally been delivered as closed solutions, entirely designed by Original Equipment Manufacturers (OEMs) in accordance with technical specifications defined at the AC Point of Connection (AC-PoC) on both sides. More recently, system owners, typically Transmission System Operators (TSOs), have moved towards unbundling the procurement of AC/DC converter stations and cable systems, creating a need for pre-design studies to support the definition of requirements at the DC-side interface. These studies often rely on Electromagnetic Transient (EMT) simulations using generic models adjusted with project-specific data, typically focusing on the characterisation of DC short-circuit currents (DC-SCC) and temporary overvoltages (DC-TOV). To minimise pre-design study efforts, previous work has sought to define common specifications applicable across similar HVDC projects [1]. A crucial challenge is balancing the required level of conservatism with the risk of overdesign to ensure cost-effectiveness despite data uncertainty, a task made even more complex in a Multi-Vendor (MV) context.

A key topic addressed by several international working groups and standardisation committees concerns DC cable qualification; specifically, the definition of requirements and testing procedures that reflect realistic electrical stress conditions [2]. Once voltage withstand levels are established across the full range of transient, from fast to slow-front waves, and dynamic phenomena, guidelines can be developed to support insulation coordination studies. These guidelines are particularly relevant for defining protective levels, e.g., for surge arrester design.

In this context, the IEC 60071 series, particularly Part 11, partially addresses HVDC applications [3], with a primary focus on DC switchyard equipment. Although originally developed for Line-Commutated Converter (LCC) systems, considerable efforts have since been made to extend its applicability to Voltage-Sourced Converter (VSC)-based schemes. However, the specific challenges associated with emerging topologies such as bipolar and Multi-Terminal (MT) configurations are only beginning to be fully understood. In the particular case of bipolar systems, there are currently no standardised practices for rating the Dedicated Metallic Return (DMR), and existing cable testing procedures may not adequately represent the expected electrical stresses. Extensive parametric investigations reported in [4], highlight the significant influence of specific system design parameters, such as protection settings, grounding resistor value, and assigned protective levels, on the results.

Within the InterOPERA project, an MT HVDC grid design study process was proposed and applied to the demonstrator (see previous work [5] [6] [7]). Specifically, [7] investigated the impact of different assumptions on DC circuit breaker (DCCB) fault separation capabilities and AC/DC converter DC side reactor values on the transient stresses recorded at subsystem interfaces. In short, when DC fault ride through (DC-FRT) requirements are applied, depending on the considered maximum fault neutralisation time, increased reactor values may become necessary to comply with limited current capability constraints. This, in turn, can affect system overvoltages at fault clearance. Although surge arresters may ultimately limit maximum voltage levels, the resulting absorbed currents and energies may become excessively high and unevenly distributed among subsystems, potentially requiring a revision of the overall system design.

This work presents further details on the preliminary insulation coordination study conducted for the InterOPERA demonstrator design, with the main contributions summarised as follows:

1. **A general methodology** to incorporate insulation coordination aspects into HVDC grid transient design studies using generic models is proposed.
2. **Application of the methodology to the InterOPERA demonstrator** setup provides insight into the expected electrical stress levels in such systems.
3. **A parametric analysis** highlights the sensitivity of key electrical stress metrics to:
 - system-level design parameters, such as the grounding resistor value,
 - subsystem requirements, such as withstand voltages, and
 - subsystem design parameters within the OEM scope that are typically uncertain during early-stage studies, such as surge arrester characteristics including the protective levels at both the High Voltage (HV) poles and the neutral system.

Section 2 outlines the scope and key assumptions of this study. Sections 3 to 5 present simulation results, beginning with DC faults. The risk of current non-zero crossing during AC single-phase faults on the converter side is discussed in Section 6. Finally, conclusions are presented in Section 7.

2 Scope, assumptions, methodology and modelling

The InterOPERA demonstrator is based on 2 GW bipoles with a highest system voltage of 525 kV and a DMR. Two topologies are considered: a three-terminal (3T) and a five-terminal (5T) configuration, comprising three and five AC/DC converter stations, respectively [8]. Design studies and this work focus on the **3T base case** illustrated in Figure 1, which features four DC Switching Stations (DCSSs). Only two DCSSs are equipped with DC Circuit Breakers (DCCBs), located at the North-West (NW, DCSS #1) and at the central station (DCSS #5).

2.1 Fixed parameters: fault neutralisation time, reactors, DC cable and AC side data

Two different types of models, denoted A and B in Figure 1, are used to represent the two DCCB technologies available in InterOPERA. As in [7], they are parameterised to yield equivalent fault neutralisation times (T_N), set here to **5 ms**. The reactors at the DC Switching Units (DCSUs) equipped with DCCBs are set to **200 mH**. The AC/DC converter generic model includes an arm inductance of **35 mH** and a DC-side reactor of **150 mH**. Wideband models are employed to capture the frequency-dependent behaviour of the DC cables, based on the data in [9]. For fault inception and overvoltage monitoring along Cables #2 and #4, each 350 km long, 50 km sections are implemented, resulting in seven identical sections per cable¹.

The DC-TOV profile proposed in [8] is adopted for the DC poles. Onshore grids are considered strong (43 GVA) and represented by Thevenin equivalents, while offshore grids are represented using aggregated Wind Power Plant (WPP) generic models. Further details are provided in [7].

¹ The choice of section length represents a compromise between wideband model accuracy (generally higher for longer sections) and the ability to assess internal cable faults. Uniform segmentation is adopted for simplicity, but alternative approaches, such as selecting critical locations to include grounding points near faults, may be more appropriate if detailed cable data are available, particularly when the study focuses on the cable system itself.

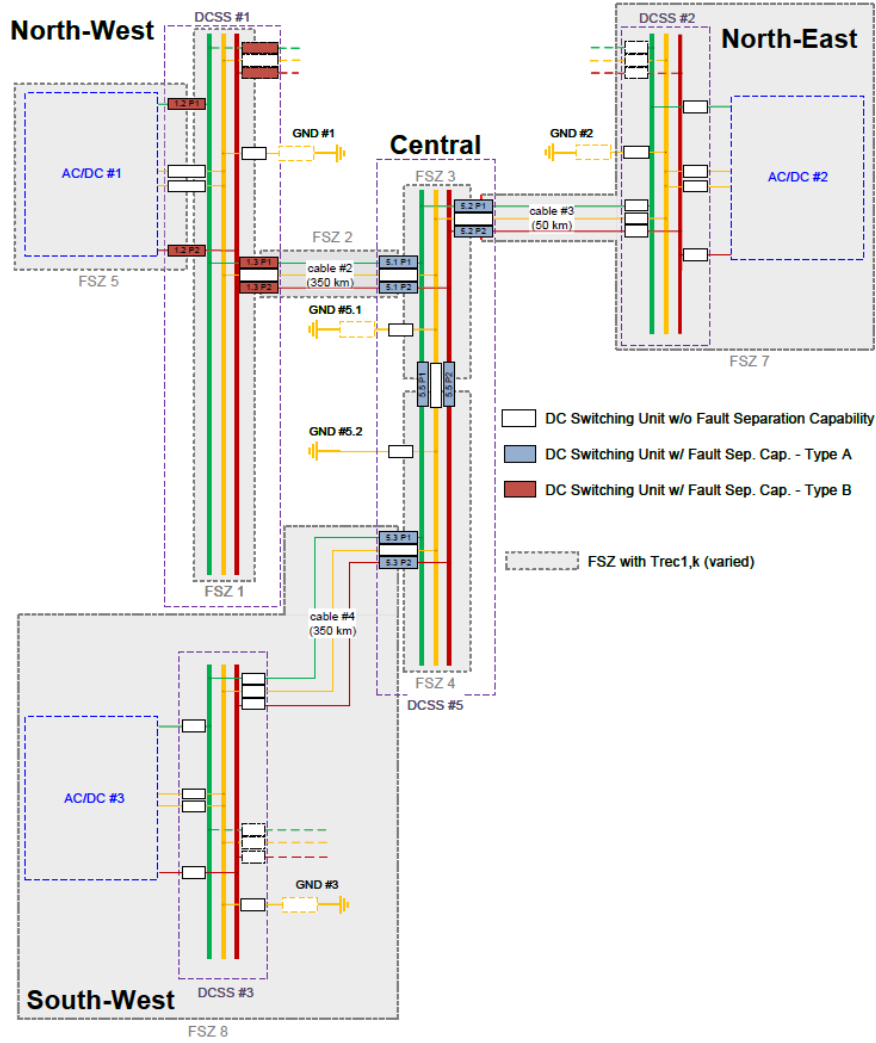


Figure 1 – 3T DC grid topology showing DCCB locations resulting in seven Fault Separation Zones (FSZs)

2.2 Assumptions on the pole withstand voltages

IEC and CIGRE recommend different Switching Impulse Withstand Voltage (SIWV) values for 525 kV HVDC systems [2] [3]. For the InterOPERA demonstrator, a preliminary **SIWV** of **1050 kV** is adopted, representing an intermediate value within the IEC range (refer to Table C.1 in [3]). Based on this SIWV, two possible Lightning Impulse Withstand Voltages (**LIWVs**) are defined: **1050 kV** and **1175 kV**. The results for both cases are compared in Section 5.

2.3 Assumptions on the surge arrester characteristic and pole protective levels

As in [7], the generic voltage-current (V/I) characteristic defined in IEC 60071-11 [3] is used to model surge arresters, which are installed at subsystem interfaces and DCSS busbars. The pole Lightning Impulse Protective Level (**LIPL**), defined at 10 kA, is set to **875 kV** and **980 kV** by applying a safety factor of 1.2 to the two selected LIWVs (1050 kV and 1175 kV), following the recommendations of IEC 60071-11 (refer to Table 3 in [3]). It is worth noting, however, that the standard does not account for the presence of DCCBs. Figure 2 shows that these settings result in a vertical translation of the V/I characteristic, anchored at a single reference point (the LIPL at 10 kA), with all other points on the curve scaled accordingly.

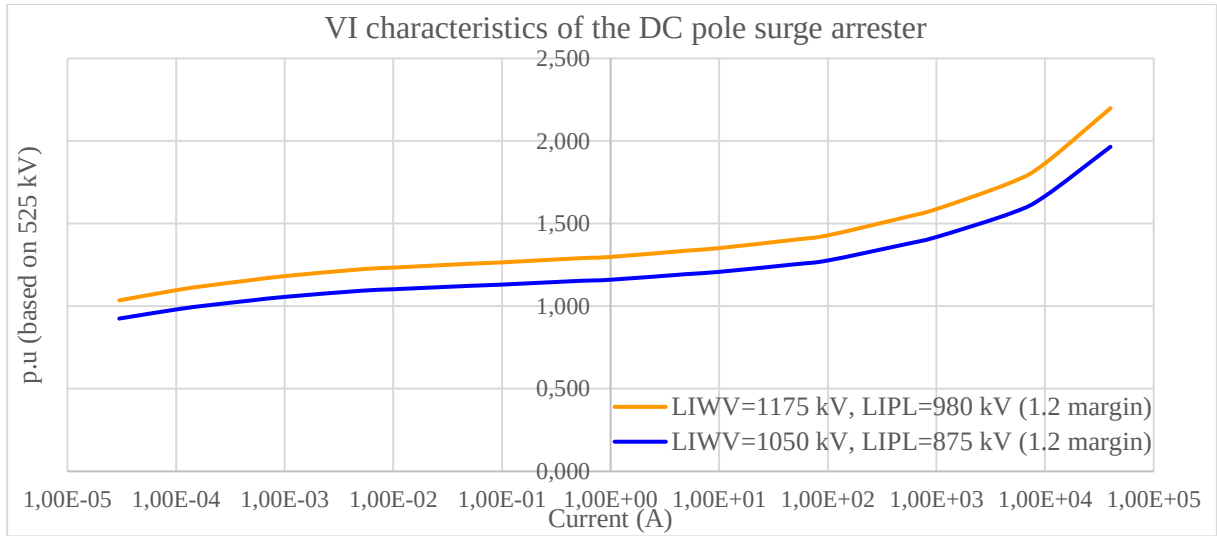


Figure 2 – Implemented VI characteristic for the pole arresters, based on [3] and selected LIWV

2.4 Assumptions on DMR rating and protective level

Under steady-state conditions, the DMR current and voltage are close to zero when all units are available and remain very low during asymmetrical operation. In practice, the DMR's rated voltage is defined based on the system's transient response to DC faults rather than its maximum continuous operating voltage. As demonstrated in this work, broader performance criteria may also influence the required protective level, as the system response is highly sensitive to the characteristics of the earth return path. In InterOPERA, the DMR rating was derived from the required protective level, an outcome of the insulation coordination study; thus, applying a reverse logic compared to the conventional approach used for pole cable design. Here, only the insulation thickness is reduced relative to the pole cables (11 mm instead of 26 mm), and three LIPL cases are considered: **83 kV**, **100 kV**, and **125 kV** (at 10 kA). The IEC generic voltage-current (V/I) characteristic displayed in Figure 2 is scaled accordingly

2.5 Assumptions on the neutral system grounding

The neutral system is considered grounded at the central DCSS (#5) under normal operation. Other grounding locations may be used in degraded modes (e.g., DCSS #5 unavailability); however, this study is limited to the nominal topology. Three additional cases with different grounding resistor values are defined: **0.001 Ω** (representing solid grounding), **5 Ω** , and **10 Ω** .

2.6 Scenarios

In InterOPERA, various configurations in terms of station type (onshore/offshore) at each location are explored. In this work, as in [7], the focus is placed on the GGW (Grid-Grid-Wind) case for brevity, meaning that both western stations (NW and SW) connect to onshore grids and operate in P-Vdc voltage droop control mode, while the NE station connects to an offshore WPP and operates in VF control mode. Eight initial operating points are considered, covering two different DC voltage profiles and full-power import (2 GW into the AC grid), full-power export (2 GW into the DC grid), and near-zero power for the onshore stations; for the offshore station, only the latter two conditions apply. Twenty-two events are analysed, including:

- 18 DC cable faults: 2x8 locations along the two 350 km cables (modelled by seven 50 km sections), plus both ends of Cable #3 (modelled as a single 50 km section),
- the NW DC Point of Connection (DC-PoC), and
- three busbar faults (one in DCSS #1 and two in DCSS #5 which have a coupling DCCB).

This results in **176 scenarios** for each of the eight cases (1408 total). It is worth noting that only Cable #2 is equipped with DCCBs at both ends, whereas DC faults on Cables #3 and #4 can only be cleared by ACCB operation, leading to the disconnection of the affected converter unit.

3 Simulation results: neutral system protective level

This section investigates the impact of varying the neutral system protective level assumptions on electrical stresses across different subsystems. The grounding resistor value is fixed at 5Ω , and the HV pole LIPL is set to 980 kV (corresponding to a LIWV of 1175 kV). Variations of these parameters are discussed in the subsequent sections 4 and 5, respectively.

3.1 A time-domain example

Scenario:

- Initial operating conditions: power transfer from NE to SW, DC voltage at NE = 505 kV.
- Event: DC fault at cable #4 (FSZ #8), i.e., SW converter station DC-PoC, negative pole.

The *unaffected* part of the DC grid is first quickly (≈ 5 ms) separated from the fault by the DCCB located at the central DCSS (negative pole only). However, the fault continues to be fed from the converter side until it is cleared by ACCB operation, occurring after approximately 80 ms. The affected converter unit (SW negative pole) blocks shortly after fault inception, as the arm current exceeds the predefined generic protection threshold (3.5 kA). Throughout this process, the disturbance continues to propagate through the DMR. Figure 3 shows that, although the DMR protective level has a negligible impact on the total fault current, the distribution of current between the grounding resistor and the neutral system surge arrester varies significantly.

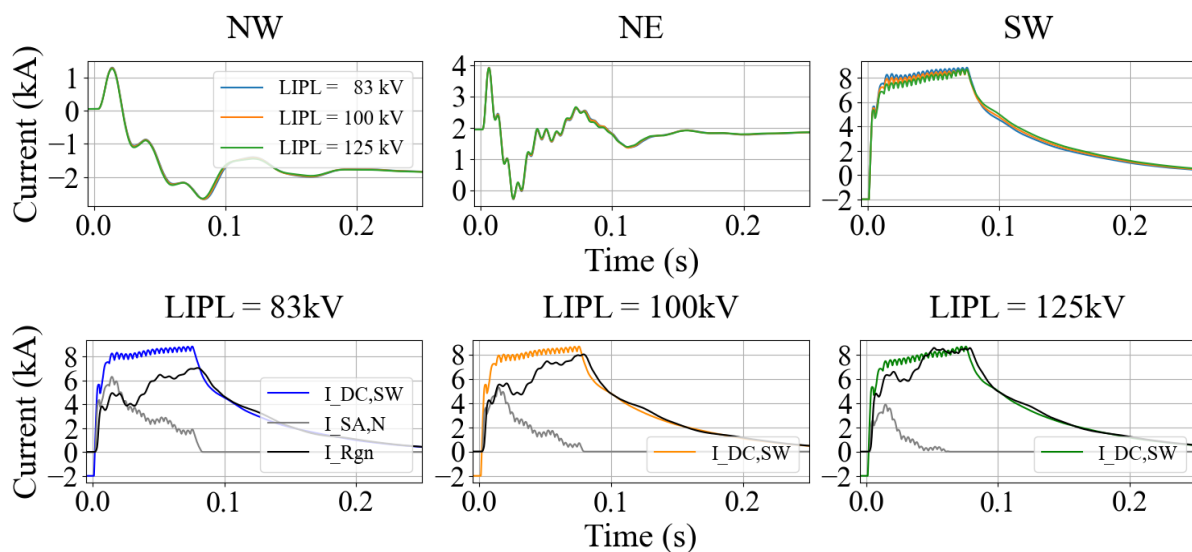


Figure 3 – DC current on the affected pole for varying neutral LIPL (grounding resistor= 5Ω). Converter terminals (top), neutral arrester and grounding resistor sharing at SW (bottom)

Specifically, the DC fault current reaches approximately 8 kA in all three variants, while the arrester peak current, in grey, increases from 4 kA to 6 kA as the protective level decreases from 125 kV to 83 kV. Figure 4 shows that the overvoltage at the DMR following a DC fault exhibits a characteristic plateau extending over the dynamic range ($\approx$ hundreds of milliseconds), closely matching the assigned LIPL, consistent with findings reported in the literature [4].

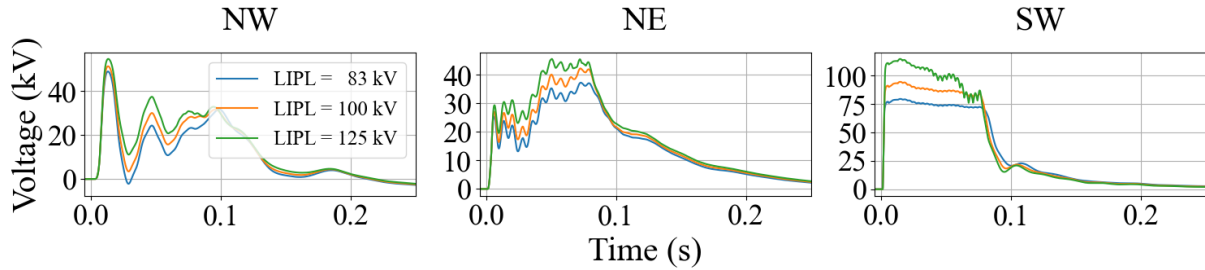


Figure 4 – DC voltage at the neutral point for varying neutral LIPL (grounding resistor=5 Ω)

The voltage reduction associated with lower LIPLs is, however, insufficient to offset the corresponding increase in arrester current, leading to higher absorbed energies. The neutral arrester absorbs 9 MJ in the 125 kV LIPL case, 15 MJ when the LIPL is set to 100 kV, and 19 MJ for an 83 kV LIPL, while the grounding resistor energy absorption shifts from 29 MJ to 23 MJ and 18 MJ across the same cases. In this scenario, no surge-arrester conduction is observed on the HV poles.

Figures 5 (affected pole) and 6 (healthy pole) show that while increasing the neutral system LIPL, which ultimately implies a higher DMR rating, may alleviate energy constraints in surge arresters, it does so at the expense of greater disturbance propagation to the healthy pole voltage when measured to ground (see Figure 6, bottom). In contrast, pole-to-neutral voltages (tops), which are controlled by the AC/DC converters, remain largely unaffected.

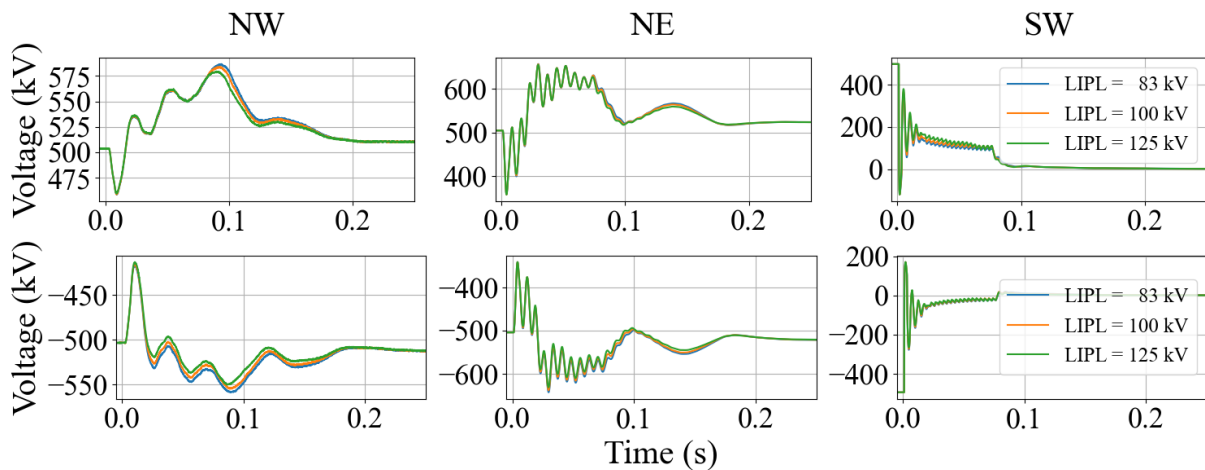


Figure 5 – DC voltage on the affected pole for varying neutral LIPL (grounding resistor=5 Ω). Pole-to-Neutral (top), Pole-to-Ground (bottom)

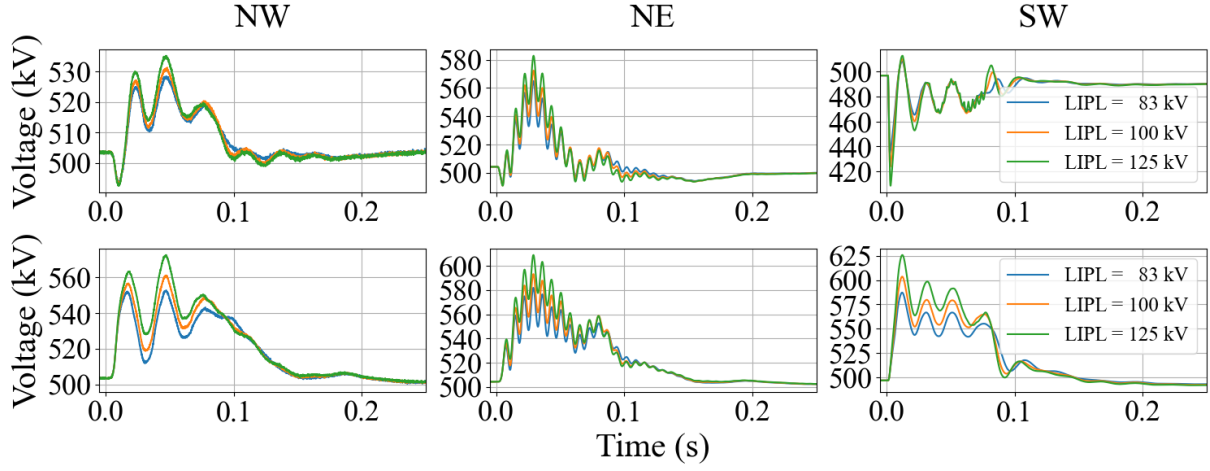


Figure 6 – DC voltage on the healthy pole for varying neutral LIPL (grounding resistor=5 Ω). Pole-to-Neutral (top), Pole-to-Ground (bottom)

3.2 Aggregated results: all scenarios

Figure 7 (left) shows the DMR overvoltages for the base case (neutral LIPL of 83 kV and a 5 Ω grounding resistor). A maximum envelope, shown in blue, is derived from the time-domain signals across all measurement locations and 176 scenarios. For a meaningful profile synthesis, individual curves are time-shifted to align the voltage surges at the instant of fault clearance, thereby compensating for propagation delays. Figure 7 (middle) compares the resulting DMR overvoltage envelopes for varying neutral LIPL assumptions, while Figure 7 (right) presents the corresponding results for the healthy pole-to-ground voltage. Preliminary observations from the previous section are generalised, confirming the **higher sensitivity of the healthy pole DC voltage** to this parameter. Across the three variants considered, surge arresters conduct primarily at the neutral system and, to a lesser extent, on the affected pole, due to the temporary voltage excursions in the surviving parts during recovery after fault clearance. Figure 8 (middle) shows that, as before, the energy absorbed by the neutral system arresters decreases with increasing protective level, whereas the **energy dissipated in the grounding resistor tends to increase** (Figure 8, right). The box represents the interquartile range ($\pm 25\%$), and the whiskers extend to the 5th and 95th percentiles. Figure 8 (left) also indicates that, in the cases where the affected pole arresters conduct, the associated energy absorption remains very limited.

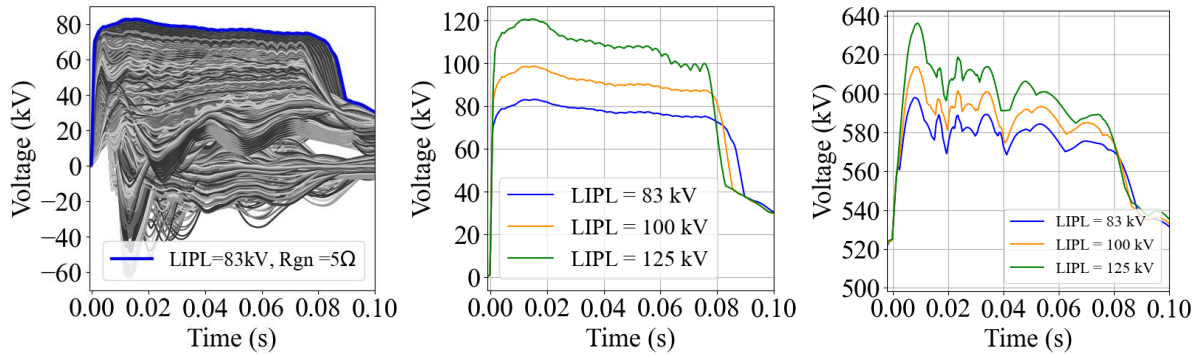


Figure 7 – Maximum voltage envelopes for varying neutral LIPL. DMR (left and middle), healthy pole (right)

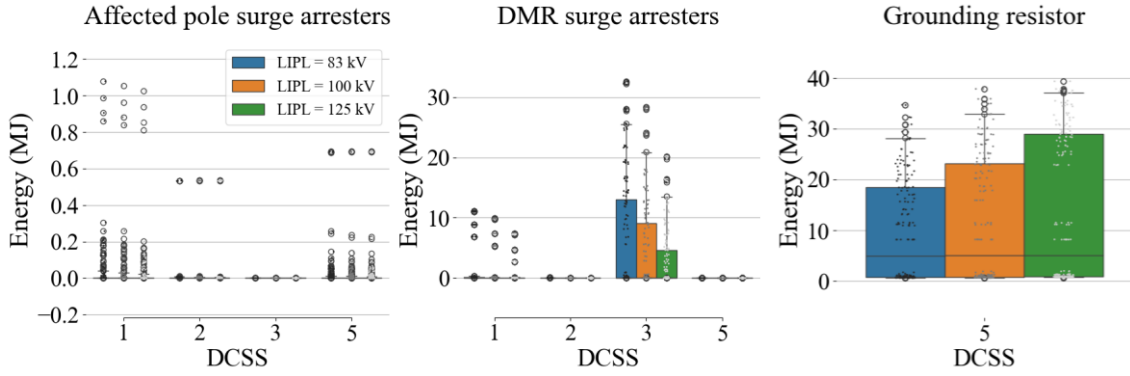


Figure 8 - Absorbed energy at the affected pole arrester (left), neutral surge arrester (middle) and grounding resistor (right) for varying assumptions on the neutral system protective level (grounding resistor=5 Ω)

4 Simulation results: grounding resistor

This section investigates the impact of varying grounding resistor assumptions on the dielectric stresses at different subsystems. By default, the pole LIWV remains at 1175 kV (LIPL equal to 980 kV), and the neutral LIPL is set to the lowest considered value (83 kV).

4.1 A time-domain example

The same scenario as in Section 3.1 is considered, involving a DC fault at the SW converter DC-PoC affecting only the negative pole while the converter operates at full power in inverter mode. Figure 9 shows that lower grounding resistor values lead to reduced neutral voltage excursions in the remote stations. Near the fault location, the maximum neutral voltage remains limited by the assigned protective level; however, the overvoltage duration tends to decrease as the grounding resistance is reduced. Finally, Figure 10 shows that, after AC-side fault isolation, the decay of the converter's inductive current accelerates with higher neutral resistance.

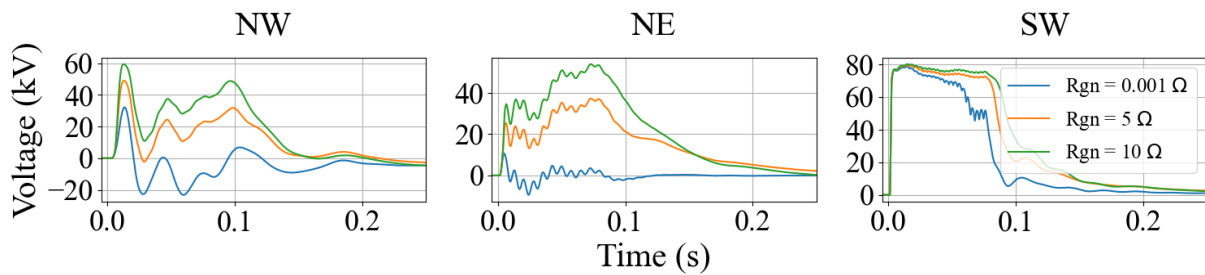


Figure 9 - DC voltage at the neutral point for varying grounding resistor (Neutral LIPL=83 kV)

As before, a larger portion of the fault current shifts toward the arrester as the grounding resistor value increases. For the selected scenario, the neutral arrester peak current and absorbed energy at SW increase from 5 kA and 10 MJ to 7 kA and 26 MJ, respectively, when the grounding resistor value is raised from 0.001 Ω to 10 Ω . Figure 11 shows the pole-to-ground voltage at the converter terminals, again exhibiting an inverse trend between the HV poles driven by the neutral shift, which is reduced in the surviving areas under solid-grounding conditions.

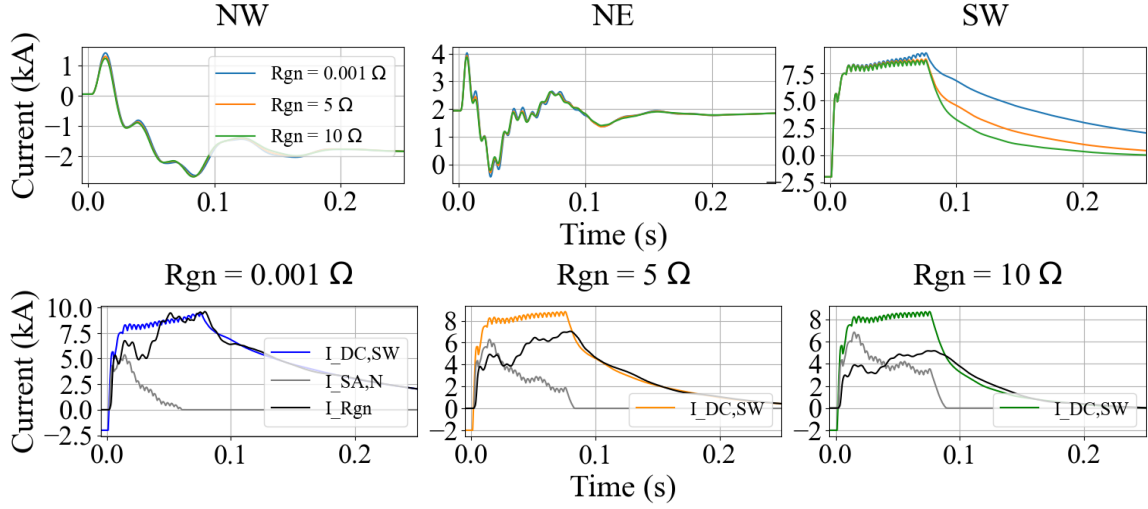


Figure 10 - DC current on affected pole for varying grounding resistor (neutral LIPL=83 kV). Converter terminals (top), neutral arrester and grounding resistor sharing at SW (bottom)

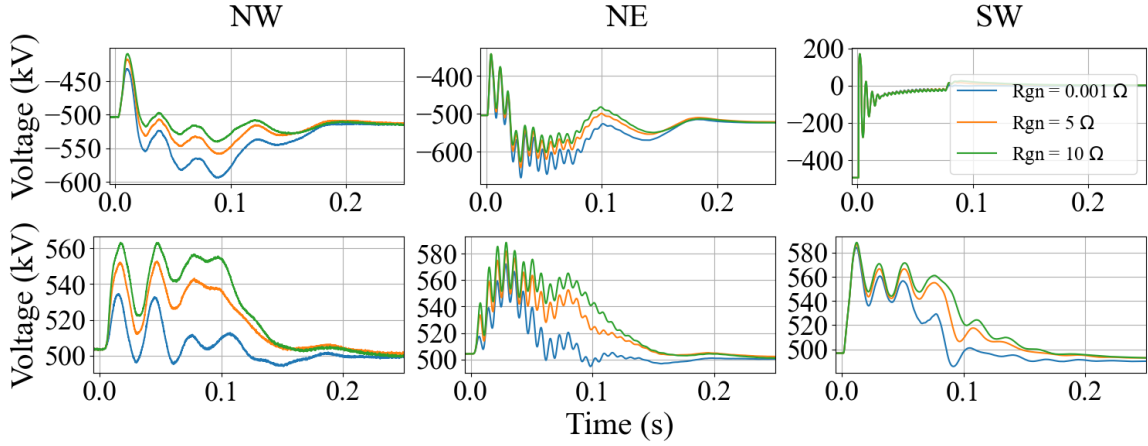


Figure 11 – Pole-to-ground DC voltage on HV poles for varying grounding resistor (neutral LIPL=83 kV). Affected pole (top), healthy pole (bottom)

4.2 Aggregated results: all scenarios

Figure 12 shows that, while the neutral surge arresters remain effective in limiting overvoltages across different grounding resistor values, the maximum value of the envelope remains essentially unchanged. However, the duration of the overvoltage increases as the grounding resistance becomes larger, which in turn affects how the absorbed energy is distributed among the surge arresters (see Figure 13). Although the energy absorbed by the arresters on the affected pole decreases with increasing grounding resistance, the solicitation of the neutral arresters rises from 22 MJ (solid grounding) to 40 MJ (10 Ω), with all other parameters kept constant. It must nonetheless be noted that, as reported in [7], the energy absorbed by the affected pole arresters is proportionally sensitive to the AC/DC converter reactor values and the DCCB fault neutralisation times, and inversely proportional to the pole LIPL (see Section 5). For solid grounding, the current provides a clearer indication of the stress on the grounding point, which, as expected, decreases from 12.6 kA to 6 kA as the grounding resistor value increases. The impact on energy is minor, owing to a compensating increase in the overvoltage duration.

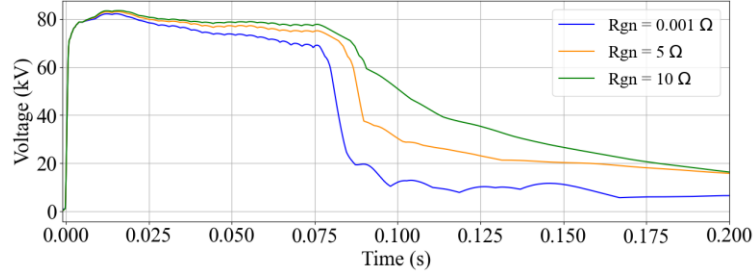


Figure 12 - DMR voltage envelope in the 3T system for different grounding resistor (neutral LIPL=83 kV)

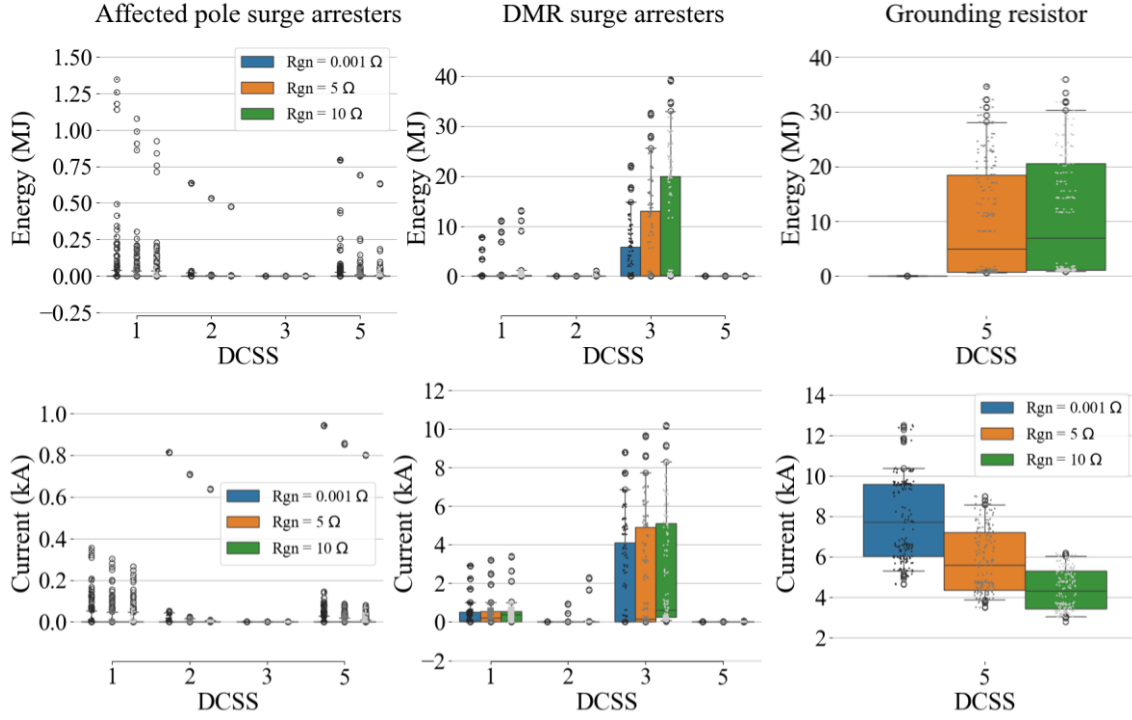


Figure 13 – Absorbed energy (top): affected pole surge arrester (left), DMR surge arrester (middle), and grounding resistor (right) for different grounding resistor (neutral LIPL=83 kV). Absorbed current (bottom)

5 Simulation results: HV pole protective level and DC grid configuration

Lastly, increasing the protective level of the HV poles naturally allows extreme cases to approach more closely the assigned DC cable TOV profile (see Figure 14, left) and reduces the energy absorption in the affected pole arresters (see Figure 14, right), occurring in the surviving part of the system during voltage recovery after fault clearance. For the InterOPERA setup and selected configuration, this parameter has a limited impact on other relevant quantities.

Before concluding, it is worth commenting on the observed voltage surge front rate with respect to the adopted TOV profile from [8]. The voltage peak U_1 is set to $1.7U_0$, with U_0 equal to 525 kV (i.e., 892.5 kV), and the time to peak t_1 ranges between 4 and 10 ms (the lower bound being retained here). In InterOPERA, some scenarios exhibit a significantly faster time to peak, close to 1 ms, which raises the question of whether these first peaks should be constrained by compliance with the slow DC-TOV profile or by other criteria, such as switching impulse.

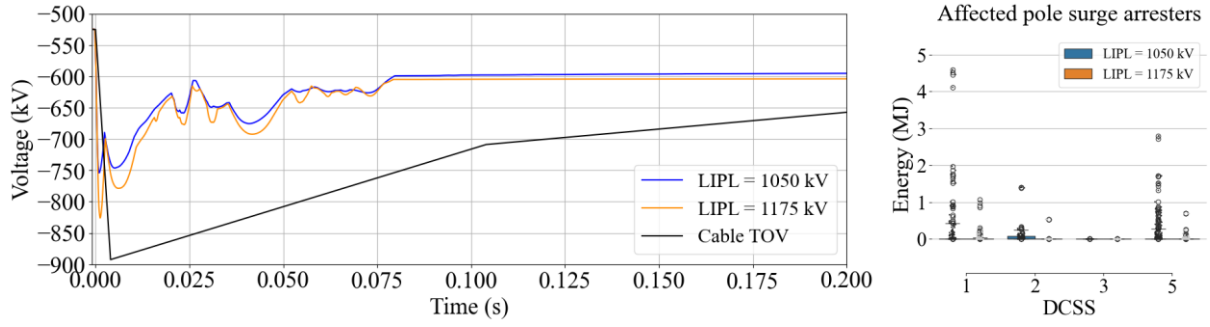


Figure 14 - Observed overvoltage envelopes on the affected pole and related surge arrester absorbed energies for different pole LIPLs (neutral LIPL=83 kV and Grounding resistor=5 Ω)

6 Ensuring AC current zero crossing for converter side single phase faults

In InterOPERA, it was decided to establish a lower bound for the grounding resistor based on the results of single-phase AC faults on the converter side, ensuring current zero-crossing. Although it is acknowledged that alternative countermeasures exist, these are considered vendor-specific and therefore cannot be specified. In this section, the GGG (Grid-Grid-Grid) case, with all three converter stations connected to onshore grids, is considered, since the worst-case scenario for this phenomenon occurs when the NE station is connected to a strong grid.

6.1 A time-domain example: preliminary minimum grounding resistor value

Figure 15 shows simulation results for a fault on phase A at the converter side of the NE station transformer for different grounding resistor values. This station is selected because it is the closest to the central DCSS, where system grounding is assumed, adding the minimum cable resistance ($0.43 \Omega^2$). It should be noted that no open command is issued to the ACCB. Although the highest neutral system protective level is considered here (neutral LIPL = 125 kV), surge arresters may be neglected as a first approximation. In this scenario, the converter blocks following fault inception. Under solid DC grid grounding, the decaying aperiodic DC component of the phase A short-circuit current prevents the current from crossing zero, thereby jeopardising successful ACCB opening within the first cycles after receiving the tripping order. This phenomenon can be effectively mitigated by using higher grounding resistor values.

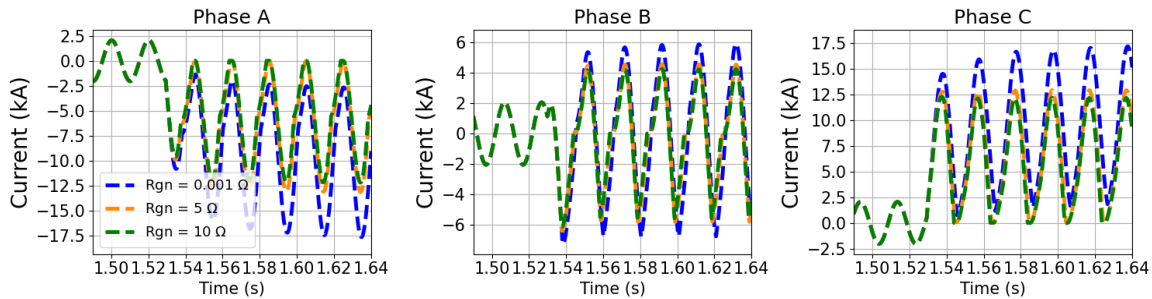


Figure 15 - Three-phase current at the primary (grid) side of the transformer at NE station for different grounding resistance values (neutral LIPL = 125 kV)

² In this work, the DC cable resistance is set to 8.63 m Ω /km, corresponding to a 2500 mm² copper conductor at 70 °C, in accordance with IEC 60228 [13].

6.2 A time-domain example: impact of the neutral system surge arrester protective level

Figure 16 illustrates that reducing the neutral LIPL increases the DC component of the single-phase fault current (see Table 1), thereby decreasing the effectiveness of the selected mitigation measure and causing the non-zero crossing issue to reappear when using the preliminary grounding resistor value initially retained for the InterOPERA demonstrator ($5\ \Omega$). This is due to the neutral voltage limitation reducing the current through the grounding resistor, effectively lowering the equivalent resistance as seen from the AC side. The total DMR current increases, with the difference flowing through the arrester, which partially bypasses the grounding path.

Further parametric analysis indicates that zero-crossing can be reestablished by increasing the grounding resistor and, if necessary, raising the neutral system protective level. For the setup considered in this work, a $10\ \Omega$ resistor remains insufficient for the 83 kV case but enables zero-crossing at a higher setting (e.g., 100-125 kV), for which the DC component of the fault current is below the AC component amplitude. These findings highlight the critical importance of a **coordinated assessment of the grounding system and surge arrester design**, demonstrating how individual subsystem choices influence overall system performance; a deep understanding of these interdependencies becomes particularly crucial in a MV context. In practice, more comprehensive assessments, including point-on-wave investigations, must be performed.

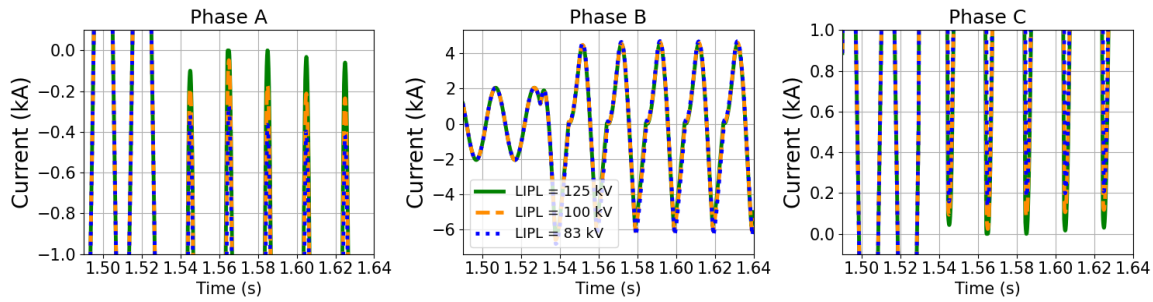


Figure 16 - Three-phase current at the primary (grid) side of the transformer at NE station for different neutral LIPL (Grounding resistor = $5\ \Omega$) – DC offset increase resulting from a DMR LIPL reduction

Table 1 – DC offset vs. AC current amplitude for different neutral system LIPL and grounding resistor

LIPL (kV)	125	100	83
DC offset/AC component/ Δ (kA) – $5\ \Omega$	6.50 / 6.20 / 0.30	6.80 / 6.50 / 0.30	7.20 / 6.70 / 0.50
DC offset/AC component/ Δ (kA) – $10\ \Omega$	5.70 / 5.90 / -0.20	6.17 / 6.19 / -0.02	6.65 / 6.40 / 0.25

7 Conclusion

Driven by the energy transition and the large-scale integration of offshore wind, HVDC technology is evolving from traditional point-to-point links towards MT MV grids, shifting the responsibility for DC-side design from a single OEM to a *System Integrator*. In the InterOPERA project, HVDC grid design studies were conducted using generic models to support subsystem specification [10]. Insulation coordination requirements must remain functional and were therefore limited to minimum withstand voltages and safety margins, defined in accordance with IEC 60071-1 [3], while the surge arrester equipment selection has been left to the OEMs.

Within this framework, early-stage HVDC grid transient design studies validate system-level parameters, primarily the rated and withstand voltages of the HV poles and the DMR, together with the grounding system design (location and resistor value), which are then used as inputs by subsystem suppliers. Whether these requirements are sufficient to ensure robust subsystem design and MV interoperability remains an open question. Overvoltages along DC cables must be verified to remain below the assigned limits, and additional dynamic constraints may apply to other subsystems, such as AC/DC converter stations. This work presents key findings from the InterOPERA demonstrator preliminary insulation coordination study. Although limited to the nominal topology with the central DCSS in service, degraded modes with alternative grounding arrangements should also be assessed in practice if operation under such conditions is planned. From a methodological perspective, the following process is proposed:

1. Establish initial assumptions on HV equipment capabilities and DMR design, including, but not limited to³, rated and withstand voltages, DC-TOV profiles, and current limits.
2. Apply IEC safety margins to determine pole surge arrester protective levels. Using a generic V/I characteristic ensures vendor neutrality and accounts for the unavailability of detailed manufacturer data. Standardised datasets should be used wherever relevant.
3. Define the grounding configuration and determine the minimum suitable resistor value by simulating single-phase AC faults on the converter bus, ensuring fault isolation through guaranteed current zero-crossing at the converter's main ACCB. If a preliminary DMR design is available, surge arresters may be included at this stage; otherwise, this assumption can be refined in a subsequent study iteration.
4. Conduct DC-side transient studies, typically involving comprehensive DC fault simulations, using candidate grounding resistor values and generic surge arrester models, preferably based on standardised V/I characteristics.
5. Assess electrical stresses at all subsystem interfaces, including DC-SCC, TOV, and energy absorption in both the grounding resistor and surge arresters. Particular attention should be given to DMR overvoltages to confirm or adjust the selected protective level.
6. Iterate steps 3 to 5. As illustrated in Section 6, further grounding resistor adjustments may be required to restore current zero-crossing while fine-tuning the DMR surge arrester protective level.

Looking ahead, the InterOPERA project is entering its second phase, in which interaction studies will be conducted in both offline and real-time simulation environments using vendor-specific solutions [11]. The adequacy of the specifications in ensuring that transient stresses remain within equipment capabilities will also be assessed. Should the specifications prove insufficient, lessons learned from the demonstrator are expected to inform updates to the functional framework [12]. Drawing inspiration from AC system practices, these updates could potentially include additional requirements for surge arrester design, limited to protective level alignment or eventually consider the deployment of homologated solutions, to ensure that the expected performance is achieved through enhanced coordination. In this work, investigations were limited to external faults from a subsystem perspective, while focussing on system-level

³ As discussed in detail in [5]- [7], several additional assumptions are required to conduct early-stage HVDC grid design studies. For the transient analysis, DCCB capabilities and reactor sizing are, for example, of particular importance. In this work, the focus is limited to insulation coordination aspects.

arrester design located exclusively at the DCSSs, offering a potential path to mitigate MV design interoperability risks. For instance, in the absence of methodologies to ensure an even distribution of transient stresses among subsystems, the energy burden of such events could be assigned to the DCSSs by specifying slightly higher protective levels for the AC/DC converters.

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