

Optimized Real-time simulation for VSC-HVDC bipolar scheme with physical control replica in the loop

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SUMMARY

This paper investigates various techniques from parallelization and sparse solver solution methods to speed up the real-time simulation of a Voltage Source Converter (VSC)-High Voltage Direct Current (HVDC) bipolar scheme with physical control replica in the loop. The VSC-HVDC bipolar technology is one considered in the InterOPERA project which aims to achieve interoperability of multi-vendor HVDC grids connecting offshore wind farms. To test this interoperability, a real-time simulation demonstrator will contain physical control and protection replicas from each HVDC vendors. The Hardware-In-the-Loop (HIL) setup of each replica involving the Electro-Magnetic Transient (EMT) modeling of HVDC converters is quite challenging in terms of performance in such time-constrained simulations. The EMT solution method used for the simulation is based on the solution of sparse linear systems at each time-point via LDU factorization. Repetitive commutations from HVDC converters slow down this solution process as factorization should be redone from the updated linear sparse system. Otherwise, for parallelization, no natural propagation delay is available to decouple the solution without any loss of accuracy. Sparse solver solution methods based on partial refactorization technique or free-delay parallelization technique such as the Compensation Method are tested on a HIL VSC-HVDC bipolar setup in Static synchronous compensator (STATCOM) mode. Several test scenarios validated the performance gains.

KEYWORDS

EMT-type simulation, Bipolar HVDC transmission system, Modular Multilevel Converter (MMC), Voltage source converter (VSC), Real-Time Simulation, Hardware-in-the-loop (HIL), sparse matrix solver, Parallel simulation, Compensation method, Factorization Paths.

1. Introduction

Energy Transition is reshaping transmission networks. A significant amount of renewable energy from offshore wind farms will be integrated into the grid in the coming decades. High Voltage Direct Current (HVDC) technology plays a key role in connecting these parks to the grid, addressing challenges posed by long distances and higher power ratings. In this context, the InterOPERA project [1] aims to achieve interoperability of multi-vendor HVDC grids connecting offshore winds farms. The selected HVDC transmission system is a bipolar configuration, rated at 2 GW $\pm$ 500 kV with metallic return, and based on the Modular Multilevel Converter (MMC) - Voltage Source Converter (VSC) technology. To assess the performance and stability of such links, Electromagnetic Transients (EMT) simulation is employed to accurately reproduce the fast dynamics of HVDC converters [2]. Real-time Hardware-In-the-Loop (HIL) simulation is necessary to test the dynamic performances of the system with the actual control cubicles. One of InterOPERA's objectives is to build a real-time simulation demonstrator with the physical control and protection replicas from each HVDC vendors to test their interoperability.

A major challenge for this real-time simulation platform is the computation time required to satisfy the real-time clock constraint, as EMT simulations are computationally intensive. Parallelization has been widely adopted as a solution to accelerate the simulation. Propagation delays in DC cables can decouple the simulation without any loss of accuracy. However, for bipolar MMC-VSC converters, no natural decoupling delay is available to enable their parallelized solution. This paper investigates solutions to accelerate the real-time simulation of bipolar converters on a single core and/or through parallelization. EMT simulations involve solving linear sparse systems at each time-point via LDU factorization [3]. Non-linearities and switching events in the converter require repetitive LDU factors computation through iterations, which is computationally intensive. From previous work [4] on sparse solver techniques, the

path-based partial refactorization technique [5][6] can be applied to accelerate this factorization step and achieve fast computations on a single core. For parallelization, it is not straightforward to decouple with artificial delay the two poles of a bipolar converter while keeping the accuracy. Instead, delay-free parallelization techniques such as the Compensation Method [7][8], can be used and have demonstrated promising performance efficiency in [9] while keeping good accuracy. With a faster simulation, the time-step interval can be reduced to improve accuracy and eliminate numerical oscillations. In this work, the real-time simulation environment from [3] is used for implementation and testing.

This paper is organized as follows. Section 2 presents the HIL setup of a bipolar VSC-HVDC in static synchronous compensator (STATCOM) mode from one InterOPERA's HVDC converter vendor which will be part of the up-coming real-time demonstrator. Its complexity in terms of EMT modeling is highlighted. In section 3, various techniques which aim to accelerate the simulation are presented: the path-based partial refactorization technique on one core, the free-delay parallelization techniques such as the Compensation Method on multiple cores. Their accuracy and real-time performance are compared. Final section presents a selection of tested scenarios from the validation of the HIL setup to demonstrate how a lower simulation time-step from the path-based refactorization technique can improve its accuracy and its performance.

2. HIL setup of a VSC-HVDC bipolar scheme

The study system is a VSC-HVDC bipolar converter in STATCOM mode based on the MMC technology. An EMT modelling (Figure 1) is used for the power part. In detail, short circuit Thevenin equivalent are used to represent the AC network. For the MMC VSC converters, a switching function equivalent [10][11] represents each arm as depicted in Figure 1. In operation, for each arm, the status of the two diodes may change at every time-point according to the voltage arm switching function value. Iterations on the nodal solver are required to solve the nonlinear diodes included in the valve model [11]. Each converter is controlled through simulator IOs, by the physical control and protection replica provided by one of InterOPERA's HVDC vendor (Figure 2). With a $40 \mu\text{s}$ time-step, the HIL real-time simulation is run on one core of an OP5033XG target 64 bits Linux with 16 cores (2 CPU Intel Xeon Gold 6234 3.3 GHz – 8 cores).

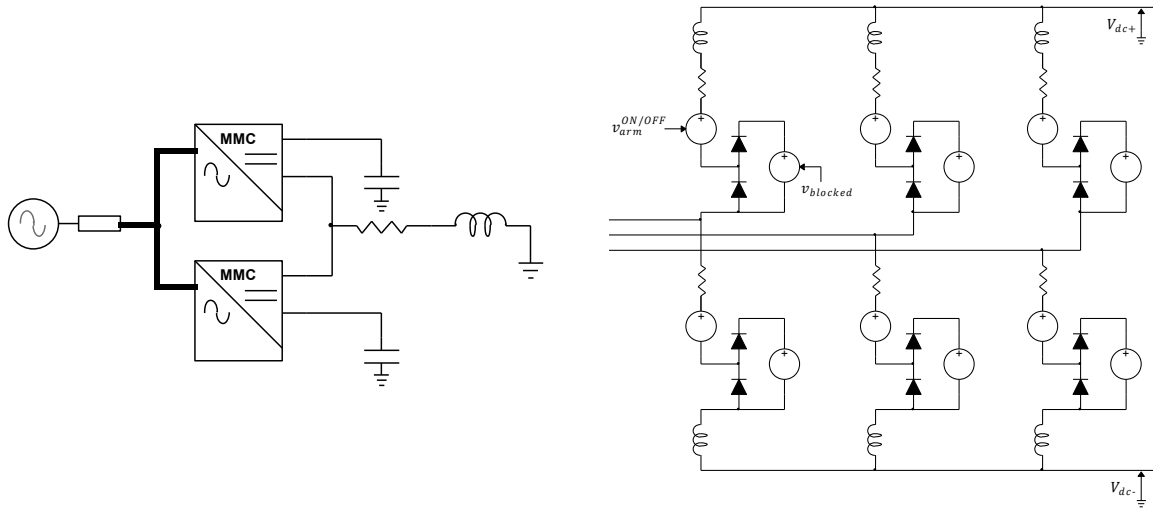


Figure 1 – EMT modelling of a VSC-HVDC bipolar scheme (left), converter equivalent (right)



Figure 2 – View of the VSC-HVDC bipolar control replica in the real-time simulation lab

By using classical nodal analysis, the EMT solution of network equations can be written in a linear form to be solved at each time-point

$$Yv = i \quad (1)$$

Where Y is the nodal matrix, v the vector of unknown voltages and i the vector of current sources including history terms. For nonlinearities, a Newton method is applied where Y is the Jacobian matrix. Indeed, linearized Norton equivalents are provided to Y and i . They are updated at each time-point iteration. The admittance matrix Y is generally sparse and can be unsymmetric. A direct sparse LDU factorization is used to solve (1). The matrix Y is factorized as

$$Y = LDU \quad (2)$$

Where L , U and D are respectively lower triangular, upper triangular and diagonal matrices. Then, a forward substitution is first performed using

$$Lx = i \quad (3)$$

A backward substitution follows it with

$$DUv = x \quad (4)$$

Table 1 displays the data complexity of the converters task for the previous solution steps. One can find the sparse matrix data of Y , with n the whole dimension or the number of nodes, nnz the number of non-zeros and n_{var} the number of variable nodes from time varying and nonlinear components. Additionally, types and numbers of time-varying and nonlinear components are detailed. Rn refers to nonlinear resistor (surge arresters), Ln to nonlinear inductor (transformer saturations), Tr to tap changer transformers, SW to switch (topological switching), DI to diode for power electronic switching. For this case, the factorization step of LDU factors is quite demanding in computation time as several recomputations (refactorizations) are required during the simulation. It comes from switching and nonlinear elements, 73% of the nodes, which modify repeatedly the network matrix. Next part is trying to reduce the computation time of this step.

Table 1 – EMT modelling data complexity

n	nnz	n_{var}	Rn	Ln	Tr	SW	DI
116	462	77	5	6	6	15	24

3. Improving the real-time performance

This part elaborates on two approaches to accelerate the real-time simulation of a bipolar VSC-HVDC converter. The first one is a path-based partial refactorization technique [4]-[6] which aims to improve on one core the efficiency of the recomputation of LDU factors. The second one is based on parallelization by using a delay-free decoupling technique such as the Compensation Method [7]-[9]. Then, a validation and a performance analysis are done for both techniques during the energization process.

3.1. Path-based partial refactorization technique

The LDU factorization is done in-place by the algorithm 1 (Figure 3). This algorithm computes sequentially the set $C = \llbracket 1, n \rrbracket$ of LDU row-columns from the upper-left corner to the lower-right corner. Also, Figure 3 illustrates the LDU factorization where the row-column i is computed. Moreover, the sparsity is managed through code generation which is commonly used for real-time simulation [3]. Since no pivoting is used for the factorization, the sparsity structures of matrix Y and LDU factors do not change and are known prior the simulation. Only non-zero operations are printed in the generated code. When the matrix Y is updated during the simulation, the objective of partial refactorization is to recompute LDU factors by proceeding fewer row-columns in algorithm 1 by minimizing the size of C .

Algorithm 1 LDU factorization without pivoting

for $i \in C$ **do**

$$D_{ii} = Y_{ii} - \sum_{k=1}^{i-1} D_{kk} L_{ik} U_{ki}$$

for $j = i + 1$ **to** n **do**

$$U_{ij} = \frac{1}{D_{ii}} \left(Y_{ij} - \sum_{k=1}^{i-1} D_{kk} L_{ik} U_{kj} \right)$$

$$L_{ji} = \frac{1}{D_{ii}} \left(Y_{ji} - \sum_{k=1}^{i-1} D_{kk} L_{jk} U_{ki} \right)$$

end for

end for

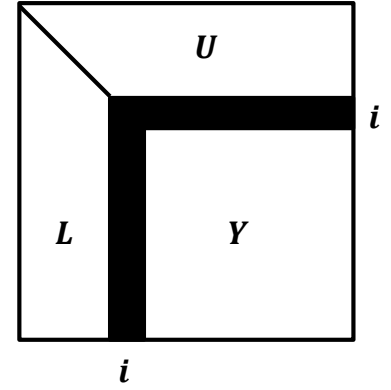


Figure 3 – LDU factorization algorithm

A traditional technique used in real-time is to first reorder Y by putting time-varying and nonlinear elements in the lower-down corner as illustrated in Figure 4. This guarantees to have at least $C \subseteq \llbracket n - n_{var}, n \rrbracket$ where only the variable lower-down corner needs to be refactorize. The LDU factors of the fixed part, L_{fixed} , D_{fixed} and U_{fixed} remain constant during the simulation. Additionally, at each time-point, the minim index of changed nodes, n_{chg} , can be determined. Then, only row-columns from n_{chg} of the updated part of Y , Y_{chg} , require a refactorization ($C = \llbracket n_{chg}, n \rrbracket$). This technique is called RefactChg.

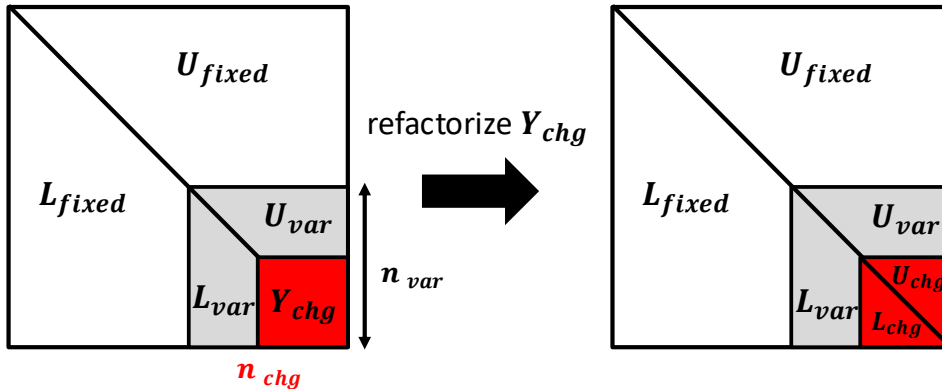


Figure 4 – Current partial refactorization technique

The path-based approach, RefactPath, consists of determining a minimal subset of row-columns between n_{chg} and n which require recomputation after changes in Y by considering row-column dependencies in the LDU factorization. These row-column dependencies can be directly extracted from the sparse pattern of matrix L . More details are available in [4]. If $L_{ij} \neq 0$, then row-column i depends on row-column j in the factorization process. When a row-column j_0 is updated, the sequence of row-column to refactorize (algorithm 2 in Figure 5), its factorization path, $path_{j_0}$, can be obtained by recursively traversing its first non-zero off-diagonal element at row k . Then, j_0 is added to the

factorization path and k is considered to the next column to traverse. The traversing ends when no non-zero off-diagonal element is found or the last column n has been proceeded. As the sparse pattern of L does not change during the simulation, all factorization paths from variable row-columns between $n - n_{var}$ and n can be precomputed prior the simulation. During the simulation, algorithm 3 in Figure 5 merges all factorization paths into $C_{RefactPath}$ of the row-columns updated in Y . The size of the subset of row-columns, $C_{RefactPath}$, to refactorize, is expected to be lower than $n - n_{chg}$ to have a faster refactorization of LDU factors.

Algorithm 2 Factorization path of row-column j

```

found = true
j0 = j
while found do
  pathj = pathj ∪ {j0}
  found = false
  for k ∈ [j0 + 1, n] do
    if Lkj0 then
      j0 = k
      found = true
      break
    end if
  end for
end while

```

Algorithm 3 Compute $C_{RefactPath}$

```

CRefactPath = ∅
foreach Yij updated in Y do
  j0 = min(i, j)
  CRefactPath = CRefactPath ∪ pathj0
end foreach

```

Figure 5 – Factorization path and row-columns sequence to refactorize algorithms

To illustrate it, one considers a seven nodes network ($n = 7$) with its L sparse structure in Figure 6 (a). Grey boxes indicate non-zeros elements in L . For a changed value (1,3) in Y , the corresponding initial updated row-column is $\min(1,3) = 1$. The traversing of column first off-diagonal non-zero gives the following factorization path $\{1,3,6,7\}$, green boxes in Figure 6 (b). For a change value in (6,7), the factorization path is $\{6,7\}$, blue boxes in Figure 6 (c). By combining both factorization paths, the row-column sequence to update is $C_{RefactPath} = \{1,3,6,7\}$. Its size is less than the sequence from the previous refactorization technique, RefactChg, where $C_{RefactChg} = \{1,2,3,4,5,6,7\}$. With fewer row-columns to recompute RefactPath is expected to be faster.

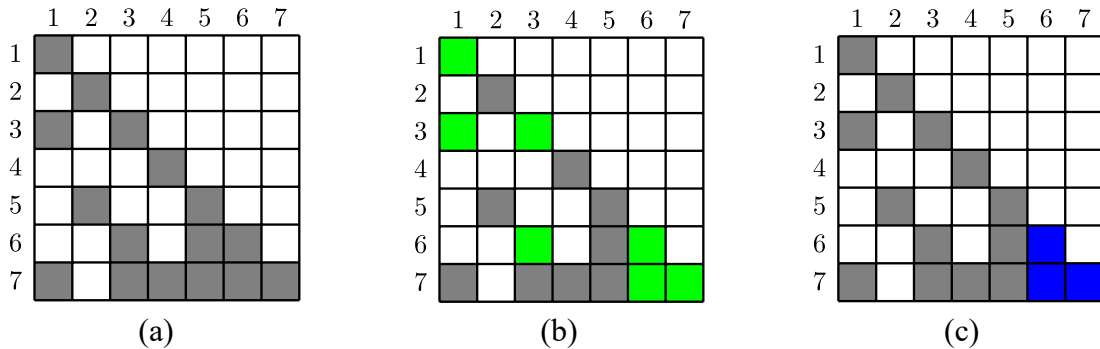


Figure 6 – Sparse pattern of matrix L (a), factorization path traversing for changes (1,3) in (b) and (6,6) in (c)

3.2. Parallelization through Compensation Method

The Compensation Method (CM) [7]-[9] is a free-delay technique which decouples a network into subnetworks by cutting through wires. For the case of the bipolar VSC-HVDC converter in Figure 7, a per pole decoupling is done by CM through wires cuttings in the AC and DC sides.

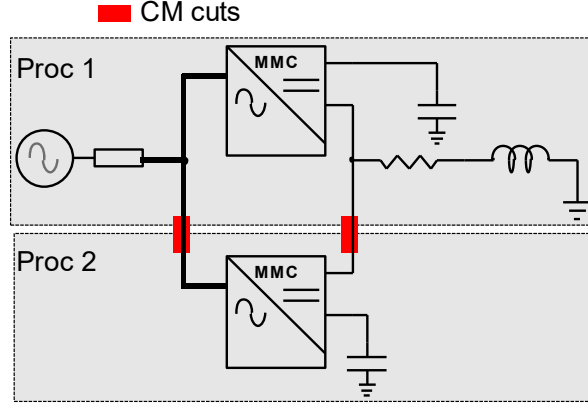


Figure 7 – Compensation Method decoupling for the bipolar VSC-HVDC converter

It is equivalent to add extra variables, wires or compensation currents, to the network equations formulation. The following bordered-block diagonal form is obtained for the two subnetworks of Figure 7,

$$\begin{bmatrix} Y_1 & 0 & S_1 \\ 0 & Y_2 & S_2 \\ S_1 & S_2 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_c \end{bmatrix} = \begin{bmatrix} i_1 \\ i_2 \\ 0 \end{bmatrix} \quad (5)$$

Where Y_i , v_i and i_i are the nodal formulation elements for the subnetwork in Proc i , i_c the added wires or compensation currents from decoupling, S_i the connectivity matrices for interconnecting the two subnetworks through wires with zero impedance. The solution of each subnetwork can be processed in parallel once interface variables i_c are computed. The computation of i_c requires the Thevenin equivalents of both subnetworks, (Z_{thi}, v_{thi}) , extracted from the wire cuts. The equivalent network to solve is illustrated in Figure 8. More details on the whole computation process can be found in [9].

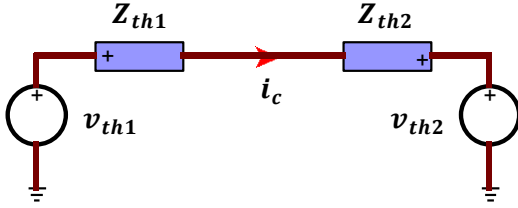


Figure 8 – Compensation Method decoupling for the bipolar VSC-HVDC converter

Table 2 shows the data complexity of the convert task in converter 1 after the CM decoupling which allows to reduce by 40% the dimension of the initial problem. Then, previous partial refactorization technique, RefactPath, can be applied for the network solution.

Table 2 – EMT modelling data complexity after CM parallel decoupling

n	nnz	n_{var}	Rn	Ln	Tr	SW	DI
69	263	44	3	3	3	10	12

3.3. Validation and real-time performance

Validation of both techniques, RefactChg and CM, toward the reference sequential solution (SEQ+RefactChg) is done through a 10 s Software-in-the-loop simulation of the converter energization with a 40 μ s time-step. A generic HVDC controller imported from Matlab/Simulink using an EMT-Simulink interface [12] replaces the HIL setup. The DC voltage for this offline model is ± 525 kV. For precision comparisons, the following relative numerical error between a reference solution vector f and a given solution $\tilde{f}$ is used:

$$e\% = 100 \times \left(\|\tilde{f} - f\|_2 / \|f\|_2 \right) \quad (6)$$

Table 3 displays the validation and the real-time performance with the HIL setup of each method where $e\%$ is the relative error of the DC voltage toward the reference for the SIL simulation, Nb Cores, the

number of cores used and RT Δt , the minimum HIL real-time time-step where no overrun occurs during the energization of the converter. CM offers a good accuracy with a 0.074% relative error toward the reference. The partial refactorization technique, RefactPath, has a higher accuracy with a perfect match. As only a smaller subset of row-columns is processed during the refactorization, its accuracy is the same as the reference. Figure 9 displays a good superposition for the DC voltage for both techniques, CM and RefactPath during the 10 s energization process. In terms of performance, RefactPath reduces by 7 μ s the admissible real-time time-step bringing the same performance gain in one core as parallelization through CM on two cores. The combination of CM with RefactPath does not improve that much the simulation performance with only 1 μ s gained. For this case, SEQ+RefactPath is kept for the rest of the paper using less simulation resource.

Table 3 – Validation and real-time performance results

Solution methods	SEQ		CM	
	RefactChg	RefactPath	RefactChg	RefactPath
Nb Cores	1	1	2	2
$e\%$	0	0	0.074	0.074
RT Δt	36 μ s	29 μ s	29 μ s	28 μ s

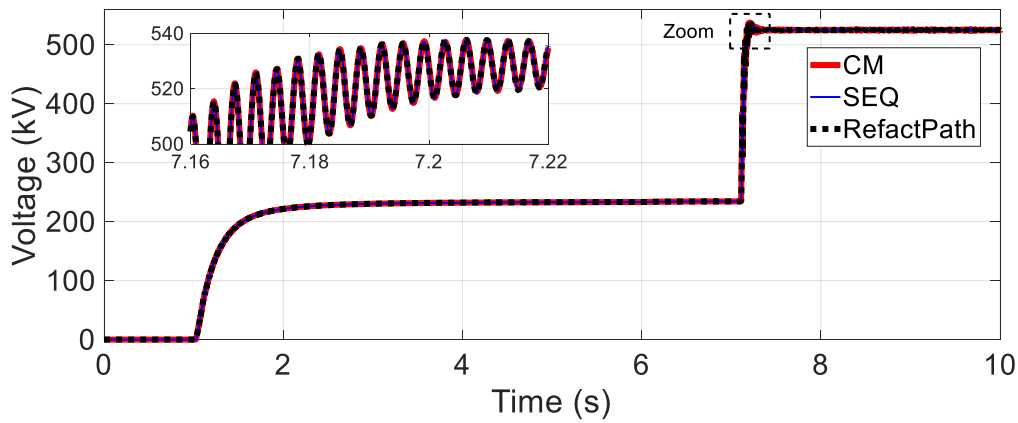


Figure 9 – DC Voltage during the energization SIL simulation for SEQ, CM and RefactPath

4. Validation Tests

In this part, some scenarios from the dry run validation tests of the HIL setup in STATCOM mode are presented to demonstrate the accuracy improvements by reducing the time-step. For the current solver (SEQ+RefactChg), the time-step is set to 40 μ s, for the factorization path technique (SEQ+RefactPath), the time-step is 30 μ s. The following test scenarios are considered:

- Test-1, starting sequence with a reactive power ramp of 200 MVar by using the multi-link control mode.
- Test-2, a permanent DC pole-to-ground fault occurs at the positive pole to validate the well-behavior of the bipolar control.
- Test-3, a permanent AC three phase-to-ground fault occurs at the positive pole station behind the secondary transformer side.

In Test-1 (Figure 10), for the reactive power dispatched on the two poles, oscillations amplitude is damped with a lower time-step from 4 MVar to 0.9 MVar.

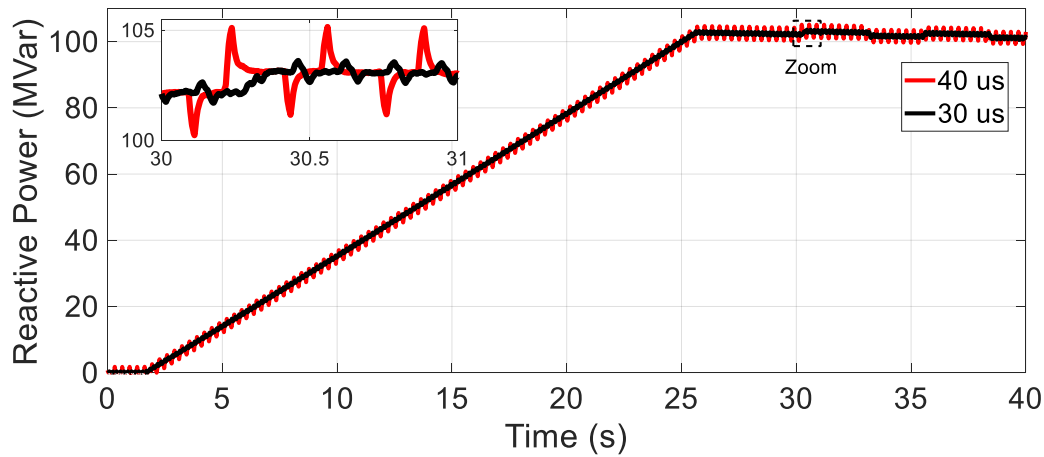


Figure 10 – Test-1 reactive power ramp

In Test-2 (Figure 11), the variation of the time-step has no impact on the well-behavior of a bipolar configuration. A small disturbance is observed on the healthy pole (negative pole) which can continue its operations.

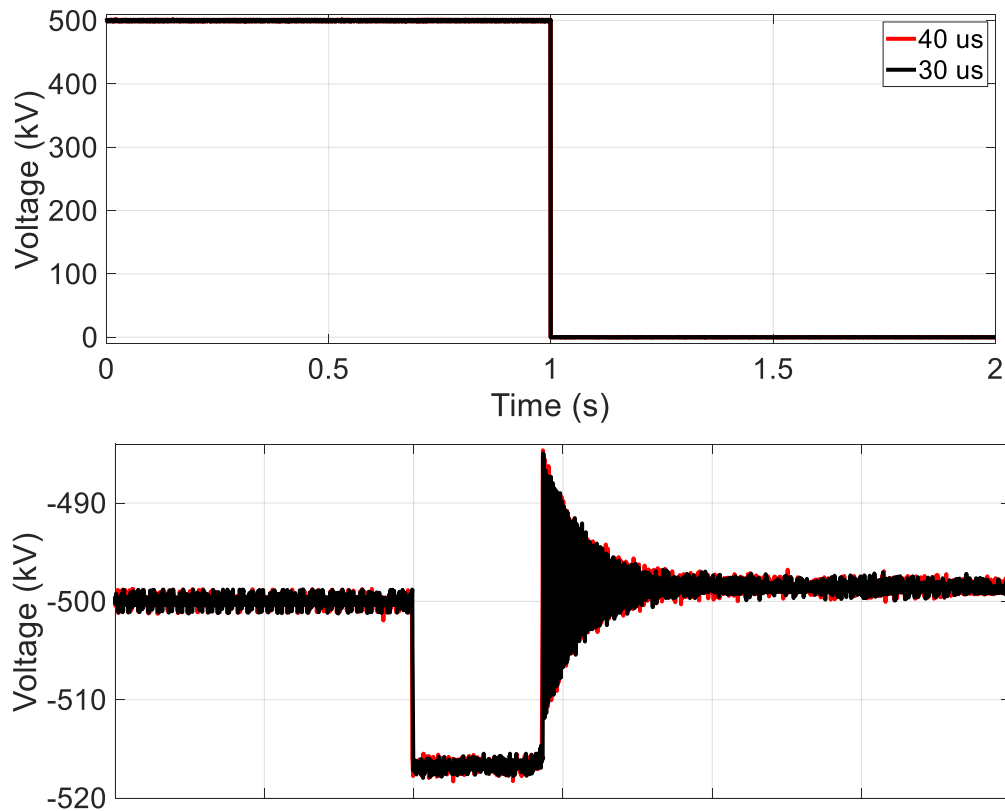


Figure 11 – Test-2, faulty (top) and healthy (down) DC Voltage during the DC fault

On last test (Figure 12), for both cases, the healthy pole is still working after a small perturbation. Differences can be observed on the faulty arm current peak during the three phase-to-ground faults. With 40 μ s, a higher peak by 10% is obtained. It can be explained by a lower sampling rate from the time-step which can impact the reactivity of the control to protect the station (trip) from faulty overcurrent's. With 30 μ s, the control response is faster as the overcurrent peak is reduced.

This part has showed through a sample of tests that a gain of 10 μ s for the time-step impacts the simulation results by damping reactive power oscillations or having a faster control response.

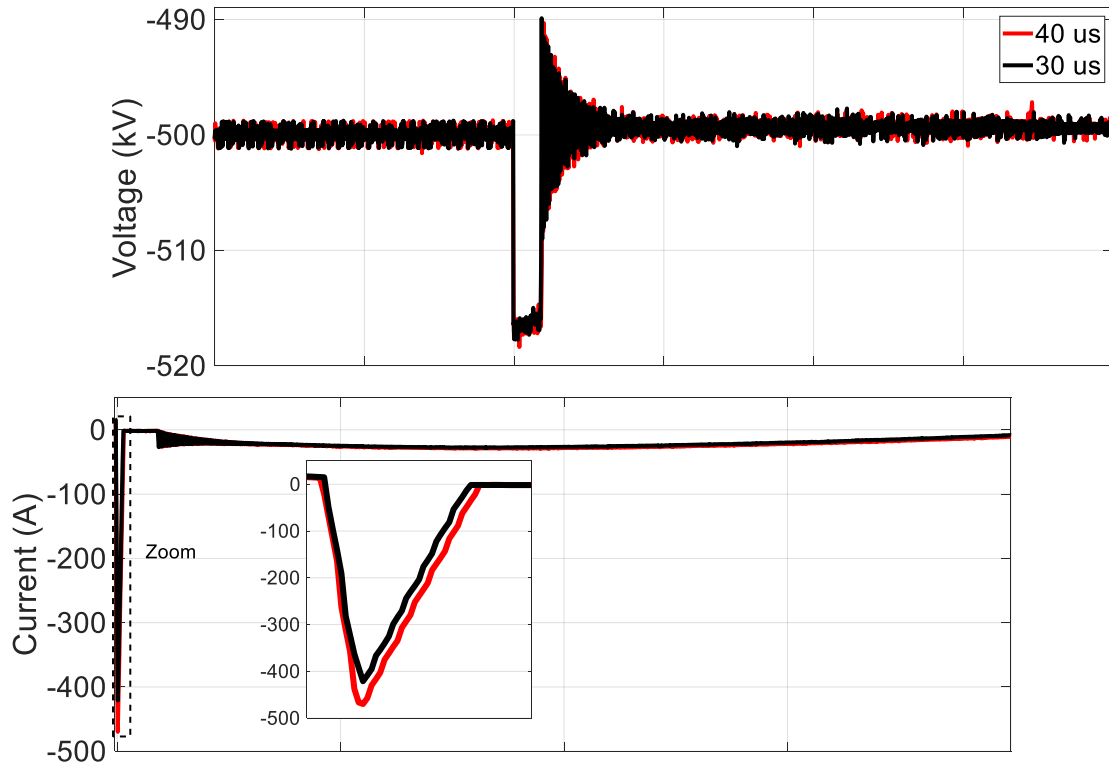


Figure 12 – Test-3, healthy DC Voltage (top) and faulty arm current phase a (down) during the AC fault

5. Conclusion

This paper has investigated two approaches to optimize the real-time simulation of an VSC-HVDC bipolar scheme with physical control replica in the loop: the path-based partial refactorization technique and the Compensation Method, a free-delay parallelization technique. Both techniques provide similar performance gains, reducing the real-time time-step by up to 24% while keeping good accuracy. The partial refactorization technique has been selected as it requires fewer simulation resources, using only one core compared to the two cores required for the parallelization from the Compensation Method.

A set of dry run tests demonstrates the impact of a reduced time-step on the simulation accuracy. Numerical oscillations are damped, and a faster control response is obtained. Applied only to the STATCOM mode, the path-based partial refactorization technique can be used for larger HVDC transmission systems in a bipolar configuration such as that used in the final InterOPERA demonstrator test case. Although long DC cables enable parallel decoupling, bipolar converter tasks can be accelerated on a single core by using the partial refactorization technique.

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DISCLAIMER

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